A 140-GHz Power Amplifier in a 250-nm InP Process with 32% PAE

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***Abstract*— This work presents a 120- to 140-GHz 250-nm Indium Phosphide (InP) HBT power amplifier (PA) capable of delivering 15-dBm saturated output power (P_{sat}) and 32% power added efficiency (PAE). The PA is designed using a pseudo-differential common-base (CB) stage to improve the power gain and power-added efficiency (PAE). A load-line matching design methodology is described for CB topology using a planar sub-quarter wavelength balun (SQWB). The chip size is $0.4mm * 0.5mm$ including pads. To the authors' current knowledge, this is a record PAE for D-band PAs using any integrated circuit process.**

***Keywords*— millimeter-wave, D-band, 140-GHz, power amplifier, power-added efficiency**

I. Introduction

Emerging 5G and future wireless communication schemes place an acute challenge to achieve high efficiency and high power in the power amplifier (PA). While there are diminished improvements in f_{max} for Silicon-based semiconductors (Si, SiGe), these typically come at the expense of lower breakdown voltage. Consequently, III-V compound semiconductors, e.g. GaAs, GaN, and InP, can offer higher output power as well as continued improvements in f_{max} through device engineering. The combination of improved output power and potential efficiency will play a key role in the feasibility of communication system beyond 100GHz.

The 250nm InP HBT has a peak f_t/f_{max} of around 350/600GHz and has been demonstrated for applications above 100 GHz [1], [2]. The high f_{max} suggests that the 250-nm InP HBT should realize high PAE. At a given output power, increasing gain or decreasing the DC power consumption by shifting towards class-B or class-C operation are two methods to improve the PAE. In [1], [2], a 110-150GHz, 24dBm P_{sat} 5-stage PA was presented with 7% PAE. In [3], a 15.5dBm P_{sat}, 5.7% PAE 130nm SiGe PA was presented. Although these work could provide the high output power, the PAE are less than 10% and limit the attractiveness for communication systems that operate at lower average efficiencies.

In this work, we demonstrate high-efficiency through class-B biasing to maintain high gain and linearity while decreasing the DC power consumption compared to prior work based on class-A biasing. In Section II, we demonstrate improved gain from the PA stage through the use of a pseudo-differential common-base PA stage. In the CB topology, the SQWB should be designed with specific matching network to satisfy both input and output matching conditions. In Section III, we introduce a new loadline matching approach that improves the efficiency at peak power. In Section IV, we present measurement results with comparison to the simulation results.

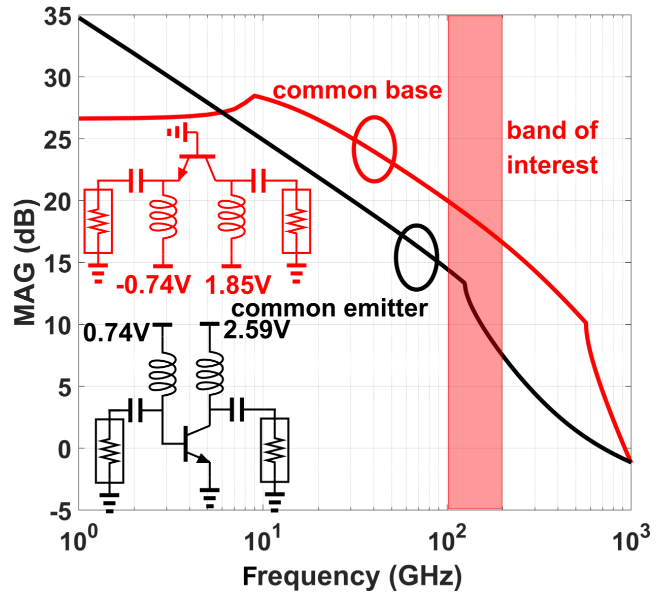

Fig. 1. MAG of a $4um * 4$ InP HBT biased at $266\mu A/\mu m$ for common emitter and common base configurations

II. Common-base InP PA Stages

Fig. 1 plots the MAG for a common-emitter (CE) and common-base (CB) transistor at a collector bias current density of $266\mu A/\mu m$. At 140 GHz, the HBT could provide maximum available gain (MAG) of 7 dB with the CE topology and 17 dB with the CB topology. In general, the CB topology always offers higher MAG at any frequency. In an InP HBT, the parasitic capacitance C_{CE} is much smaller compared than C_{CB} due to the vertical device structure. Feedback current from the CB topology is therefore much smaller than in the CE topology and the PA could be unconditionally stable without stabilization circuit. However, the base inductance greatly impacts the stability of the CB configurtation. Using the InP HBT process, the base can be directly connected to ground to eliminate any bypass capacitance requirement to produce an AC ground at the base node. Consequently, the emitter and the collector are biased from positive and negative rails. In Fig. 2, a layout of the $4\mu m * 4$ common base PA is shown that the base of HBT is directly connected to the ground to reduce the resistance and inductance from base to ground. The emitter and collector are connected to baluns on the input and output. Above 100 GHz, loss from the matching

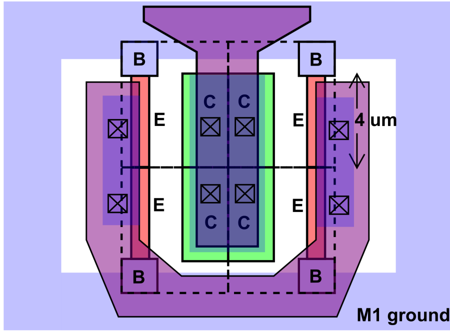

Fig. 2. Footprint of $4\mu m * 4$ CB HBT

network or stabilization network is a critical factor that reduces the PAE. To improve the PAE, the matching networks need to be synthesized to introduce low loss.

III. Sub-quarter wavelength balun with CB device matching

In [4], [5], a sub-quarter wavelength balun (SQWB) at W-band was proposed as a power combining technique for mm-wave power amplifier with using a CE differential pair. The SQWB has the advantage of reducing the power combiner area as well as the insertion loss (IL). In [4], the impedance seen into the SQWB is 25Ω with shunt inductance for each path. The balun is sized such that the shunt inductance tunes resonantly with the output parasitic capacitances from the HBT.

The SQWB is a primary consideration in the pseudo-differential design. A shorter transmission line (t-line) electrical length has advantage of lower loss but the disadvantage of higher amplitude and phase imbalance between the two paths. The balun length is swept assuming a 25-Ohm characteristic impedance to find the lowest average loss since the two paths of the SQWB are not identical. At 130-GHz, the electrical length is $\lambda/10$ to keep the loss as low as 0.3dB with 0.4dB imbalance. The impedance seen into the balun is 25Ω with shunt inductance.

For CB devices, the impedance seen looking into the emitter is different than the impedance looking into the collector. While $I_E \approx I_C$ for sufficiently large β, the voltage gain is directly proportional to the ratio of the impedances at the collector and emitter. We choose the impedance of emitter port to be close to 25Ω and requires a larger impedance seen at the collector. In Fig. 3, a load pull simulation result for the CB configuration is shown for a $4x4um$ device with input matching to 25Ω and a shunt inductor at the output to tune the load impedance close to real axis. Note that the peak power and peak efficiency occur under similar matching conditions. The peak output power is 14.5 dBm with 45% PAE with a 100Ω load.

Fig. 4 plots the Smith chart representing impedances seen into SQWB (Z_A) as well as from the collector and emitters. For input matching (Z_D), a shunt capacitor is added to match the input to a 25Ω impedance. In our implementation, this shunt capacitor comprises the HBT intrinsic parasitic capacitance C_{be} and an explicit capacitor. For the output matching (Z_C), a series inductor produces an impedance transformation from the 25Ω constant contour (Z_B) to match to the 100Ω constant contour (Z_C) as shown in Fig. 4 in red.

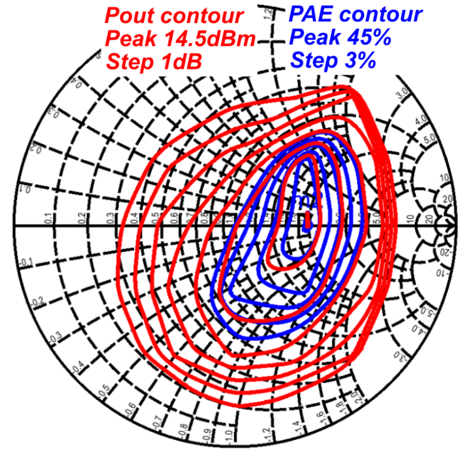

Fig. 3. Load pull simulation of a 4x4um CB HBT biased at $266\mu A/\mu m$

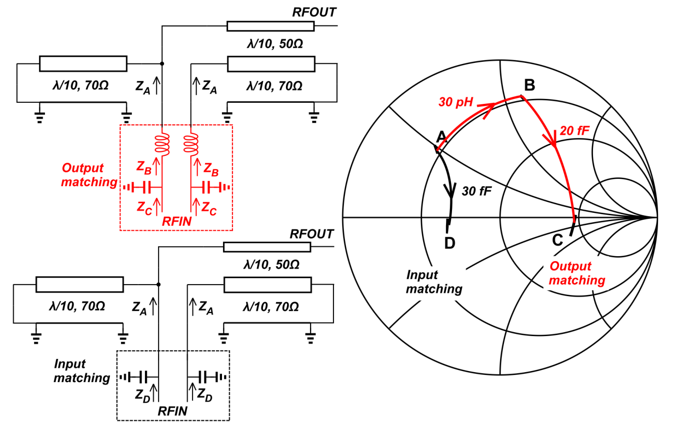

Fig. 4. Input and output matching network with sub-quarter wavelength balun with conceptual matching approach

Fig. 5 illustrates the pseudo-differential CB PA stage schematic and indicates the input and output SQWB implementations at the emitter and collector. The SQWBs are connected in reverse at the input and output ports to reduce the impact of imbalance. This equalizes the loss and phase difference from the two paths.

IV. PA implementation and measurement results

The PA is implemented with a 250nm InP HBT process and is shown in Fig. 6. The chip size is $0.4mm*0.5mm$ including the DC and RF pads. The V_{EE} is set to be $-0.74V$ for a class-B bias condition. The V_{CC} is $1.85V$ which is within the safe-operating range of the HBT breakdown voltage to provide high output power with reliable operation.

The chip is measured with a 110GHz-170GHz VDI frequency extender head and the Keysight N5247A PNA. The probes

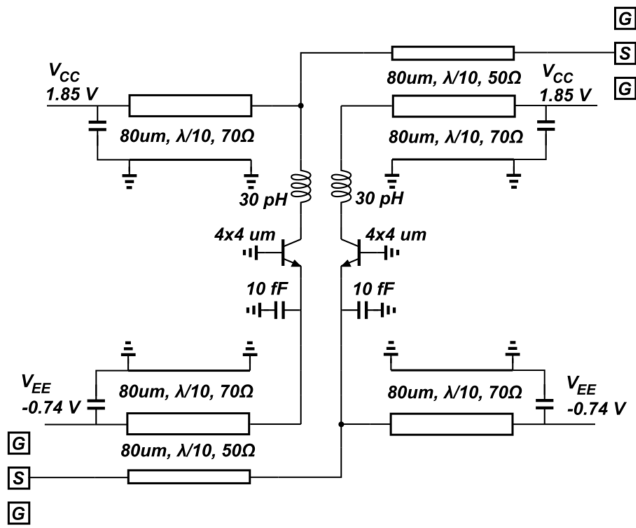

Fig. 5. Schematic of the CB PA with input and output matching

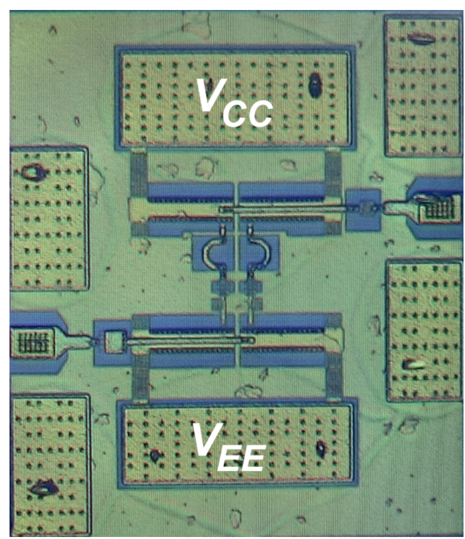

Fig. 6. Micrograph of the 140-GHz, 250-nm InP HBT PA

are GGB waveguide 110-170GHz with $150\mu m$ pitch. Power calibration is performed with an Erickson PM4 power meter. Two different length transmission lines are measured with the same setup to de-embed the loss from the probe under the assumption that probes are identical. The calculated result shows each probe has 2 dB loss. The fixed output power from the VDI head is 10.7 dBm and the S-parameters are measured under relatively high input power conditions as 8.55 dBm. The simulated and measured results are compared in Fig. 7 and demonstrate excellent agreement in between the large signal measurement and simulation results. The peak large-signal S21 is 6 dB with a 116-144GHz 3dB bandwidth.
The power is measured by calibrating the VDI extender heads to measure power levels at each frequency and level setting. The loss of the probes has been de-embedded from the measurements. The emitter current is monitored and used to calculate the total power consumption. Fig. 8 plots PAE

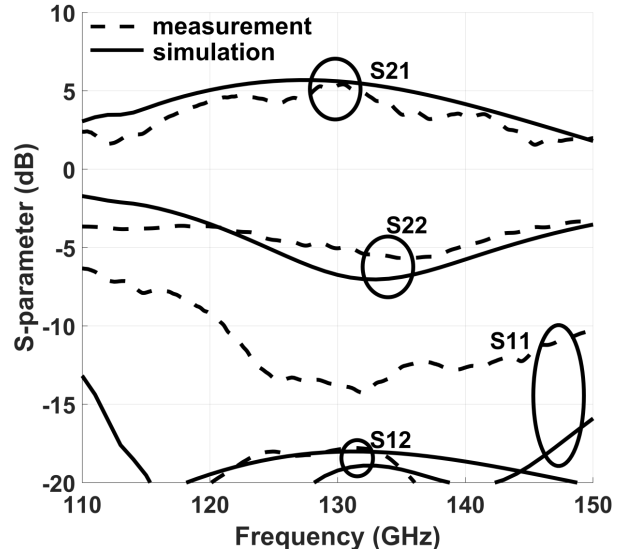

Fig. 7. Comparison of the simulated and measured S-parameters

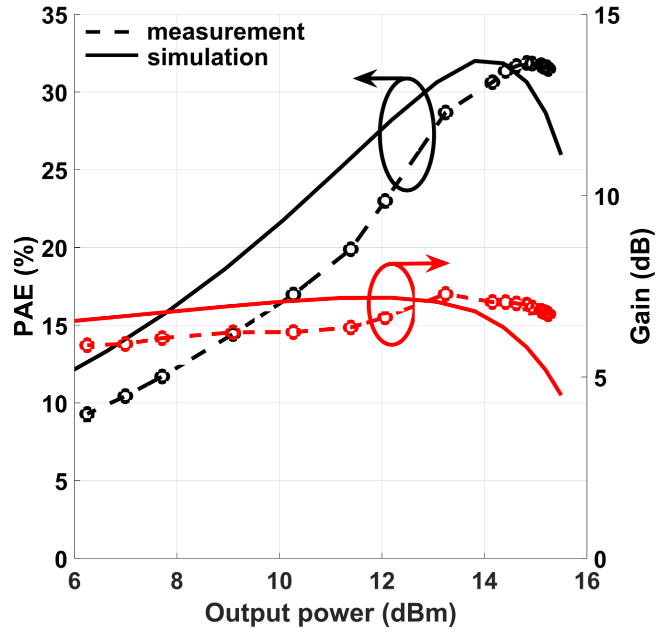

Fig. 8. Large-signal characterization of the PAE and gain

as a function of P_{out} and AM-AM results comparison at 130 GHz. The peak gain occurs at P_{out} of 13-dBm at 7dB. This PA achieves 32% peak PAE with 15.3dBm P_{sat}. Fig. 9 shows the P_{sat} and PAE over the band. The input power across the band is calibrated to between 8dBm and 8.7dBm with variation due to the probe loss variation over the band. From this result, the 3dB power bandwidth is from 118GHz to 148GHz.

V. Conclusion

In this work, a 120- to 140-GHz, 250-nm InP HBT PA is demonstrated with 15.3dBm P_{sat} and 32 % PAE. The PA is based on a pseudo-differential CB PA is designed with low loss sub-quarter wavelength baluns. A matching network design methodology is demonstrated could be easily used for

Comparison with state of art D-band PAs

Ref.	Technology	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE (%)	Chip Size (mm^2)
[1]	250nm InP HBT	110-150	14-16	24	20	8.87	1.88
[3]	130nm SiGe HBT	131-180	27	14	13.2	5.7	0.48
[6]	0.14μm GaN DHFET	98-122	22	27	-	7	6.98
[7]	0.1μm‘ InP HEMT	65-140	6-8	14	-	2-4	1.68
[8]	90nm SiGe BiCMOS	110-140	7.7	22	-	3.6	0.62
This work	250nm InP HBT	118-148	7	15.3	14.4	32	0.2

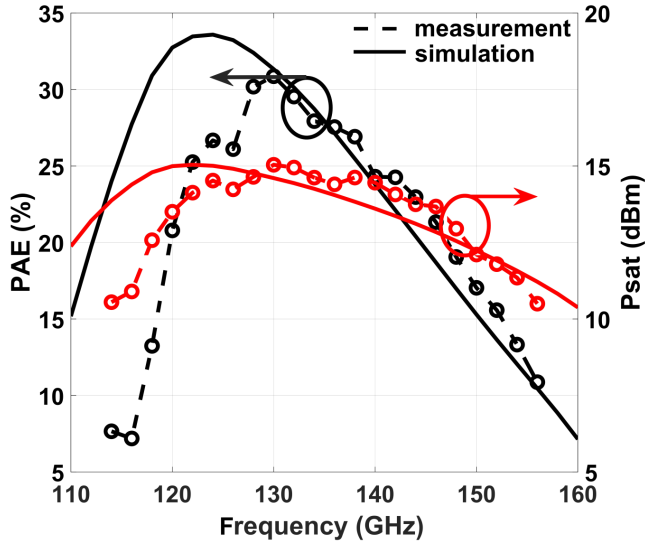

Fig. 9. Psat and PAE over the frequency band

future design that tuning to another frequency. The high PAE indicates the potential for future communication systems above 100 GHz.

Acknowledgment

The author would like to thank the funding support of JUMP program task 2778.10 by the Semiconductor Research Corporation (SRC) and Prof. Gabriel Rebeiz for lending testing equipment.

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