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Towards Energy Efficient Mobile Wireless Receivers Above 100 GHz

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ABSTRACT Wireless communication above 100 GHz offers the potential for massive data rates and has attracted considerable attention for Beyond 5G and 6G systems. A key challenge in the receiver design in these bands is power consumption, particularly for mobile and portable devices. This paper provides a general methodology for understanding the trade-offs of power consumption and end-to-end performance of a large class of potential receivers for these frequencies. The framework is applied to the design of a fully digital 140 GHz receiver with a 2 GHz sample rate, targeted for likely 6G cellular applications. Design options are developed for key RF components including the low noise amplifier (LNA), mixer, local oscillator (LO) and analog-digital converter (ADC) in 90 nm SiGe BiCMOS. The proposed framework, combined with detailed circuit and system simulations, is then used to select among the design options for the overall optimal end-to-end performance and power tradeoff. The analysis reveals critical design choices and bottlenecks. It is shown that optimizing these critical components can enable a dramatic 70 to 80% power reduction relative to a standard baseline design enabling fully-digital 140 GHz receivers with RF power consumption less than 2 W.

INDEX TERMS Energy efficiency, optimization methods, power optimization, nonlinear systems, Terahertz, millimeter wave, 5G, 6G, mobile communication.

I. INTRODUCTION

There has been growing interest in communication systems above 100 GHz where vast swaths of largely unused spectrum offer the potential for links with massive data rates and ultra low latencies [1]. These bands include both the upper millimeter wave (mmWave) frequencies from 100 to 300 GHz as well as the terahertz (THz) band from 300 GHz to 3 THz. With the deployment of fifth generation (5G) systems in the lower millimeter wave bands (particularly 28, 37 and 73 GHz) underway, the frequencies above 100 GHz are now being actively considered for potential 6G use cases [2], [3].

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Although communication above 100 GHz has enormous potential, the development of consumer communication devices operating in the frequencies faces significant technical obstacles. A key challenge, and the focus of this paper, is *power consumption*, an issue particularly important for mobile and portable devices. To overcome the high isotropic path loss in the mmWave and THz bands, systems require a large number of elements for sufficient beamforming gain [4]. These high-dimensional arrays increase the number of RF chains, drawing significantly more power. Signals must also be processed at high sample rates, increasing the power in both the ADC and baseband processing. In addition, front-end devices above 100 GHz are still in their infancy [5]–[8] and operate at much lower efficiencies than circuits below 100 GHz.

One recent initial estimate [9] for the state-of-the-art in power consumption is sobering: A 2 GHz mobile receiver with 64 antennas operating at 140 GHz, a likely configuration for 6G cellular applications at the UE [2], could consume approximately 7 W of power. Moreover, even this high value was achieved only after using state-of-the-art devices combined with aggressive bit width reduction on the ADCs. Moreover, the 7 W power consumption number was almost *30 times* greater than the estimated power consumption of a 28 GHz receiver with typical 5G parameters [10].

The broad purpose of this paper is to provide a methodology to understand the performance and power consumption tradeoffs in the receiver radio frequency front-end (RFFE) and develop new designs to better optimize that tradeoff. To this end, we develop an analytic framework for characterizing the end-to-end performance of a large class of potential receiver designs. In the proposed framework, we model a general multi-antenna RFFE and beamformer as a mathematical transform that may include both non-linearities and noise. Then, to measure the performance of the receiver, we define an *input-output SNR* relation that describes the effective SNR at the output of the RFFE as a function of the received SNR at the input to the RFFE. The output SNR can rigorously bound the information-theoretic capacity of the link as this provides a useful metric for system evaluation. Also, since mobile receivers experience signals over a large range of received powers, the input-output SNR relation describes the performance over this input received power range, as opposed to a single input power level.

We then consider the circuit design of common components of the receiver to understand their impact on the end-to-end performance. Our analysis considers state-of-the-art high-frequency RF designs for the low noise amplifier (LNA), mixer, local oscillator (LO), and analog-to-digital converter (ADC). For each component, we perform detailed circuit simulations of various designs in 90 nm SiGe BiCMOS, a popular technology process for mmWave RF [11]. We can then search among the design options in each of the components to find the set of design configuration with the overall optimal performance. Prior power estimation works such as [9], [12], [13], generally used a fixed selection of components in the power analysis. With the proposed methodology, we can identify the key design knobs in each component and mathematically relate those knobs to their impact on the overall performance. This analysis in turn enables us to locate the critical areas for power consumption and better optimize the power consumption for a given performance level.

CONTRIBUTIONS OF THIS WORK

The proposed mathematical framework and circuit design analysis enables several interesting designs insights that may impact design:

- *Effective Noise Figure and Saturation SNR:* We argue that, for a large class of practical systems, the input-output SNR relation can be described by two key parameters: (i) An *effective noise figure* that applies in a low input signal regime, and (ii) a *saturation SNR* that applies in a high input SNR regime. In most practical systems, the effective noise figure corresponds to the value from the classic noise figure analysis of linear systems, while the saturation SNR is determined by the non-linearities in the RFFE components.
- *Power optimization methodology:* This performance characterization leads to a natural power optimization methodology: select the components in the RFFE chain to minimize the total power consumed subject to a maximum effective noise figure and minimum saturation SNR. Since both quantities can be easily computed for a given design choice, the procedure provides a simple and effective power optimization methodology.
- *Linearity requirements and potential power savings:* It is well-known that most cellular and wireless LAN systems rarely use high SNRs. In our framework, this fact implies that the saturation SNR target can be significantly relaxed. The consequence at the circuit level is that linearity requirements can be reduced offering the potential to dramatically save power.
- *Application to* 140 GHz *receivers for 6G*: We apply this concept to the design of a fully digital, super-heterodyne receiver targeted for potential cellular applications. We use realistic parameters for 140 GHz licensed spectrum discussed in [9]. We focus on a fully digital design, as opposed to standard analog beamforming, since it enables rapid search that is valuable in mobile applications for initial access in [14], [15], beam tracking [16], low latency recovery from blocking [10], [17], [18], and aggressive use of idle and DRX modes [19]. That being said, the proposed design methodology is general and could also be applied to standard analog beamformers with phase shifters.
- *Mixer optimization*: Similar to several other works on fully digital receivers, we consider low resolution ADCs (e.g. 3-4 bits) for low power consumption [12], [20]–[22]. Consistent with [9], our analysis reveals that once low resolution ADCs are used, the mixer and LO distribution are the dominant components in the power consumption. Using the fact that we can reduce the linearity requirements in the mixer and LO, we propose three optimizations: (i) use of an active mixer instead of a passive mixer, (ii) using significantly lower LO power, and (iii) optimizing the LO splitting. The use of the lower LO power generally decreases the linearity of the mixer. However, our main insight is that, when low resolution ADCs are used, the reduced non-linearity does not significantly impact the end-to-end performance. Equivalently, in our terminology, the saturation SNR is already set by the ADCs.
- *Significant power savings:* Overall, we show that the optimized designs can achieve more than 70 to 85% power savings relative to baseline designs such as [9] without the design optimizations.

- *5G NR simulation:* We develop a 5G-New Radio (NR) link-layer simulator in MATLAB package with detailed RFFE models derived from the circuit simulation [23]. Our results match the analytic performance.

II. SYSTEM MODEL

A. ARCHITECTURE

While our analysis methodology that applies to a large class of receiver architectures, it is useful to focus on a specific case to make the analysis concrete. We thus consider mostly the fully-digital superheterodyne receiver architecture shown in Fig. 1. The receiver has N_{rx} antennas with each antenna supporting an independent RF front-end. Specifically, the signal from each antenna is amplified with a low noise amplifier (LNA), an intermediate-frequency (IF) mixer, an IF image rejection filter, and adaptive gain control (AGC) amplifier, a direct conversion mixer, and a pair of analog to digital converters (ADC). Each ADC is running at the full wideband sample rate f_s.

Although most mobile devices have used phased arrays for RF beamforming in 5G, we consider this fully digital architecture for future radio evolution since it offers the fast beam search in mobile environments [16], that there is a need to support low latency recovery from blocking [10], [17], [18], and aggressive use of idle and DRX modes [19]. Fully digital architectures observe all directions simultaneously [20], [21] to reduce the initial access time by an order of magnitude [14], [15]. To consider practical features of radio architecture and packaging for large arrays, we consider a super-heterodyne structure, as opposed to a direct conversion because it separates the front-end and baseband circuit blocks to support the fine pitch in frequency bands above 100 GHz. Furthermore, it will allow us to optimize the image rejection and the dynamic range of the system [24]. Nonetheless, the analysis can also be applied to phased array and direct conversion architectures as well.

B. CHANNEL AND BEAMFORMING MODEL

Since we are focusing on the receiver, we consider a single input multi-output (SIMO) system where the transmitter transmits a single stream.

We let x_k be the sequence of complex scalar transmitted symbols at the sample rate f_s. To simplify the analysis, we will consider a single path channel where the complex baseband received samples on the N_{rx} antennas are given by,

$$\mathbf{r}_k = \sqrt{E_s}\mathbf{w}x_k + \mathbf{d}_k \quad \mathbf{d}_k \sim \mathcal{CN}(0, N_0\mathbf{I}), \tag{1}$$

where $\mathbf{w} \in \mathbb{C}^{N_{\text{rx}}}$ is the channel vector, E_s is the received energy per symbol per antenna and $\mathbf{d}_k$ is the thermal noise with N_0 energy per sample. For normalization, we assume $\mathbb{E}|w_j|^2 = 1$ for all receive antennas j and $\mathbb{E}|x_k|^2 = 1$. Hence the received SNR per symbol per antenna is E_s/N_0. Since the symbols $\mathbf{r}_k$ appear at the input to the receiver chain, we will call $\gamma_{\text{in}} := E_s/N_0$ the *input SNR per symbol*.

We represent the action of the components of the receiver front-end (e.g. LNA, mixer and ADC) by a general memoryless mapping,

$$\mathbf{y}_k = \Phi(\mathbf{r}_k, \mathbf{v}_k), \tag{2}$$

where $\Phi(\cdot)$ is a function that includes all the gains and nonlinearities in the components and $\mathbf{v}_k$ are additional noise terms added in those components. We will describe these models in detail below for the various RFFE front-end blocks. In a fully digital design, the output $\mathbf{y}_k$ from the front-end will have N_{rx} outputs, one for each RX antenna. We will assume that the RX has perfectly estimated the channel $\mathbf{w}$ and performs digital beamforming along that direction to produce a scalar symbol,

$$\begin{aligned} z_k &= \mathbf{w}^{\mathsf{H}}\mathbf{y}_k = \mathbf{w}^{\mathsf{H}}\Phi(\mathbf{r}_k, \mathbf{v}_k) \\ &= \mathbf{w}^{\mathsf{H}}\Phi(\sqrt{E_s}\mathbf{w}x_k + \mathbf{d}_k, \mathbf{v}_k). \end{aligned} \tag{3}$$

We will call the symbols z_k the *output symbols* of the receiver.

III. UNDERSTANDING PERFORMANCE VIA INPUT-OUTPUT SNR

A. INPUT-OUTPUT SNR RELATION

The mapping from the input transmitted symbol x_k to the output received symbol z_k in (3) incorporates the entire receiver path including the channel, noise, the effects of the gains and non-linearities in the RFFE and the beamforming. Our goal is to characterize the performance of this receiver for the purpose of demodulating symbols x_k in the context of a power constraint. To this end, we introduce a concept of *output SNR* and the *input-output SNR relationship* as follows.

We assume there is some statistical model on the complex symbols where $x_k \sim X$ for some complex random variable X. We will sometimes normalize X so that $\mathbb{E}|X|^2 = 1$. We also assume the noise terms have distributions $\mathbf{v}_k \sim \mathbf{V}$ and $\mathbf{d}_k \sim \mathbf{D}$ for random vectors $\mathbf{V}$ and $\mathbf{D}$. For now, we model the channel as $\mathbf{w}$ as deterministic. Under this assumption, the received symbol, z_k, post-beamforming will be distributed as,

$$Z = \mathbf{w}^{\mathsf{H}}\Phi(\sqrt{E_s}\mathbf{w}X + \mathbf{D}, \mathbf{V}). \tag{4}$$

Using Bussgang-Rowe decomposition [25], [26], we can write the output of the system as a scalar multiple of the input plus an additive noise which is uncorrelated with the input as,

$$Z = AX + Q, \tag{5}$$

where Q is a complex random variable with $\mathbb{E}(Q) = 0$, $\mathbb{E}(QX) = 0$ and $E|Q|^2 = \tau$, and A and τ are given by,

$$A := \frac{\mathbb{E}\left[X^*Z\right]}{\mathbb{E}|X|^2}, \quad \tau := \mathbb{E}|Z - AX|^2, \tag{6}$$

where X^* denotes the complex conjugate of X. Equation (5) shows that, even if the receiver processing is nonlinear, the effect of the receiver chain can be described by a linear model with some gain A and noise Q. In the sequel, we will call A the *the effective channel gain* and call τ *the effective noise energy per symbol*. Note that the effective noise Q will not, in general, be Gaussian.

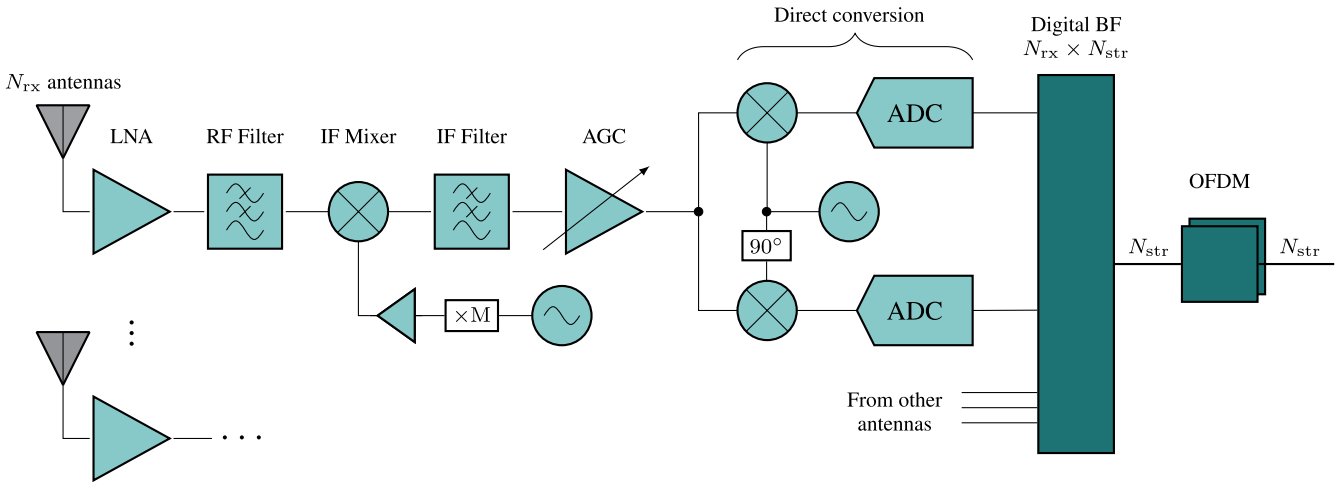

FIGURE 1. High-level architecture of the fully-digital super-heterodyne receiver architecture. The architecture supports N_{rx} antennas and N_{str} digital streams. The light green boxes represent analog and the dark-green boxes the digital components. In the RF front-end, some component are not shown.

In general, both A and τ are functions of the input SNR γ_{in} so we may write $A = A(\gamma_{\text{in}})$ and $\tau = \tau(\gamma_{\text{in}})$. From (5), we can then define the *output SNR* as,

$$\gamma_{\text{out}} = G(\gamma_{\text{in}}) := \frac{|A(\gamma_{\text{in}})|^2}{\tau(\gamma_{\text{in}})}\mathbb{E}|X|^2, \tag{7}$$

which represents the SNR that would be seen in attempting to recover the input transmitted symbol X from the output symbol Z.

We will call the function $G(\gamma_{\text{in}})$ in (7) the *input-to-output SNR* mapping. This mapping will provide the main metric by which we evaluate the receiver performance. Since wireless receivers must operate over a wide range of receiver power levels, we cannot look at a single input SNR. Instead, we need to consider the performance over a range of possible input SNR levels. The function $G(\gamma_{\text{in}})$ in (7) provides exactly this characterization, describing the output SNR for each possible input SNR.

B. OUTPUT SNR AND CAPACITY

The use of the output SNR defined in (7) as a metric for the system performance can be rigorously justified along information theoretic lines. For example, first suppose that the transmitted symbols x_k are i.i.d. complex Gaussian with zero mean and $\mathbb{E}|x_k|^2 = 1$. Then, using [27, Lemma 2] we show in Appendix A that the capacity is lower bounded by the classic Shannon formula,

$$C \geq f_s \log_2(1 + \gamma_{\text{out}}), \tag{8}$$

where the capacity is in bits per seconds and, we recall that f_s is the sample rate.

Now, in many cases, the receiver ADC over-samples the signal to provide digital filtering. In this case, the transmitted symbols x_k would not be i.i.d. Using analysis in [27], we argue in the Appendix B that the capacity can be lower bounded as,

$$C \geq \alpha f_s \log_2\left(1 + \frac{\gamma_{\text{out}}}{\alpha}\right), \tag{9}$$

where α is the fraction of the occupied bandwidth.

C. LINEAR RECEIVERS

First, we consider a linear input-to-output mapping in (7) for the receiver. Specifically, suppose the function $\Phi(\cdot)$ in (2) is

$$\mathbf{y}_k = \Phi(\mathbf{r}_k, \mathbf{v}_k) = C_0(\mathbf{r}_k + \mathbf{v}_k), \tag{10}$$

where C_0 is some scalar gain and $\mathbf{v}_k$ is an input referenced noise,

$$\mathbf{v}_k \sim \mathcal{CN}(0, (F-1)N_0\mathbf{I}), \tag{11}$$

where F represents the noise figure. For simplicity, assume $\mathbb{E}|X|^2 = 1$. In this case, A and τ in (5) are given by

$$A = \|\mathbf{w}\|^2\sqrt{E_s}C_0, \quad \tau = |C_0|^2\|\mathbf{w}\|^2 F N_0, \tag{12}$$

so the output SNR is

$$\gamma_{\text{out}} = \frac{|A|^2}{\tau} = \frac{\|\mathbf{w}\|^2 E_s}{FN_0}. \tag{13}$$

Now, recall that our normalization assumption is that $\|\mathbf{w}\|^2 = N_{\text{rx}}$. Also, the input SNR is $\gamma_{\text{in}} = E_s/N_0$. Hence, the input-to-output SNR mapping in (7) is given by,

$$\gamma_{\text{out}} = G(\gamma_{\text{in}}) = \frac{N_{\text{rx}}}{F}\gamma_{\text{in}}. \tag{14}$$

Hence, the linear receiver increases the SNR by a beamforming gain N_{rx} and decreases the SNR by the noise figure F.

D. NONLINEAR RECEIVERS

Detailed simulations below will show that, for many non-linear functions of interest, the input-output SNR relation can be approximated by a function of the form,

$$\gamma_{\text{out}} = G(\gamma_{\text{in}}) = \frac{N_{\text{rx}}\gamma_{\text{in}}}{F + N_{\text{rx}}\gamma_{\text{in}}/\gamma_{\text{sat}}}, \tag{15}$$

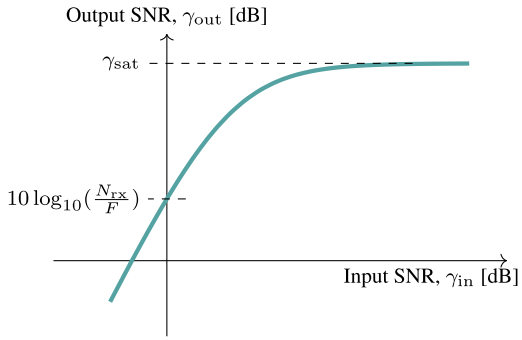

FIGURE 2. Input-output SNR relation with an effective noise figure, F, beamforming gain N_{rx} and saturation SNR, γ_{sat}.

for two parameters F and γ_{sat} that we will call the *effective noise figure* and *saturation SNR*.

The parameters F and γ_{sat} will provide the metrics that we can evaluate the receiver front-end performance. To interpret the roles of the parameters Fig. 2 plots γ_{out} vs. γ_{in} with both the values in dB-scale. We see two distinct regimes.

1) LOW INPUT SNR REGIME

When $N_{\text{rx}}\gamma_{\text{in}}/F \ll \gamma_{\text{sat}}$, the output SNR in (15) simplifies to

$$\gamma_{\text{out}} = G(\gamma_{\text{in}}) \approx \frac{N_{\text{rx}}}{F}\gamma_{\text{in}}, \tag{16}$$

which matches the linear case (14). We will thus call F in (15) the *effective noise figure*. This regime appears on the left side of Fig. 2 where γ_{out} (in dB) increases linearly with γ_{in} with an offset given by beamforming gain N_{rx} minus the effective noise figure F.

We will see below that the low input SNR regime occurs when the RFFE components have sufficiently small input levels that they do not saturate and act linearly. In this case, the effective noise figure is determined by the standard noise figure analysis with an additional term from the quantization noise at the ADC.

2) HIGH INPUT SNR REGIME

At very large input SNRs ($N_{\text{rx}}\gamma_{\text{in}}/F \gg \gamma_{\text{sat}}$), the output SNR in (15) simplifies to

$$\gamma_{\text{out}} \approx G(\gamma_{\text{in}}) \approx \gamma_{\text{sat}}. \tag{17}$$

Hence, the output SNR saturates as shown in Fig. 2. It is for this reason that γ_{sat} is called the saturation SNR. In this case, we will see that the saturation SNR is determined by the nonlinearities in the devices and the quantization in the ADC.

IV. POWER OPTIMIZATION METHODOLOGY

A. OVERVIEW

The above discussion analysis suggests we can characterize the performance of an RFFE with two key parameters: the effective noise figure, F, and saturation SNR, γ_{sat}. A natural power optimization is then to find the design with the lowest power to meet some target noise figure and saturation SNR.

To state this precisely mathematically, suppose that we have a set of potential receiver front-end designs, indexed by some parameter θ. For example, θ could denote the selections of design options in each of the receiver components such as the choice of LNA, mixer, LO power and the number of bits in the ADC. Also, suppose that for each θ, the input-output SNR model (15), provides a close approximation of the actual input-to-output SNR relation. In this case, the performance of each design choice θ can be characterized by the two performance parameters: the effective noise figure, $F(\theta)$, and the saturation SNR $\gamma_{\text{sat}}(\theta)$. Also assume that for each design choice θ we have some estimate of its power consumption, $P(\theta)$.

The design requirement can then be specified by two target values: a target noise figure, F^{tgt}, and a target saturation SNR, $\gamma_{\text{sat}}^{\text{tgt}}$. Given these two targets, we can then find the minimum power needed by the minimization,

$$P_{\min}(F^{\text{tgt}}, \gamma_{\text{sat}}^{\text{tgt}}) := \min_{\theta} P(\theta) \quad \text{s.t. } F(\theta) \le F^{\text{tgt}}, \gamma_{\text{sat}}(\theta) \ge \gamma_{\text{sat}}^{\text{tgt}}. \tag{18}$$

That is, among all the design choices that satisfy the noise figure and saturation SNR targets, $P_{\min}(F^{\text{tgt}}, \gamma_{\text{sat}}^{\text{tgt}})$ represents the minimum power design choice.

B. DESIGN TARGETS AND THEIR SYSTEM IMPACT

The choice of the design targets, F^{tgt} and $\gamma_{\text{sat}}^{\text{tgt}}$, will depend on the particular use case. Nevertheless, it is useful to briefly understand some general principles on how they would be selected.

1) EFFECTIVE NOISE FIGURE

As we saw above, the effective noise figure is relevant in the low SNR regime. From a systems perspective, decoding and detecting in low SNR typically occurs during procedures such as search, synchronization, and control messaging as well as receiving data channels at low order modulation. Typical values for receivers in the mmWave range from 4 to 9 dB [28], [29].

2) SATURATION SNR

The saturation SNR represents the maximum output SNR that the system can achieve. From a systems perspective, this maximum SNR is relevant in two key ways:

- The maximum SNR determines the maximum modulation and coding system (MCS) that the link can support; and
- The dynamic range of power when decoding signals from multiple transmitters, or decoding in the presence of blockers.

What is important is that most commercial systems do not need high SNRs. For example, with the 3GPP New Radio low-density parity check (LDPC) codes, most modulation and coding schemes (MCSs) up to 64-QAM can be decoded reliably with less than 25 dB [30]. Also, in loaded cellular

systems, the SNR including interference is typically less than 5 dB [31].

Moreover, dynamic range requirements are also not typically large. In a cellular system in licensed spectrum, a mobile will generally connect to the strongest serving cell provided there is no restricted association. In unlicensed spectrum, links typically operate with carrier sense and do not transmit until the radio spectrum is free.

3) LINEARITY AND POTENTIAL POWER SAVINGS

The fact that the saturation SNR target can be relatively low will be critical for power savings. As we will see below, the saturation SNR is determined by the nonlinearities in the devices. By relaxing these requirements, we will see there are significant power savings.

V. COMPONENT AND POWER CONSUMPTION MODELS

Having discussed the general power optimization framework, we now study the key components in the RFFE. Our goal is to understand the design choices in each component and how they impact the overall performance. As stated in the Introduction, all the designs are in 90 nm SiGe BiCMOS, although other process nodes could be considered.

A. LNA

In higher mmWave frequencies, the LNA design is challenging due to the noise figure requirements [8]. The overall performance of a receiver is affected by the limited gain and the noise figure of the LNA and these parameters directly impact the effective noise figure of the system. The nonlinearity of an LNA is characterized by the third-order input intercept point (IIP3) that relates the third-order intermodulation distortion (IMD) to the input signal power [32]–[34]. Using the IIP3, we can define the input power that saturates the linear response of the LNA.

The power consumption of the LNA is related to the IIP3 where higher DC power typically allows the LNA to maintain more linear operation and is not incorporated into earlier analysis. In [9], the DC power of an LNA in mW can be calculated as

$$P_{\mathrm{DC}} = \frac{G}{\mathrm{FoM}(F-1)}, \tag{19}$$

where G is the gain, FoM is the figure of merit in mW^{-1}, and F is noise figure of the LNA. All the parameters are in linear scale.

We developed four LNA designs based on a 90-nm SiGe BiCMOS HBT technology to minimize the power consumption at a certain performance in terms of gain, F, and IIP3. The proposed LNAs have multiples stages to achieve a gain exceeding 10 dB, and are based either on a common base (CB) or a hybrid common base and common emitter (CB/CE) topology. Based on the technology all the HBT devices have $f_{\max} = 310$ GHz frequency with a peak performance about 2 mA/μ m. Several studies have characterized the noise minimum in millimeter-wave bands [35], [36]. In Table 1, we summarize the noise figure, gain, IIP3, FOM and DC power for each LNA design.

TABLE 1. Parameters of the LNA designs used in the analysis and evaluation of the receiver model.

Parameter	$\mathrm{LNA}^{(1)}$	$\mathrm{LNA}^{(2)}$	$\mathrm{LNA}^{(3)}$	$\mathrm{LNA}^{(4)}$
Number of stages	3	3	2	4
Topology	CB	CB	CB	CB/CE
Design [µm]	1-2	2-4	4	2-4
Noise Figure [dB]	7.71	7.69	7.50	7.48
Gain [dB]	12.22	11.85	11.13	16.56
IIP3 [dBm]	-3.30	-6.12	-9.15	-8.90
FOM [mW^{-1}]	0.3082	0.4551	0.6049	0.6409
Power [mW]	11.55	7.2	4.8	15.9

TABLE 2. Power consumption of the mixers designs used in the analysis and evaluation of the receiver model.

Parameter	$\mathrm{Mixer}^{(1)}$	$\mathrm{Mixer}^{(2)}$	$\mathrm{Mixer}^{(3)}$	$\mathrm{Mixer}^{(4)}$	$\mathrm{Mixer}^{(5)}$
Design [µm]	6	4	4	2	1
Power [mW]	41	23.6	15.2	9.7	5

B. MIXER

As shown in Fig. 1, we consider a super-heterodyne receiver architecture with two downconvertion stages. In the first stage, we downconvert the RF signal from 140 GHz to an IF around 10 GHz. In the next stage, we use a direct conversion (zero-IF) architecture to downconvert the signal to baseband. This allow us to optimize the image rejection and the dynamic range of the system.

A mixer can be designed either as a passive or an active device. Passive mixers do not consume DC power but require higher LO power. However, LO power in the upper mmWave bands requires significant power consumption to generate. Consequently, we consider active mixer designs for the RF-to-IF stage in order to minimize the power required by local oscillator (LO) for our analysis.

We designed and evaluated five double-balanced active mixers based on the 90nm SiGe BiCMOS HBT technology based on a conventional Gilbert cell design, which provides excellent performance and is widely used in integrated circuit. The mixer performance can be measured based on the noise figure, gain, and IIP3, which are all characteristics that depend on the LO power. In Table 2 we summarize the transistor size as a parameter for each design and we report the DC power consumption in mW. In Fig. 3, we show the noise figure, gain and IIP3 for each design as function of LO input power. Specifically, we show that the LO power the increases with the gain, while the NF decreases.

Since the direct conversion block incorporates variable gain control, it is assumed to operate in the linear regime and does not introduce any extra distortion. The gain of the components before this part make the noise figure introduced by these mixers minimal. Thus, the impact of this circuit in the non-linear behavior of the system is

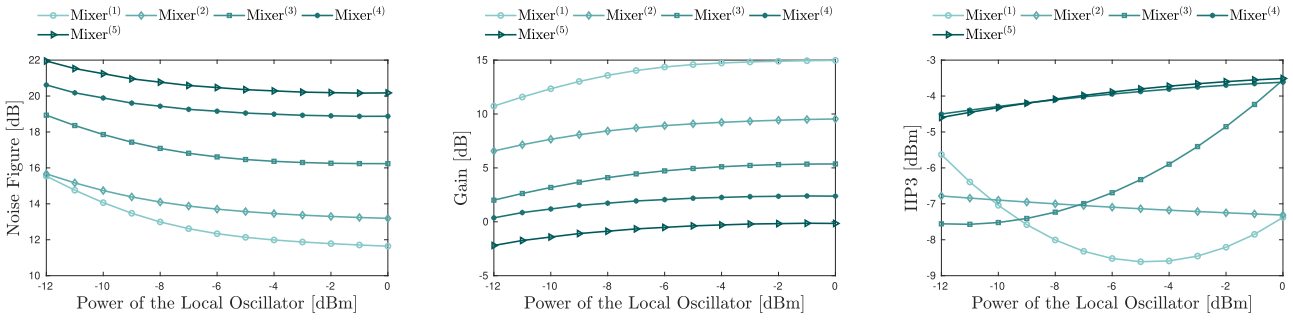

FIGURE 3. Parameters of the IF mixers used in our analysis. We show noise figure in dB (a), gain in dB (b) and IIP3 in dBm (c) as a function of the input LO power.

TABLE 3. Parameters and DC power consumption of the ×4 multiplier design.

P_{in} [dBm]	P_{out} [dBm]	f_{in} [GHz]	f_{max} [GHz]	P_{DC} [mW]
-10	2	32.5	130	48

negligible. We do not consider in our analysis the power of this circuit.

C. LOCAL OSCILLATOR

The available LO power at a 140-GHz LO is typically limited. Consequently, a digital beamformer is considered to be power hungry due to the need to drive the LO at each mixer. With an active mixer, some optimization of the LO power chain can be considered. The LO generation network is based on a ×4 multiplier and buffer (post) amplifier to reach the desired LO power. For example, the multiplier design is based on two frequency doublers. In Table 3 we summarize the parameters and the power consumption of the LO generation network. In [37], an active mixer is used to reduce the required LO power to around −10 dBm and the DC power consumption of the multiplier chain is 57 mW while the active mixer consumes 14 mW. In [6], the power consumption per channel is on the order of 100 mW to generate 3 dBm of LO power to a passive mixer. Based on our design of the LO generation network, the power consumption of the ×4 multiplier and the post amplifier is $P_{\text{mul}} = 43$ mW. In a fully digital system, where we need one mixer per antenna this component will have a major contribution to the total power consumption.

For the system in Fig. 1 we have N_{rx} mixers. Based on our analysis, for $N_{\text{rx}} = 16$ the total power from the LO drivers will be about 40% of the total power of the system. Thus, there is an imminent need for optimal configuration of the LO drivers that will decrease the total power consumption while maintaining the same performance.

We consider the LO power distribution model in Fig. 4. To drive N_{rx} mixers with N_d tiles, we assume that the mixers in the same tile will share a common LO driver. To share the LO, power dividers split the input power to each amplifier

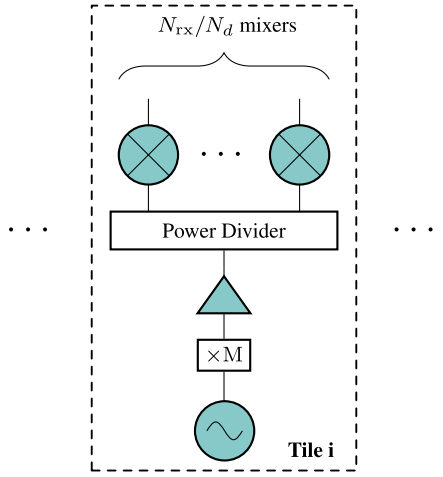

FIGURE 4. Architectural model for sharing the LO driver across multiple mixers in a tile.

driving a tile and power dividers also divide the output power to the mixer. For the divider, we consider a loss, $L_{3\text{dB}} = 0.5$ dB, while for the amplifier we assume a maximum power-added efficiency (PAE), $\eta_{\text{opt}} = 25\%$, and maximum output power, $P_{\text{opt}} = 10$ dBm, based on the designed SiGe technology. The input power of the LO signal to the power divider, $P_{\text{in}} = -5$ dBm. To find the total DC power consumption for a given number of LO drivers N_d, we can use the following set of equations,

$$P_{\text{amp}} = P_{\text{LO}}\,(N_{\text{rx}} - N_d + 1)10^{0.1\,L_{3\text{dB}}\,\log_2(N_{\text{rx}}/N_{\text{d}})}, \quad (20)$$

$$\eta_{\text{amp}} = \eta_{\text{opt}} \frac{2}{\frac{P_{\text{amp}}}{P_{\text{opt}}} + \frac{P_{\text{opt}}}{P_{\text{amp}}}}, \quad (21)$$

$$P_{\text{DC}} = N_d \left(\frac{P_{\text{amp}}}{\eta_{\text{amp}}} + P_{\text{mul}} \right), \quad (22)$$

where P_{LO} is the power required at the input of each mixer, N_{rx} is the total number of mixers, N_d is the total number of LO drivers, $L_{3\text{dB}}$ is the loss, P_{amp} is the output power of the amplifier, η_{amp} is the PAE of the amplifier, P_{opt} the output power of the amplifier that achieves peak efficiency, and P_{mul} is the power consumption of the LO generation network.

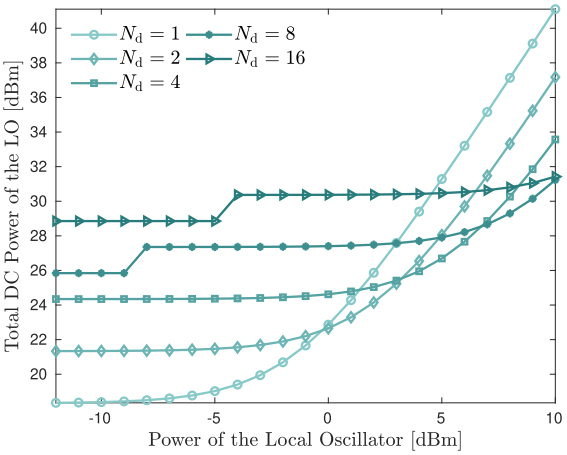

FIGURE 5. Total DC power of the LO generation and LO distribution over the LO power required by the mixer.

Using (22), we can find the optimal configuration of LO drivers based on the power required as input to the mixers. In Fig. 5, we show the total DC power consumption for each configuration of $N_{\text{rx}} = 16$ mixers and $N_d = [1, 2, 4, 8, 16]$ over the input LO power. For active mixers, the power divider provides an optimal solution since they operate efficiently with low input LO power. However, for receivers with passive mixers, the power divider will provide a sub-optimal solution since the passive mixers require a high input LO power. In [6] the $P_{\text{LO}} = 19.9$ dBm based on a design for a 140 GHz system with passive mixers.

D. ADC

The proposed receiver architecture requires one ADC pair for each of the N_{rx} antennas to sample the in-phase (I) component and quadrature-phase (Q) component. The power consumption of each ADC is given by [20],

$$P_{\text{ADC}} = \text{FOM}\, f_s\, 2^n, \tag{23}$$

where f_s is the sampling rate, n is the number of bits and FOM is the figure-of-merit of the data conversion, sometimes called the energy per conversion step.

To reduce the power consumption, we can reduce the ADC resolution with the assumption that the degradation in SNR will be compensated with beamforming. Prior simulations [12], [20]–[22] have indicated that 4 bits are sufficient for the most cellular data and data control operations. In our analysis we consider an ADC with FOM = 65 fJ/conv, based on a 4-bit flash-based ADC designed in [38]. In our analysis we consider 4-6 bits of resolution based on the performance and power results.

VI. SIMULATION AND POWER OPTIMIZATION RESULTS

A. OVERVIEW

Having developed models for all the RFFE components, we can now select the design choices to optimally trade-off the overall power and performance. We use the methodology in Section IV.

To expedite the optimization, we first evaluate the performance of the end-to-end system in a simplified *symbol-level simulation*. In the symbol-level simulation, for each design option, we pass through a sequence of symbols and look at the demodulation performance in time-domain. The channel is randomly generated and assumed to be known. The performance is then measured over an average of channel realizations and symbols. This symbol-level simulation can be performed rapidly and enables us to obtain performance numbers for all design combinations in all the RFFE components.

Once we have a characterized all the design combinations, we select a few potential designs that represent good trade-offs of performance and power. We then evaluate these smaller numbers of designs in a more detailed *New Radio link-layer simulation* using the New Radio waveform with realistic parameters for 140 GHz. Importantly, this NR link-layer simulation includes all the effects of channel estimation, phase noise and phase tracking. We verify that the performance on the NR-like waveform matches the values predicted for the symbol-level simulation.

B. SYMBOL-LEVEL SIMULATION

The details of the symbol-level simulation are as follows. We consider the SIMO system described in Section II. We generate the transmit symbols x_k that are i.i.d. complex Gaussian with zero mean and $\mathbb{E}|x_k|^2 = 1$. We consider a single path channel w with i.i.d. uniform random phase in $[0, 2\pi]$. The number of receive antennas is set to $N_{\text{rx}} = 16$ or 64 for all receivers. Then, for each design option θ we generate an RFFE using the components we discussed in Section V. Importantly, the simulation contains the models for each component extracted from the detailed circuit-level simulations and thus represents an extremely realistic characterization of the true circuit performance. In total, we explore 3900 different combinations of the RFFE components. We consider a linear receiver that uses the known channel w to perform the receive beamforming. We sweep the input SNR and measure the output SNR using (14). This generates an input-output SNR curve as shown in Fig. 6. This figure shows the input-output SNR curve for three potential design choices. The other design choices have similar shapes. To make the results more interpretable in Fig. 6, we have plotted the input power instead of the input SNR.

For each such curve, we can also fit the relation (15). We see, for example, in Fig. 6 that the model provides an excellent fit. In particular, we see the linear regime for low input SNRs and a saturation SNR at high input powers. From the model, we can then extract the two key parameters, $F(\theta)$ and $\gamma_{\text{sat}}(\theta)$, for each design choice. We also compute its power consumption $P(\theta)$.

Next, for each target effective noise figure F^{tgt} and target saturation SNR $\gamma_{\text{sat}}^{\text{tgt}}$, we compute the minimum power as shown in (18). This minimum power would represent the lowest power design choice among all the LNA, mixer, LO,

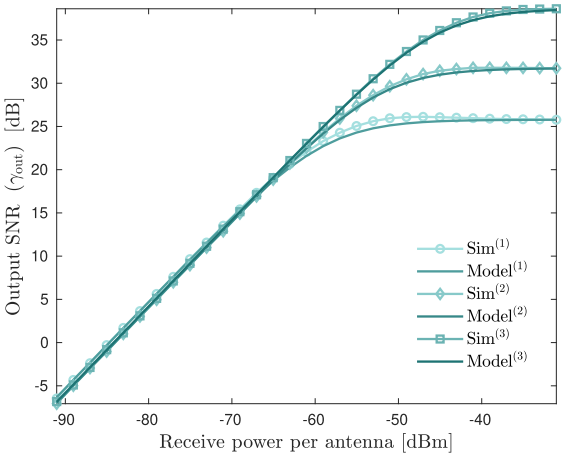

FIGURE 6. Evaluation of the approximation model for different design options θ.

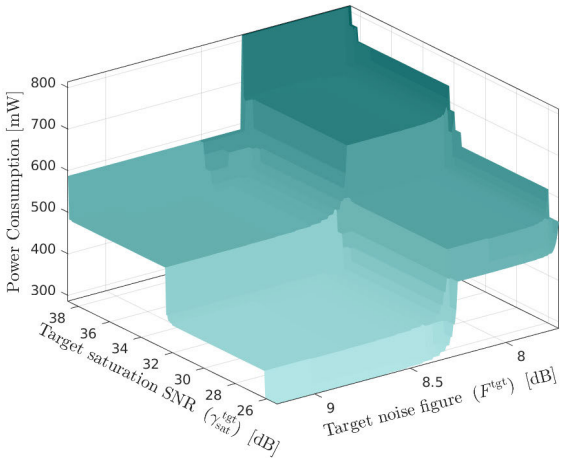

FIGURE 7. Minimum power consumption for each design choice θ based on a target noise figure F^{tgt} and a target stauration SNR $\gamma_{\text{sat}}^{\text{tgt}}$. Using this analysis we find the best design choices based on a given set of constraints.

and ADC options. Fig. 7 we report this optimal power consumption of a receiver for each pair of targets F^{tgt} and $\gamma_{\text{sat}}^{\text{tgt}}$.

C. OPTIMIZATION RESULT RESULTS

Any power value in Fig. 7 is pareto optimal in that it is the minimum power level for a given target performance metrics. But, to illustrate the savings we select two reasonable design choices that we call Design$^{(1)}$ and Design$^{(2)}$. The details of these choices and their performance are shown in Table 4.

To understand the potential benefits of the power optimization, In Table 4 compare the two optimized designs with a reference baseline fully-digital architecture described in [9]. The design in [9] used the LNA in [6] which was developed in 45 nm CMOS SOI and has a a minimum noise figure $NF = 5.2$ dB, and $FoM = 0.87$ mW^{-1}. The designs here were in 90 nm SiGe BiCMOS. To properly compare the baseline and the design here, we replace the LNA in [6] with LNA$^{(3)}$ that achieves the optimal power consumption amongst our designs. Furthermore, the baseline design considers passive mixers that introduce insertion loss (IL) and do not draw any power. For the LO generation network and LO drivers they consider the design in [6], that has $P_{\text{LO}} = 19.9$ dBm. In this system, the number of LO drivers is the same as the number of antennas. Similarly, in the analysis a 4-bit ADC with FoM = 65 fJ/conv, based on the 4-bit flash-based ADC designed in [38] with a sampling frequency $f_s = 1.6$ GHz.

To optimize the baseline design we will use (18) by setting the design parameters similarly to the baseline. To find Design$^{(1)}$ we set $F^{tgt} = 8$ dB and $\gamma_{sat}^{tgt} = 25$. For $N_{\text{rx}} = 16$ antennas the design will have effective noise $F = 7.95$ dB, saturation SNR $\gamma_{sat} = 25.64$ dB, and minimum power consumption $P = 464$ mW. For $N_{\text{rx}} = 64$ antennas the design will have effective noise $F = 7.95$ dB and saturation SNR $\gamma_{sat} = 26.11$ dB. Both designs will be comprised by LNA$^{(4)}$, Mixer$^{(5)}$, $P_{\text{LO}} = -11$ dBm, 1 LO driver and 4-bit ADCs. This system will similar performance as the baseline, and it will be about 70% more power-efficient.

Based on the simulation results and (18) we can explore more options for optimizing the power efficiency of the baseline design. For instance, we could set a lower target effective noise figure $F^{tgt} = 8.4$ dB and increase the saturation SNR $\gamma_{sat}^{tgt} = 32$. For $N_{\text{rx}} = 16$ antennas this optimization parameters will have effective noise $F = 8.37$ dB, saturation SNR $\gamma_{sat} = 32.31$ dB, and minimum power consumption $P = 358$ mW. For $N_{\text{rx}} = 64$ antennas we get effective noise $F = 8.37$ dB, saturation SNR $\gamma_{sat} = 33.56$ dB, and minimum power consumption $P = 1355$ mW. Both designs will be comprised by LNA$^{(3)}$, Mixer$^{(5)}$, $P_{\text{LO}} = -6$ dBm. For the 16-antenna design is optimal to use 1 LO driver and 4-bit ADCs, while for the 64-antenna design we need 2 LO drivers and 5-bit ADCs. This system will have much better performance for higher saturation SNR compare to the baseline, and it will be about 80% more power-efficient. Overall, we see we can match or exceed the baseline performance with dramatically lower power.

D. 3GPP NR-LIKE MULTI-CARRIER LINK-LAYER SIMULATION

As a final validation of the method, we show that the SNR analysis in the symbol level simulations applies to a full realistic link-layer simulation. We consider a downlink system with a single NR base station (gNB), and a single UE device. Although the NR standard was developed for 5G [40], the system is flexible and provides a natural baseline design for 6G systems as well. Similar to [9], we consider a mobile device at 140 GHz with carrier aggregation [41]. We assume that the UE device is equipped with an antenna array with $N_{\text{rx}} = 16$ antenna elements (i.e., 4×4 UPA). Note, as described in [10], UE devices may have multiple arrays for 360-degree coverage, but we assume here that only one such array is on at a time.

For the carrier aggregation, we let $N_{\text{CC}} = 8$ denote the number of component carriers (CCs). Each component carrier uses OFDM processing with an FFT of size $N_{\text{FFT}} = 1024$,

TABLE 4. We compare a set of optimized designs with a baseline analyzed in [9]. Provide the number of antenna elements N_{rx}, the effective noise figure F^{tgt}, and the saturation SNR γ_{sat} of designs (top). To find the model parameters we use (18) and Fig. 7. We provide the power consumption estimates in mW for the baseline and the optimized designs (bottom).

Parameter	Baseline [9]		Design$^{(1)}$		Design$^{(2)}$		Remarks
N_{rx}	16	64	16	64	16	64	Number of RX antennas. The original baseline design assumed 64 antenna elements for a UE at 140 GHz.
F [dB]	8	8	7.95		8.37		Effective noise figure of the system.
γ_{sat} [dB]	25	26	25.64	26.11	32.31	33.5	Saturation SNR

Component	Baseline [9]		Design$^{(1)}$		Design$^{(2)}$		Remarks
LNA	76.8	307.2	254.4	1017.6	76.8	307.2	Both Baseline and Design$^{(2)}$ use LNA$^{(3)}$ while Design$^{(1)}$ use LNA$^{(4)}$.
Mixer	-	-	80	320	80	320	The baseline design considers passive mixers with negligible power, while both Design$^{(1)}$ and Design$^{(2)}$ use Mixer$^{(5)}$.
LO	1568	6272	63.57	82.3	76.8	204.15	Baseline use $P_{\mathrm{LO}} = 19.9$ dBm, while Design$^{(1)}$ uses $P_{\mathrm{LO}} = -11$ dBm and Design$^{(2)}$ uses $P_{\mathrm{LO}} = -6$ dBm.
ADC	65.43	261	65.43	261	130.86	523.44	Both baseline and Design$^{(1)}$ use 4-bit ADC pairs, while Design$^{(2)}$ uses 5-bit.
Total	**1710**	**6840**	**464**	**1682**	**358**	**1355**	

TABLE 5. System parameters used in the analysis.

Parameter	Value	Remarks
Carrier frequency, f_c	140 GHz	
Number RX antennas, N_{rx}	16 or 64	
Subcarrier spacing [kHz]	240	
Number component carriers, N_{CC}	8	
Bandwidth per CC, B_{CC} [MHz]	190.08	Based on 66 occupied RBs per CC [39]
FFT size per CC, N_{FFT}	1024	
Total bandwidth, $B_{\mathrm{CC}}N_{\mathrm{CC}}$ [GHz]	1.52	
Sample rate, f_s [GHz]	1.966	Based on FFT size, SCS and N_{CC}
OFDM symbol duration, T_{sym} [μs]	4.46	Derived from SCS
Number of digital streams per CC, N_{str}	2	More streams not needed due to lack of spatial diversity

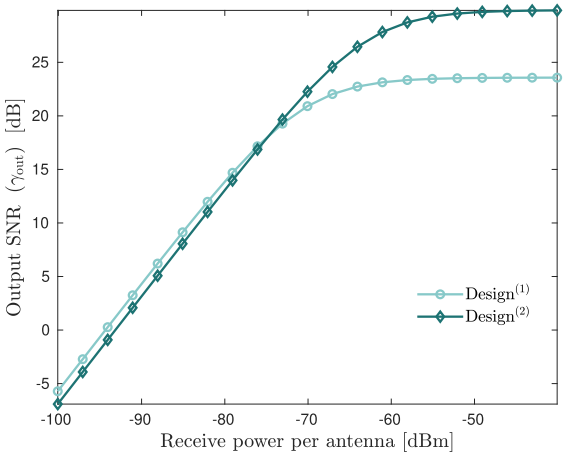

FIGURE 8. Evaluation of Design$^{(1)}$ and Design$^{(2)}$ using a 3GPP NR-like multi-carrier processing and 16 antenna elements.

and sub-carrier spacing of 240 KHz. Then, the total occupied bandwidth for each CC is $B_{\mathrm{CC}} = 190.08$ MHz. The component carriers are spaced at 200 MHz, providing a total signal bandwidth of 1.6 GHz. The sample rate of the system is derived from the FFT size, the number of component carriers and sub-carrier spacing.

The gNB is equipped with an antenna array with 64 elements (8×8 UPA), ideal RFFE, and baseband processing. The gNB can either use the entire 1.966 GHz wideband bandwidth by performing carrier aggregation, or transmit a single component carrier. We consider a single path channel between the gNB and the UE with random gain and phase. For each parameter setting, θ, we create a UE device that will process the received data at several input power levels.

The gNB generates for each component carrier a physical downlink shared channel (PDSCH) that includes the information data and some physical layer signals. The demodulation reference signals (DM-RS) and the phase tracking reference signals (PT-RS). To compensate for the common phase error (CPE), 3GPP 5G NR introduced PT-RS. In THz frequencies, the phase noise produced by the LO introduces a high degradation in the output SNR. For the PT-RS signal, we use low density in the frequency domain and a high density in the time domain. We use the algorithm provided in [42], to perform coherent estimation of the CPE.

The receiver uses DM-RS and PT-RS signals to perform practical channel estimation. For the synchronization, the receiver uses the primary synchronization signal (PSS) and the secondary synchronization signal (SSS). For each slot, we generate a random angle-of-departure (AoD) and angle-of-arrival (AoA) in both azimuth and elevation angles.

For the RFFE, we use the parameters of Design$^{(1)}$ and Design$^{(2)}$ in Table 4. The UE processes the data for each component carrier independently with ideal baseband

processing. Then, we can measure the output SNR, using (7) on the received sub-carriers. The reported output SNR is the average of all component carriers. We can then measure the average output SNR as a function of the input SNR. Our 5G NR simulations match the symbol-level simulations with a 1-2 dB difference, as shown in Fig. 8.

All the code for the simulations is provided as an open-source link-layer simulation MATLAB package [23] for evaluating 5G and 6G end-to-end communication links. Currently, the package includes models for the RF components described in Section V. Future releases will include models for RF components designed in other mmWave and THz frequencies and antenna element models. Besides the RF models, we support options for low-resolution baseband processing. Following the documentation provided in the repository, a user can replicate the simulation results.

VII. CONCLUSION

Power consumption is one of the difficult technical challenges in developing commercial mobile devices above 100 GHz. To address this issue, we have developed a general methodology for understanding the end-to-end system performance. The key metric is what we call the output SNR, that incorporates the non-linearities and noise in the receiver chain and can be rigorously tied to the achievable capacity. We have considered detailed circuit design options for each of the components in the receiver chain and jointly optimized them to meet the output SNR targets. The key insight is that since most commercial wireless systems, particularly cellular systems, do not require high output SNRs, the power consumption of the components can be dramatically reduced. In addition to low resolution ADCs that have been explored considerably, our analysis shows that the mixer power consumption – which is actually the dominant component in cellular systems – can be significantly reduced. Overall, the circuit and systems simulations show that, with appropriate optimizations, we are able to achieve a remarkable 70 to 80% reduction in power consumption. These savings are dramatic and can open new use cases for communications above 100 GHz.

There are also several interesting areas that the methodology can be applied to. This work has focused on cellular UEs at 140 GHz. These would operate in licensed bands, where we expect bandwidths will be relatively small, approximately 2 GHz at maximum. The analysis could also be applied to systems with wider bandwidths and also at higher frequencies. Also, to support mobility, we have considered fully digital architectures. But, phase array systems can also be considered.

APPENDIX A
PROOF OF (8)

From [27, Lemma 2], we have

$$C > f_s \log\left(\frac{1}{1-\rho}\right), \tag{24}$$

where ρ is the correlation coefficient between the transmitted signal X and its linear minimum mean squared estimate based on the observation Z which is

$$\rho = \frac{|\mathbb{E}(X^*Z)|^2}{\mathbb{E}|Z|^2\mathbb{E}|X|^2}. \tag{25}$$

Now from (6), we have that

$$\begin{aligned}\tau &= \mathbb{E}|Z|^2 - 2A^*\mathbb{E}(X^*Z) + |A|^2\mathbb{E}|X|^2 \\ &= \mathbb{E}|Z|^2 - \frac{|\mathbb{E}(X^*Z)|^2}{\mathbb{E}|X|^2}.\end{aligned} \tag{26}$$

Applying (25) and (26), we obtain

$$\begin{aligned}\frac{1}{1-\rho} &= 1 + \frac{1}{1-\rho} \\ &= 1 + \frac{|\mathbb{E}(X^*Z)|^2}{\mathbb{E}|Z|^2\mathbb{E}|X|^2 - |\mathbb{E}(X^*Z)|^2} \\ &= 1 + \frac{|A|^2\mathbb{E}|X|^2}{\tau} = 1 + \gamma_{\text{out}}.\end{aligned} \tag{27}$$

Substituting this in (24) concludes the result.

APPENDIX B
PROOF OF (9)

The result is a special case of the theory in [27], which provides a lower bound on the capacity when signaling on sub-bands. Specifically, consider the case of dividing the spectrum into two sub-bands with bandwidth α and $1-\alpha$. Let $\overline{P} = \mathbb{E}|X|^2$ be the average received symbol energy in time-domain. By allocating all the transmit power to sub-band 1, we can receive $P_1 = \overline{P}/\alpha$ signal energy per symbol in sub-band 1 and $P_2 = 0$ signal energy in sub-band 2. Based on [27, Theorem 2] (with appropriate change of notation to match the case here), we have that the capacity is lower bounded by

$$\begin{aligned}C &\geq \alpha f_s \log\left(1 + \frac{|A|^2P_1}{\tau}\right) + (1-\alpha) f_s \log\left(1 + \frac{|A|^2P_2}{\tau}\right). \\ &= \alpha f_s \log\left(1 + \frac{|A|^2\mathbb{E}|X|^2}{\alpha\tau}\right) \\ &= \alpha f_s \log\left(1 + \frac{\gamma_{\text{out}}}{\alpha}\right).\end{aligned} \tag{28}$$

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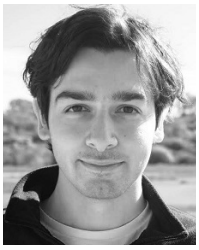

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