A compact H-band Power Amplifier with High Output Power

Ahmed S. H. Ahmed[+#1], Utku Soylu[#], Munkyo Seo[*], Miguel Urteaga[$], and Mark J. W. Rodwell[#]
[+]Marki Microwave Inc., 215 Vineyard Court, Morgan Hill, CA 95037
[#]Department of Electrical and Computer Engineering, University of California, Santa Barbara, USA
[*]Department of Electrical and Computer Engineering, Sungkyunkwan University, South Korea
[$]Teledyne Scientific Company, Thousand Oaks, CA 91360, USA
[1]a_s_ahmed@ucsb.edu

***Abstract*— We report a compact H-band power amplifier with high output power in 250nm InP HBT technology. Stacking and parallel power combining together provide the desired output power. Common-base stages with base capacitive degeneration act as stacked power cells. Four power cells are combined by a compact low-loss 4:1 transmission line network. At 270GHz, the four-stage amplifier has 16.8dBm saturated output power with 4% power-added efficiency (PAE). Over 266-285GHz, the amplifier's saturated output power is 14-16.7dBm with an associated 2.2-4%PAE. The 3-dB small-signal bandwidth extends from 233GHz to 281GHz with a peak gain of 20.5dB at 264GHz. The amplifier has a compact area of 1.08mmx0.77mm and P_{sat}/mm^2 of 57.6mW/mm^2. To the authors' knowledge, these results demonstrate a record output power and P_{sat}/mm^2 for H-band amplifiers working around 270GHz.**

***Keywords*— H-band, millimeter wave, high-efficiency, stacking, parallel combining, compact combiner, 250-nm InP.**

I. Introduction

Millimeter-wave communications permit high data rates due to the available wide spectrum. Power amplifiers are key components in the transmitter since they dominate the efficiency and limit the communication range. CMOS shows only -3.9dBm at 260GHz [1]. Advanced technologies with high power gain cut-off frequency (f_{max}) are necessary to generate moderate power at H-band frequencies [2]-[11].

Here we report a compact and high output power H-band power amplifier. The four-stage amplifier uses stacking and parallel power combining techniques. The key design features are 1) a compact and low loss 4:1 power combiner, 2) common base stages with base capacitive degeneration, and 3) driver scaling. The compact amplifier shows a broadband operation with a 48GHz small-signal bandwidth (BW) and 14-16.7dBm saturated output power from 266GHz to 281GHz.

II. Amplifier Design

A. Amplifier Block Diagram

The amplifier is fabricated in Teledyne 250nm InP HBT technology [12]. The amplifier (Fig. 1b) delivers the desired output power by series and parallel power combining. The common-base (CB) stages have significant RF voltage swings on the base nodes, hence design is similar to series-connected cells. Four power cells (Stage4 96-µm HBT periphery) are parallel-combined by a low-loss compact power combiner.

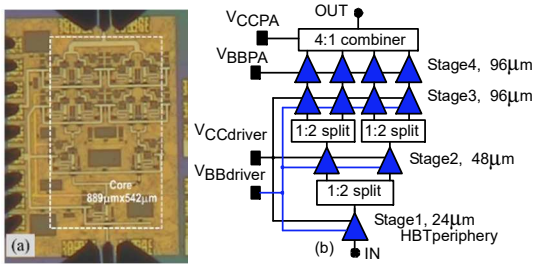

Fig. 1. (a) die photo, area including DC routing and pads is 1.08mmx0.77mm. Core area, without DC routing or pads, is 0.89mmx0.54mm and (b) amplifier block diagram.

The required gain is achieved by cascading four stages. Conservative driver scaling, (Stage1 24-µm), (Stage2 48-µm), (Stage3 96-µm) HBT periphery, ensures proper amplifier saturation.

B. Unit Cell for Driver and Power Cells

We evaluated a common emitter (CE) (Fig. 2a), a grounded CB (Fig. 2b), and a capacitive base degeneration (Fig. 2c), i.e. with significant capacitive reactance presented to the base. The maximum base capacitance value is limited by the self-resonance frequency (SRF) due to the parasitic inductance associated with the capacitor while the minimum base capacitance is limited by the minimum acceptable gain. Lossless schematic large-signal simulations are performed for the same transistor size of (4·0.25µm·6µm) with the load impedance tuned for max PAE, and under the same bias conditions (1.8mA/µm and V_{CE}=2.2V). Though all topologies have the same peak PAE (Fig. 2d), CE shows 13.1dBm of OP_{1dB} with 13.6% PAE and 4.9dB associated gain while grounded CB shows 9.6dBm of OP_{1dB} with 8.4% PAE and 10.8dB associated gain. The CB with 208fF base capacitance shows OP_{1dB}=13.7dBm with 16%PAE and 5.6dB associated gain. These results show that CB with finite base capacitance shows superior output power and PAE at 1dB gain compression which is consistent with the study in [13].

Fig. 3 shows the schematic diagram, used in drivers and power cells, of the capacitively degenerated CB stages with the matching and biasing elements. The base capacitance is implemented using MIM capacitors and symmetrically connected with a minimum parasitic inductance to the four-finger transistor (4·0.25µm·6µm). The simulated impedance presented to the base is -j2.8Ω at 270GHz.

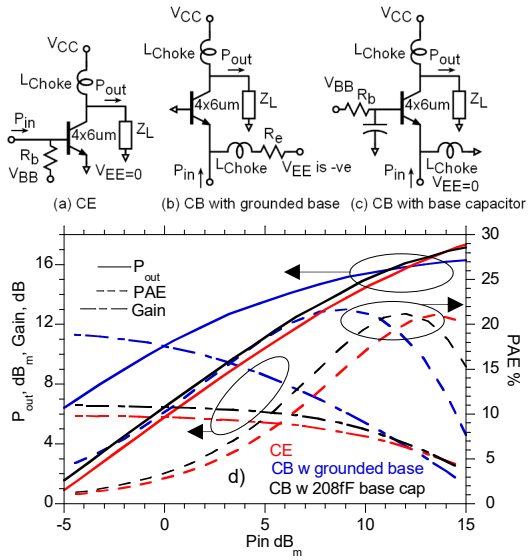

Fig. 2. Schematic diagram of: (a) CE (b) CB with grounded base; (c) CB with 208fF base capacitor; (d) P_{out}, gain, and PAE for CE, grounded CB, and CB with a base capacitor at 270GHz.

It is difficult to accurately simulate the base inductance in multifinger mm-wave transistors. If the operating frequency approaches the capacitor SRF, the stage gain becomes sensitive to small modeling errors in the base inductance; further, strong gain peaking or even instability can arise. In the capacitively degenerated CB stage, the base capacitor has small dimensions hence has small parasitic inductance and a ~400GHz simulated SRF, well above the operating frequency.

The cell can be viewed as a stacked power cell [16], [17] since there is a significant AC voltage swing on the base capacitance. With proper load tuning, the total output voltage swing exceeds that at the transistor collector-base junction. As in a stacked stage, the delivered output power is greater than that of a grounded-base CB stage having the same load impedance, with the additional output power being contributed by the driver stage.

The transistor parasitic capacitance is tuned by shunt inductive transmission lines terminated by bypass capacitors. Interconnects are microstrip lines with the signals routed on the top metal layer (Met4) and the ground plane on Met1. This provides lower losses than inverted lines (signals on Met 1, Met4 ground plane), but the necessary ground plane openings at transistor locations reduce EM modeling accuracy. After shunt inductive tuning, for maximum PAE the required load impedance for each power cell is ~35Ω. The transistor input is matched to ~50Ω.

Given uncertainties in modeling stage gains at 270GHz, the drivers are conservatively scaled to ensure that the output stages can be driven into compression. The gain cells (Fig. 1b) are all identical, but while each cell in stages 1 and 2 drives two cells, each cell in stage 3 drives only one cell. To be compact, the splitters between stages 2 and 3 are implemented by series transmission line sections and distributed capacitors, while that between stages 1 and 2, with larger available space, uses $\lambda/4$ sections.

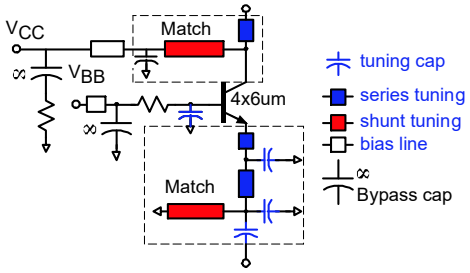

Fig. 3. Schematic diagram of the unit cell

Separate supply lines (V_{CC} and V_{BB}) for the stage 4 and the remaining stages. With 140GHz designs of similar topology [13], radio-frequency oscillations have been observed if the supply is not adequately externally bypassed. Radio-frequency oscillations have been observed if the supply is not adequately externally bypassed. Addressing this, the present IC has many on-wafer supply bypass capacitors, all with series resistors to damp *LC* resonances. With this IC, no evidence of supply-induced oscillation has been observed. All passive elements, multi-finger transistors, and matching networks are simulated by Ansys HFSS, 3-D EM simulation, and compared to ADS momentum. The presented simulations use HFSS.

C. *Proposed 4:1 Power Combiner*

The desired output power is achieved by combining four power cells (schematic in Fig. 4a and chip micrograph in Fig. 4b). Each cell requires 35Ω load impedance. 50Ω transmission line sections with negligible electrical lengths combine two cells. Therefore, the required load impedance for the pair is 17.5Ω. The load impedance is 50Ω and by symmetry, it could be split into two parallel 100Ω resistors. A quarter-wave transmission line section with 29.5Ω characteristic impedance transforms the 100Ω load impedance (for half circuit) into the required 17.5Ω. The combiner (Fig. 4) has ~0.6dB simulated loss. Because signals pass through a single $\lambda/4$ section of 29.5Ω characteristic impedance, the combiner is compact and low loss, while the low-Z_o lines are wide hence can carry large DC and RF currents. The drawback of this combiner is smaller bandwidth than a 4:1 Wilkinson, because the impedance transformation occurs at a single step. Further details of similar transmission line combiners could be found in [13]-[15]

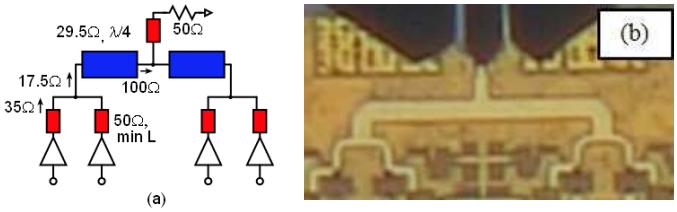

Fig. 4. proposed 4:1 power combiner: (a) schematic and (b) die photo.

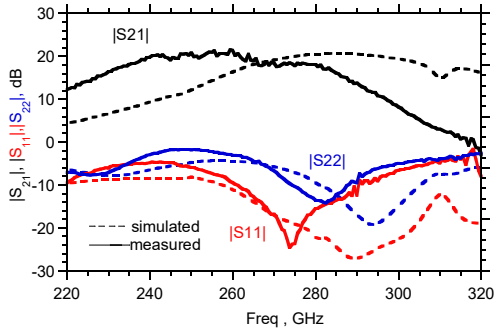

Fig. 5. Measured (solid) and simulated (dashed) S-parameters.

III. Measurement Results

The measurement is performed on the 3-mil thinned die without heatsink (Fig. 1a). S-parameters are measured using a Keysight network analyzer with 220-325GHz Oleson frequency extender modules and 325GHz GGB wafer probes. There are several calibration standards [18]. Given that the required precision in circuit measurements is relaxed compared to device modeling, a short-open-load-thru (SOLT) calibration standard is arbitrarily used. SOLT standard calibration on an external substrate moves the reference plane to the probe tips. Despite extensive EM simulations during design, a ~20GHz frequency shift is observed between the amplifier's measured and simulated S-parameters (Fig. 5) biased at (V_{CCPA}=2.2V, V_{BBPA}=2.3V, I_{CCPA}=172mA, I_{BBPA}=9.4mA, $V_{CCdriver}$=2.5V, $V_{BBdriver}$=2.1V, $I_{CCdriver}$=275.5mA, and $I_{BBdriver}$=14.8mA). The peak measured small-signal gain ($|S_{21}|$) is 20.5dB at 264GHz and it is in good agreement with simulation. The measured 3dB-BW is 48GHz. The input reflection coefficient ($|S_{11}|$) is better than -10dB from 261GHz to 291GHz. Though the output network is tuned for maximum saturated power, the output reflection coefficient ($|S_{22}|$) is better than -5dB from 266GHz up to 320GHz.

In large-signal measurements, a 110-170GHz VDI extender drives a 270-290GHz AMC doubler from Virginia diodes. The doubler is followed by an H-band coupler. The coupled port goes to an H-band harmonic mixer and spectrum analyzer. The through port goes to the Erickson power meter in the calibration phase (Fig. 6a) and a 325GHz-GGB probe followed by the amplifier in the measurement phase (Fig. 6b).

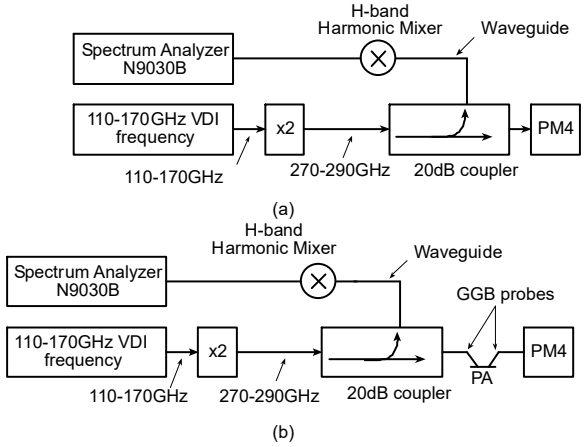

Fig. 6. Power measurement setup: a) calibration phase; b) measuring phase.

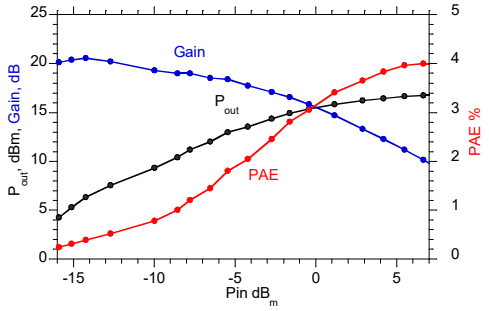

Fig. 7. Measured output power, PAE, and gain versus input power at 270GHz.

The spectrum analyzer reading represents the output power from the coupler's through port by applying the appropriate correction factor at each frequency. The correction factors are the power difference, in dB, between the spectrum analyzer readings and the PM4 in the calibration phase (Fig. 6a). The power is swept by adjusting the drive power to the 110-170GHz VDI extender.

The amplifier is biased by DC probes with bypass capacitors at (V_{CCPA}=2.2V, V_{BBPA}=2.5V, I_{CCPA}=173.3mA, I_{BBPA}=10.8mA, $V_{CCdriver}$=2.4V, $V_{BBdriver}$=2.2V, $I_{CCdriver}$= 274.8 mA, and $I_{BBdriver}$=16.2mA). The last stage's output voltage is coupled to the RF output, so the on-wafer voltage can be monitored through the probe's bias T. At 270GHz frequency (Fig. 7), the amplifier has 16.8dBm, after calibrating the probe losses, saturated output power with 4% PAE and 10.2dB associated gain. We expect that the power could further increase with proper heatsinking. The amplifier demonstrates wideband operation. Fig. 8 shows the output power at different frequencies. Over 266GHz-285GHz, the output power is 14-16.8dBm with 2.2-4% PAE and 9.6-10.9dB associated gain (Fig. 9).

IV. Conclusion

The paper presented a record PAE and output power at the H-band frequency range. Over 266-285GHz, the amplifier demonstrates 14-16.8dBm saturated output with 2.2-4%PAE. The amplifier used stacking and parallel power combining techniques to achieve the desired power. The amplifier could be integrated into mm-wave transmitters or high-power signal sources. Table 1 shows the state-of-the-art high-efficiency H-band amplifiers. The present work demonstrates record power and P_{sat}/mm^2 with reasonable PAE at 270GHz.

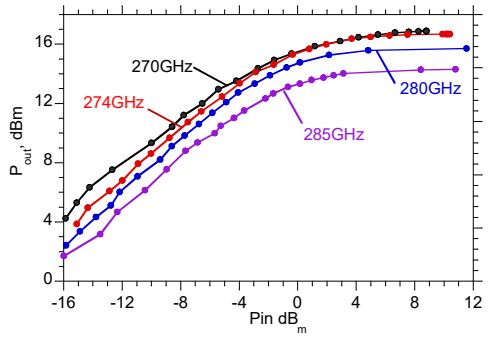

Fig. 8. Measured output power versus input power at various frequencies.

Table 1. State-of-the-art H-band amplifiers.

Ref	[5]	[7]	[8]	[2][a]	[10] [a]	[9]	[4]	[6]	[11]	[3]	This work
Freq, GHz	240	185-255 265	325	275-320	338	300-305	300	290-307.5	301	280-328	**266-285**
P_{sat}, dBm	>10.8	20-23.9 17.2	11.3	2.7-4.8	10	9.5-9.8	8	7.8-10	13.5	9.6-13.7	**14-16.8**
Gain at P_{sat} (dB)	15	12.2-17 11.7	9.4	13.5-15	3.3	7.5-7.8	11	10-12	11.8	11.5-13.8	**9.6-10.9**
PAE at P_{sat}%	5	4.1 0.95	1.1	2.3[d]	1.8	1.1	2.97	1.1	1.5	0.8-2.4	**2.2-4**
BW_{3dB}, GHz	55	53[c]	9	~100[c]	10	40	57	21	15[c]	48[c]	**48**
Chip Size (mmxmm)	1.5x0.75	2.14x1.58	0.98x1	0.5x1.35	2x0.75	0.55x0.55[b]	2x0.75	1.45x0.44	0.67x0.68	0.6x1.3[b]	**1.08x0.77**
P_{DC} (W)	-	5.24	1.12	0.129[d]	0.29	0.72	0.2	0.85	1.49	-	**1.09**
P_{sat}/Area mW/mm^2	10.6	72.5 15.7	13.9	4.5	6.66	31.6	4.2	15.7	22.3	30	**57.6**
Technology	35 nm GaAs mHEMT	250-nm InP HBT	130-nm InP HBT	35 nm InAlAs/InGaAs	50 nm InP HEMT	250-nm InP HBT	35 nm InGaAs mHEMT	250-nm InP HBT	250-nm InP HBT	35 nm InGaAs mHEMT	**250-nm InP HBT**

[a] module results, [b]total area is obtained by scaling the given photo, [c] graphically estimated, [d]calculated

ACKNOWLEDGMENT

This work was supported in part by the Semiconductor Research Corporation and DARPA under the JUMP program. The authors thank Teledyne Scientific & Imaging for the IC fabrication.

REFERENCES

[1] O. Momeni, "A 260GHz amplifier with 9.2dB gain and −3.9dBm saturated power in 65nm CMOS," 2013 IEEE ISSCC Digest of Technical Papers, San Francisco, CA, 2013, pp. 140-141.

[2] A. Tessmann et al., "A broadband 220–320 GHz medium power amplifier module," in Proc. IEEE Comp. Semicond. Integr. Symp., La Jolla, CA, USA, Dec. 2014, pp. 1–4.

[3] L. John et al., "Broadband 300-GHz Power Amplifier MMICs in InGaAs mHEMT Technology," in IEEE Transactions on Terahertz Science and Technology, vol. 10, no. 3, pp. 309-320, May 2020.

[4] B. Schoch, A. Tessmann, A. Leuther, S. Wagner and I. Kallfass, "300 GHz broadband power amplifier with 508 GHz gain-bandwidth product and 8 dBm output power," 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2019, pp. 1249-1252

[5] A. B. Amado-Rey et al., "Analysis and Development of Submillimeter-Wave Stacked-FET Power Amplifier MMICs in 35-nm mHEMT Technology," in IEEE Transactions on Terahertz Science and Technology, vol. 8, no. 3, pp. 357-364, May 2018

[6] Z. Griffith, M. Urteaga, P. Rowell and R. Pierson, "A 6–10 mW Power Amplifier at 290–307.5 GHz in 250 nm InP HBT," in IEEE MWCL, vol. 25, no. 9, pp. 597-599, Sept. 2015.

[7] Z. Griffith, M. Urteaga and P. Rowell, "180–265 GHz, 17–24 dBm output power broadband, high-gain power amplifiers in InP HBT," 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, HI, 2017, pp. 973-976.

[8] A. S. H. Ahmed, A. Simsek, M. Urteaga and M. J. W. Rodwell, "8.6-13.6 mW Series-Connected Power Amplifiers Designed at 325 GHz Using 130 nm InP HBT Technology," 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), San Diego, CA, 2018, pp. 164-167

[9] H. G. Yu, S. H. Choi, S. Jeon, and M. Kim, "300 GHz InP HBT amplifier with 10 mW output power," Electron. Lett., vol. 50, no. 5, pp. 377–379.

[10] V. Radisic et al., "A 10-mW Submillimeter-Wave Solid-State Power-Amplifier Module," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 7, pp. 1903-1909, July 2010

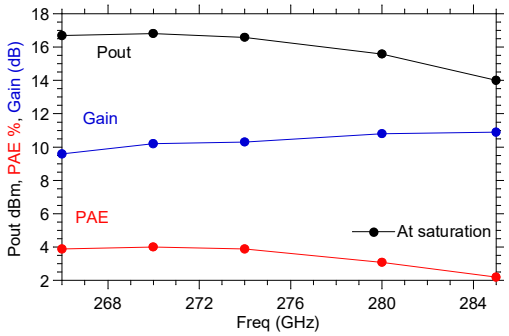

Fig. 9. Measured output power with the associated PAE and compressed gain vs. frequency reported at the peak PAE.

[11] J. Kim, S. Jeon, M. Kim, M. Urteaga and J. Jeong, "H-Band Power Amplifier Integrated Circuits Using 250-nm InP HBT Technology," in IEEE Transactions on Terahertz Science and Technology, vol. 5, no. 2, pp. 215-222, March 2015.

[12] M. Urteaga, et al., "InP HBT Technologies for THz Integrated Circuits", *Proc. of the IEEE*, vol. 105, no. 6, pp 1051-1067, June 2017.

[13] A. S. H. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter and M. J. W. Rodwell, "A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 492-495.

[14] A. S. H. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter and M. J. W. Rodwell, "A 200mW D-band Power Amplifier with 17.8% PAE in 250-nm InP HBT Technology," 2020 15th European Microwave Integrated Circuits Conference (EuMIC), Utrecht, Netherlands, 2021, pp. 1-4.

[15] A. S. H. Ahmed, U. Soylu, M. Seo, M. Urteaga, J. F. Buckwalter and M. J. W. Rodwell., " A 190-210GHz Power Amplifier with 17.7-18.5dBm Output Power and 6.9-8.5% PAE.," in press, Proc. IMS2021.

[16] A. S. H. Ahmed, et al., "204GHz Stacked-Power Amplifiers Designed by a Novel Two-Port Technique," 2018 13th European Microwave Integrated Circuits Conference (EuMIC), Madrid, 2018, pp. 29-32.

[17] H. Dabag, et al., "Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 4, pp. 1543-1556, April 2013

[18] A. Davidson, E. Strid and K. Jones, "Achieving greater on-wafer S-parameter accuracy with the LRM calibration technique," 34th ARFTG Conference Digest, Ft. Lauderdale, FL, USA, 1989, pp. 61-66.