Transistors for 100-300GHz Wireless

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***Abstract*—We examine the potential design and performance of 100-300 GHz wireless communications systems, examine the required transistors performance, and describe our present efforts to develop InP bipolar and field-effect transistors to serve in the transmitters and receivers of such systems .**

Keywords—mm-wave wireless, 6G wireless, InP HBTs, InP HEMTs, InP MOS-HEMTs, mm-wave ICs, THz wireless.

I. Introduction

Communication by radio is growing rapidly worldwide, exhausting the allocated 4G radio spectrum. In response, industry is introducing 5G wireless systems, these using carriers at sub-6, 28, 38, 57-71(WiGig), and 71-86GHz, though most deployments are still at the lower frequencies. Longer-range research now explores next-generation systems, these potentially using 100-300GHz carrier frequencies. For these, the large potential channel bandwidth permits very high data rates per signal beam, while the short wavelengths permit the use of compact multi-beam (MIMO) phased arrays supporting many simultaneous independent signal beams, each carrying independent information. Such massive spatial multiplexing can further greatly increase the transmission capacity of short-range wireless hubs and backhaul communications links. Aggregate capacities can approach or even exceed 1Tb/s. Here we will consider the transistors and integrated circuits required for such systems.

II. 100-300GHz Wireless Systems

Consider two application examples [1, 2]: a wireless communications hub (base station) serving many mobile users, and a spatially multiplexed point-point backhaul link, connecting such hubs to the internet.

Figure 1 shows a 140GHz spatially multiplexed hub, supporting 16 users per array face. Each array has 32 antennas, but is only 41mm long. If we assume that the hub's power amplifiers each provide 125mW at the 1dB gain compression point, that the handset has a 1cm^2 array (8×8 at $\lambda/2$ spacing) and has 8dB noise figure, that it is raining 50mm/hr., and that the signaling is QPSK modulation at 10^{-3} uncoded error rate, then the hub can provide each user with 10Gb/s data rate at 40m range, even with 17dB total safety margins for partial beam blockage, equipment aging, and manufacturing variations. The net transmission capacity is 160Gb/s per array face. A longer 256-element array having otherwise the same parameters could provide 10Gb/s per user to 128 users over 100m range; the net capacity is then 1.3Tb/s.

Figure 2 shows a spatially multiplexed backhaul link. N transmitters, carrying independent data, form an array of length L. The receiver, at distance R, has a similar array but uses MIMO [3] beamforming. If the array angular resolution λ/L is smaller than the element apparent angular separation L/NR, then the signals can recovered without channel-channel crosstalk degrading the SNR. Link capacity is increased N:1.

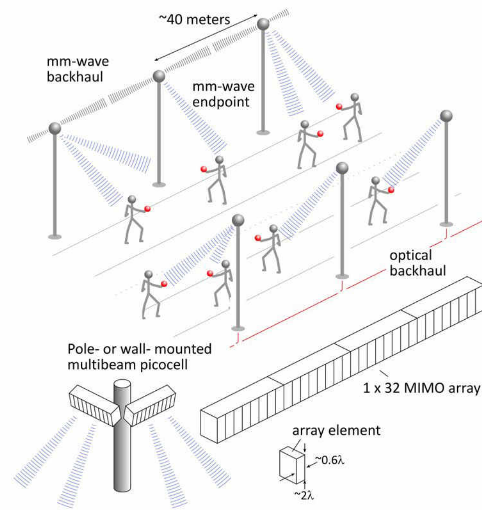

Figure 1: Spatially multiplexed network 140GHz picocell hub. The hub has 2 faces, each a 32-element MIMO array, each providing up to 16 independent signal beams. At 40m range, 10Gb/s transmission per beam is feasible with large operating margins.

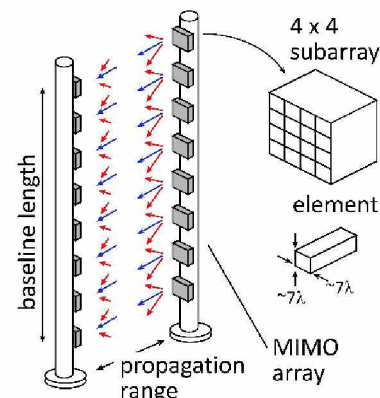

Figure 2: Spatially multiplexed wireless backhaul link, using linear transmitter and receiver arrays, with each element being a 4×4 subarray

Short wavelengths are of great advantage, as a short array can then carry many channels; at 500m range, an 8-element array must be 2.1m long at 210GHz, 2.6m at 140GHz, and 3.5m at 75GHz. At 210GHz, if each array element is an 8×8

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subarray of 7λ by 7λ elements (for small beam angle adjustment) then, with 20 dB total margins, QPSK at 10^{-3} uncoded error rate, and 6dB receiver noise figure, transmitting 640Gb/s over 500m range in 50mm/hr. rain requires only 63 mW/element output power at the 1dB gain compression point.

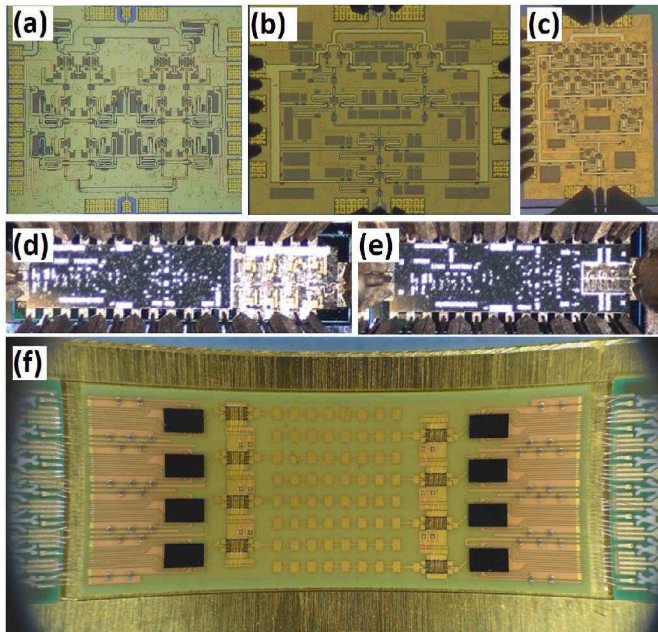

Figure 3: Representative 100-300GHz ICs, including power amplifiers at (a) 131GHz with 200mW power and 17.8% PAE, (b) 194GHz with 55mW power and 8.5% PAE, and (c) 266GHz with 48mW power and 4% PAE, (d) a 200GHz transmitter with 34mW output power, (e) a 200GHz receiver with 7.7-9.3dB noise figure, and an as-yet-untested prototype of a 140GHz 8-channel MIMO transmitter, with CMOS frequency conversion ICs and InP power amplifiers, designed for the system of figure 1.

III. High-Frequency Transistor & IC Technologies

These and similar systems will drive high-frequency transistor development. The baseband beamforming, which recent work [4,5] suggests might be feasible by digital processing, is performed in a central module by CMOS VLSI. The RF front end ICs are mounted at regular spacings within the array; these convert the low-frequency information streams to the carrier frequency, and will use come combination of CMOS, SiGe, and III-V (InP, GaAs and GaN) technologies.

CMOS works well at 140-150GHz, providing low receiver noise and moderate output power [6,7], but receiver noise and power amplifier output power and efficiency degrade sharply at higher frequencies [8]. Best CMOS performance at 100-200GHz is reported for the 65nm through 32nm nodes, not for more highly scaled technologies. Longer-range ~150GHz wireless links can use CMOS with external III-V or SiGe power amplifiers for increased output power, and can also use InP HEMT or GaAs PHEMT or MHEMT low-noise amplifiers for better receiver sensitivity. For systems having >200GHz carrier frequencies, though CMOS can still be used for frequency conversion [9,10], for best IC performance, and to reduce the number of high-frequency IC-IC connections, it is attractive to build the entire RF front end from III-V or SiGe technologies. Figure 3 shows some representative ICs [11, 12, 13, 14]

Because scaling CMOS VLSI below 32nm has not improved its performance in 100-300GHz wireless systems, progress in high-frequency wireless systems requires development of *application specific mm-wave IC technologies,* including SiGe HBT [15], GaN HEMT [16, 17], GaAs/InGaAs PHEMT [18], InP HBT [19,20], InP HEMT [21] and mm-wave optimized CMOS [22,23]. We will focus below on our own work, InP HBTs and MOS-HEMTs. Before doing so, we first consider performance objectives in developing a high-frequency IC technology.

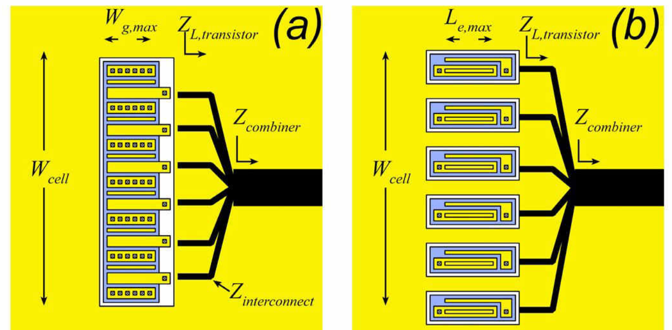

Figure 4: Impedance and current limits to power in mm-wave amplifiers. (a) Multi-finger FET and (b) multi-finger HBT power transistor cell layouts. Shifts in the impedance presented to the transistor limit the maximum cell width, while gate and base metal resistance limit the FET gate width W_g and the emitter finger length L_e.

IV. Transistor and IC Technology Requirements

While f_{max}, the transistor power-gain cutoff frequency, is the maximum usable frequency, and while Singhakowinta [24] derived the maximum gain obtainable in an unconditionally stable amplifier, practical amplifiers are rarely designed for maximum gain. Instead, receivers are designed for minimum cascaded noise figure, while transmitters are designed for maximum output power and maximum power-added efficiency (PAE). Regardless of circuit configuration, the cascaded noise figure of an amplifier cannot be less [25] than (M+1), where M is the transistor minimum noise measure. We can similarly show [26] that, if the load impedance is kept constant, the relationship between added power (P_{out}-P_{in}) and power-added efficiency (PAE) of a transistor does not change if it is embedded into an arbitrary lossless circuit. Though more difficult to measure than cutoff frequencies, the variation with frequency of noise measure, M, for transistors used in low-noise amplifiers, and peak PAE and added power density (in W/mm), for transistors used in power amplifiers, are therefore key transistor figures of merit.

The Johnson (voltage) figure-of-merit is not the only limit to output power; there is also a current limit. Transistors have some maximum output current per finger length (gate width or emitter length), and long fingers have low f_{max} from high metal resistance. There is therefore a maximum current per finger. In a power transistor cell, fingers are tied in parallel (Figure 4) to further increase the current, but there is a maximum number of fingers so connected: because the finger-finger interconnects

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are not controlled-impedance (specifically, are not terminated in their characteristic impedance), they must be kept much shorter than a wavelength to maintain uniform and controlled load impedances for all fingers. The power transistor cell therefore has some maximum output current I_{max}. Given some maximum realizable impedance $Z_{combiner}$, c.a. 75Ω, presented by the power-combining network to the power transistor cell, there is a maximum voltage swing $I_{max}Z_{combiner}$. In some cases, this can be considerably less than the transistor breakdown voltage. This current limit sets the maximum output power per multi-finger transistor to $I^2_{max}Z_{combiner}/8$. We can show that this power limit varies as f^{-3}. This limit is particularly important at very high frequencies, when the transistor breakdown voltage is large or its output current density (mA/μm) is low, or if the transistor minimum finger pitch is large.

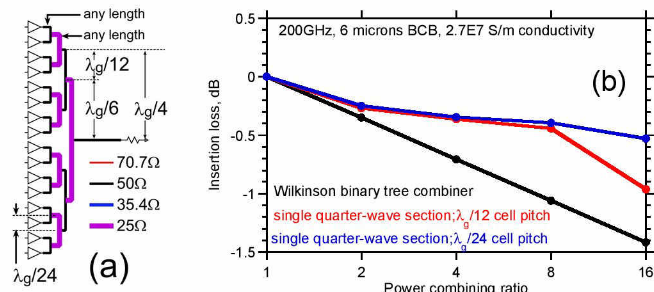

Figure 5: Dependence of power-combining losses on power transistor cell size. (a) Compact 16:1 combiner that acts effectively as a single λ/4 line, minimizing losses. (b) Simulated combining losses for a Wilkinson binary tree, for the combiner shown in the figure, and for a combiners with a larger transistor cell size that forces longer interconnect lines hence greater losses. λ_g is the guide wavelength.

Another limit to power is the loss of combining, on-wafer, the output power of many such power transistor cells. The smaller such losses, the larger the feasible output power and PAE for a given IC technology. A 2^N:1 combiner (Figure 5a) can be synthesized from a single λ/4 line section. With such small total length, the insertion loss (Figure 5b) increases only slowly with combining ratio, but only if the 2^N power cells can fit within the available width, slightly larger than $\lambda_g/2$. Beyond this N, combining losses then increase rapidly. Again, greater output power, at higher efficiency, is obtained if the transistor fingers can be tightly packed.

Although we focused above on power amplifiers, dense layouts are important in other 100-300GHz RF-front-end circuits. The MIMO systems of Figure 1 and Figure 2 can require as many as 128-256 separate RF front-ends. For manageable cost, the IC area per RF channel should be low. In 2D monolithic phased arrays [6], the IC area for each RF channel must be less than $(\lambda/2)^2$; extremely dense circuits are then imperative. 100-300GHz ICs can be made more dense by selecting the smallest feasible passive elements and by providing multiple controlled-impedance, low-loss signal planes within the wiring stack. The RF front-end can be made more compact by using IC technologies [27] with very high transistor cutoff frequencies, as higher stage gain implies fewer needed stages, and because, with higher transistor gain, fewer stage-stage interfaces require impedance-matching

V. InP Bipolar Transistors

InP HBTs have high cutoff frequencies, moderate breakdown voltages, can support moderate integration scales, and thus are useful for 100-650GHz RF front-ends and power amplifiers. When lowest noise is imperative, an InP HBT receiver might be paired with an InP HEMT low-noise amplifier.

to double the bandwidth:	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm²)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

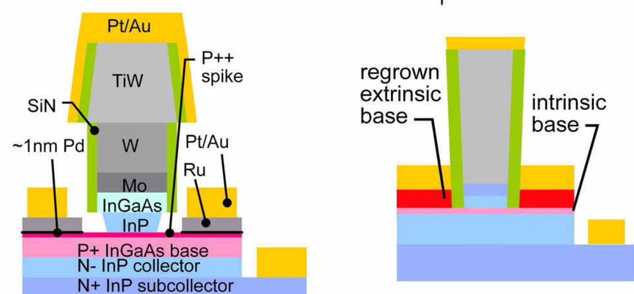

Figure 6: HBT scaling laws (top), scaled mesa HBT (bottom left) and HBT with regrown extrinsic base (bottom right).

HBT design is straightforward (Figure 6). Each 2:1 increase in cutoff frequencies (f_τ, f_{max}) requires a 2:1 thinner collector, a base between 2:1 and $2^{1/2}$:1 thinner, 4:1 narrower emitter-base and base-collector junctions, 4:1 smaller emitter and base specific contract resistivities, and 4:1 greater current density [19]. Base metal resistance can also significantly reduces f_{max} [28].

The key challenges are making narrow emitter junctions and low resistivity contacts [29]. InP HBTs with performance close to the scaling roadmap [19] have been realized through the 128nm node, with 1.1THz f_{max} demonstrated [20]. Many ICs, from 50-650GHz, have been demonstrated using the 128nm and 256nm nodes.

Though the necessary low emitter and base contact resistivities have been demonstrated in test structures [29], it is difficult to obtain, in a processed transistor, the base contact resistivity necessary for the 64nm node. This is in part because of contamination and damage to the base contact surface during prior processing. Though we have used [28] Pt/Pd solid-phase-reaction base contacts [30] to penetrate through the surface layer 2-3nm into the base, it is difficult to use such contacts at the 64nm node, where the most-heavily-doped portion of the base is only 4-5nm thick.

We have therefore explored [31] base regrowth (Figure 6). In this process, after forming the emitter contact and etching through the emitter to access the top of the intrinsic InGaAs base, an extrinsic P++ GaAs base is grown by MOCVD. Because the emitter-collector electron current does not pass through the extrinsic base, the extrinsic base P-type doping can be increased to the limits of growth without loss of DC current gain through Auger recombination [32]. Further, because the

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regrown base can be 20-50nm thick, penetrating Pd/Pt contacts can be used. These two factors may permit reduced base contact resistivity.

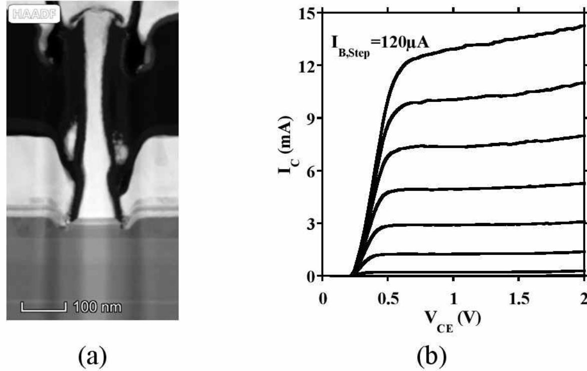

Figure 7: InP HBT with extrinsic P++ GaAs base regrowth (a) and DC common-emitter characteristics (b).

The emitter contact (Figure 7a) is a dry-etched Ti:W alloy; we regularly fabricate 64nm contacts. A Mo contact layer [29] serves as a diffusion barrier at the metal-semiconductor interface, and the metal layers are encapsulated and protected by SiN sidewalls during MOCVD regrowth.

To permit very high doping without hydrogen passivation of the carbon base dopant, the extrinsic base regrowth is lattice-mismatched (and relaxed) GaAs. This presents a valence-band barrier at the InGaAs/GaAs heterointerface, hence the GaAs must be heavily doped to provide low GaAs-metal and GaAs-InGaAs interface resistivities. Though variable between growths and difficult to measure, we observe between $4\times10^{20}\text{cm}^{-3}$ and $1\times10^{21}\text{cm}^{-3}$ extrinsic base doping and less than 1 Ω-μm^2 base contact resistivity.

Figure 7 shows DC characteristics of a device with narrow emitter-base but wide base-collector junctions. We are now working to yield a fully scaled device, seeking to obtain high cutoff frequencies.

VI. InP HEMTs and MOS-HEMTs

InP HEMTs have, at ~1.5THz $f_{\max}$, the highest reported transistor cutoff frequency [33] and, at 1.0THz, the highest demonstrated operating frequency for a transistor amplifier [21]. In part because of higher cutoff frequencies, but primarily because their normalized input resistance $g_m R_{gate}$ is smaller than that ($g_m R_{bb}$) of HBTs, InP HEMTs have the lowest noise figure of all transistors. They are therefore of value in sensitive 100-300GHz receivers. A 3dB smaller receiver noise figure would permit 2:1 smaller transmitter output power, with considerable savings in hardware cost and DC power consumption.

Consider HEMT scaling (Figure 8). To reduce 2:1 gate transit delay at fixed electron injection velocity [34], we reduce the gate length 2:1, but this alone is insufficient to double f_τ, as $1/2\pi f_\tau$ includes substantial delay terms $C_{gs,end}/g_m$ and C_{gd}/g_m associated with charging inter-electrode capacitances. The extrinsic transconductance per unit gate width must double, requiring a doubling in the intrinsic transconductance and 2:1 reduced access resistivities. Because g_m is the product of electron velocity and gate-channel capacitance density, the latter must double if the former is held constant. The remaining relationships in Figure 8 are derived from ballistic transport theory [34,35]; the channel and dielectric must be thinned not only to double g_m but also to maintain a constant g_m/G_{DS} ratio given the reduced gate length.

FET parameter	change
gate length	decrease 2:1
current density (mA/μm)	increase 2:1
contact resistivities	decrease 4:1
specific transconductance (mS/μm)	increase 2:1
→ transport mass	constant
→ 2DEG electron density	increase 2:1
→ gate-channel capacitance density	increase 2:1
→ dielectric equivalent thickness	decrease 2:1
→ channel thickness	decrease 2:1
→ channel state density	increase 2:1

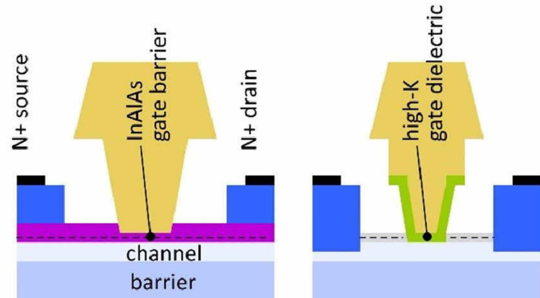

Figure 8: III-V HEMTs scaling laws (top), III-V HEMT (bottom left) and III-V MOS-HEMT (bottom right). The scaling laws are derived in the ballistic limit, assume a fixed (V_{gs}-V_{th}) across scaling generations, and require several parameters (increased 2DEG electron density at fixed transport mass) that are difficult to obtain.

Both channel transport physics and transistor construction impose limits to such scaling. Considering first transistor construction (Figure 8), in a typical HEMT the wide-bandgap InAlAs layer lies both between gate and channel and between the channel and the source/drain contacts. The barrier cannot be thinned much below ~6nm without excessive gate leakage, and the barrier increases the source and drain access resistances.

Replacing the 6nm InAlAs (ε_r=12.5) with a 2nm ZrO_2 (ε_r~25) gate insulator [36,37,38] would increase the gate-channel capacitance density, thereby increasing the transconductance. Further, the InAlAs barrier is removed from the source/drain contact regions, potentially reducing the access resistances. Yet, given that we have not changed the channel material, hence have not increased the channel 2D state density (Figure 8), the expected increase in transconductance is not immediately clear.

From ballistic theory [39], assuming bands with parabolic *E-k* dispersion, $g_m/W_g = 126\text{mS}/\mu\text{m}\cdot K_1\cdot((V_{gs}-V_{th})/1\text{V})^{1/2}$, where K_1, a function of channel and dielectric parameters, is plotted in Figure 9. This approximate analysis suggests that g_m/W_g can indeed be significantly increased. Yet, g_m is also increased by increasing the gate overdrive $(V_{gs}-V_{th})$; given the reality of nonparabolic *E-k* dispersion, g_m is maximized when the channel Fermi level is that giving maximum electron group velocity in the channel. The gate overdrive can also be limited by carriers populating the channel satellite valleys or

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populating the back barrier at large $(V_{gs} - V_{th})$. A more rigorous theory is required.

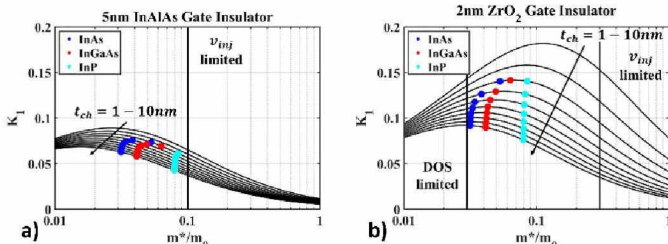

Figure 9: Normalized drain current K_1 plotted for as a function of carrier effective mass m^* and channel thickness t_{ch} for 5 nm thick InAlAs and 2 nm thick ZrO_2 gate-channel insulators. The overlaid points are in-plane m^*, vs. t_{ch} given wavefunction leakage into the InAlAs (for InGaAs and InAs) or AlAsSb (for InP) back barrier.

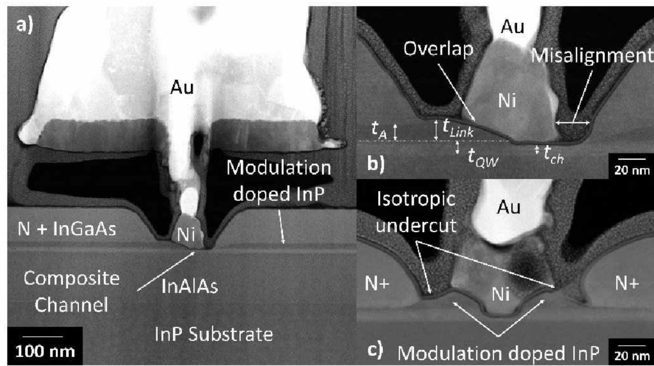

Figure 10: Cross-sectional TEMs of InGaAs-channel MOS-HEMT (a) and (b) with the InAlAs modulation-doped layer only partly removed from the S/D contact regions and (c) a different device with the InAlAs layer entirely removed from the contact regions.

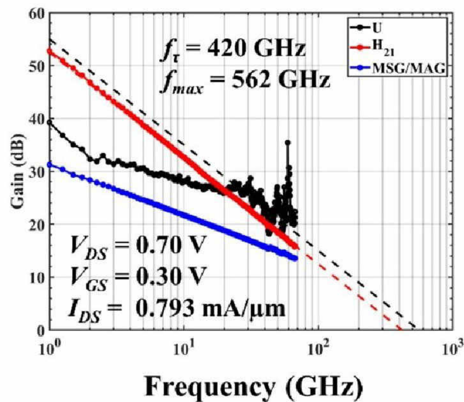

Figure 11: High-frequency gains of a InGaAs-channel MOS-HEMT with L_g=40nm

Experimentally, we fabricated [40] InGaAs-channel MOS-HEMTs in a process with separate MOCVD regrowths pattering the modulation-doped access regions and forming the N+ source/drain contacts. Figure 10 shows a device cross-section, Figure 11 shows RF data, and Figure 12 shows extracted small-signal parameters. It is evident from both the device cross-section, from the large C_{gd}, and from the variation of C_{gs} with gate length, that the device suffers from large parasitic capacitances arising from the misalignment between the gate and the recess in the InAlAs modulation-doped layer. We are developing a self-aligned process.

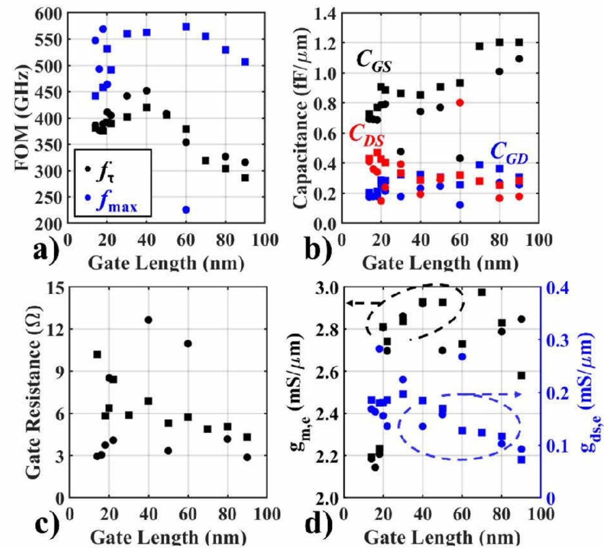

Figure 12: InGaAs MOS-HEMT small-signal parameters versus gate length. The circles are (011) and squares are $(0\bar{1}1)$ conduction (a) f_τ, f_{max} determined by extrapolation (b) C_{GS}, C_{GD} (c) R_G (d) $g_{m,e}$, $g_{ds,e}$

VII. Conclusions

The 100-300GHz spectrum can support short-range wireless backhaul and endpoint communications links with aggregate capacities approaching or exceeding 1Tb/s. To obtain such high capacities, such systems can employ massive spatial multiplexing, using compact transmitter and receiver arrays with tens or hundreds of elements. CMOS can support short-range systems to c.a. 150GHz, and, longer-range systems with the use of SiGe or III-V power amplifiers and LNAs; higher-frequency systems can be realized in III-V and SiGe technologies. Important transistor parameters include the frequency-dependent noise measure, the PAE, and the output power density (W/mm). Power amplifiers for such systems will require ~10-200mW output power; feasible power depends on transistor performance, interconnect losses, and IC integration density. Transceivers will be complex, with 10's-100's of RF channels, hence dense RF IC integration is desirable; technologies with high transistor gain (high f_{max}) provide greater IC density as well as better performance. Best reported 100-300GHz CMOS IC results are in the 65-32nm nodes; future advances in 100-300GHz systems will require developing application-specific mmWave IC technologies, including SiGe, III-V, and mmWave-optimized CMOS.

Acknowledgment

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