135GHz CMOS / LTCC MIMO Receiver Array Tile Modules

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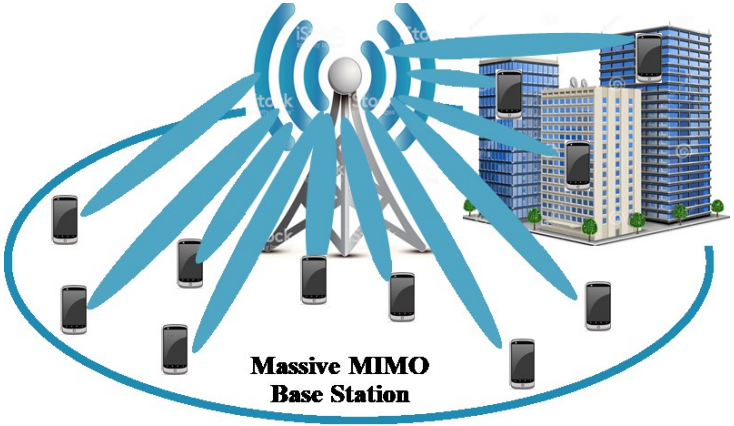
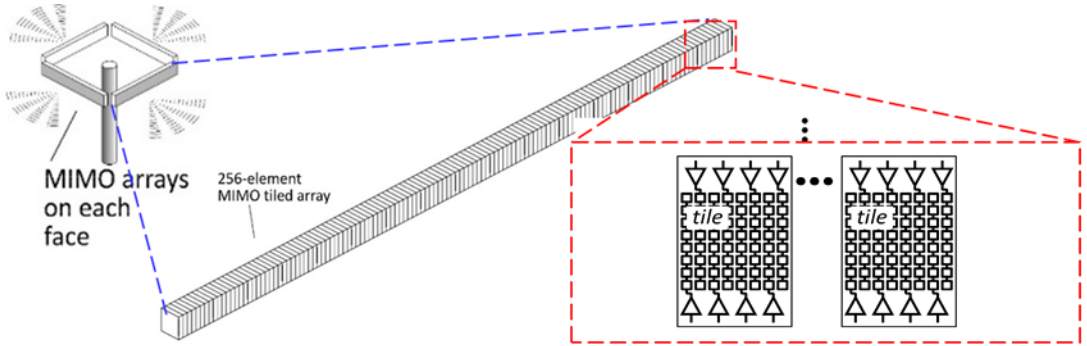
Outline

- Motivation
- IC-Package Interconnect technology
- Interposer Stack build up
- Integrated Receiver module
- Module Wireless Link Experiment
- Conclusion

Opportunities and challenges at mmwave

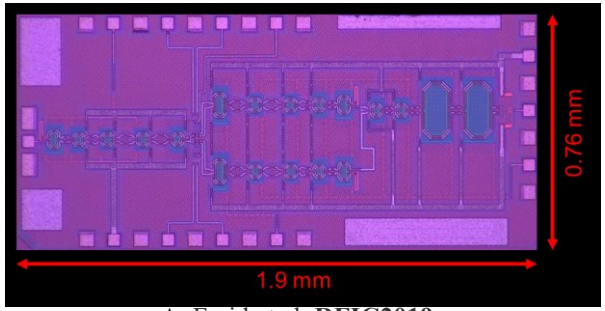


A. Farid at al, **RWS2021**



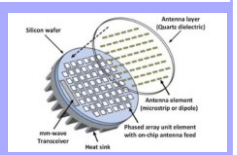
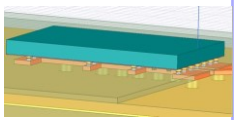
- Large available spectrum ()
- Massive # of parallel channels, Multiple independent beams
- Low-cost high-performance packaging (?)

IC and Package Interconnect



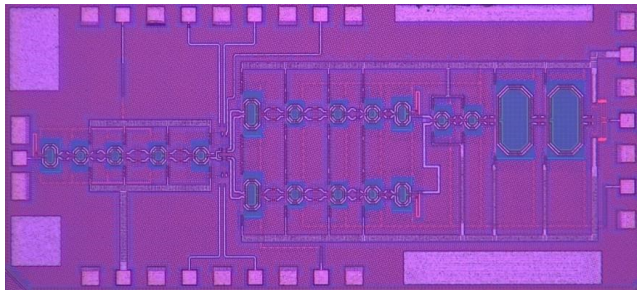
A. Farid at al, **RFIC2019**

- Direct Conversion RX in GF-22FDSOI
- 20GHz 3-dB BW
- 27dB Conversion gain

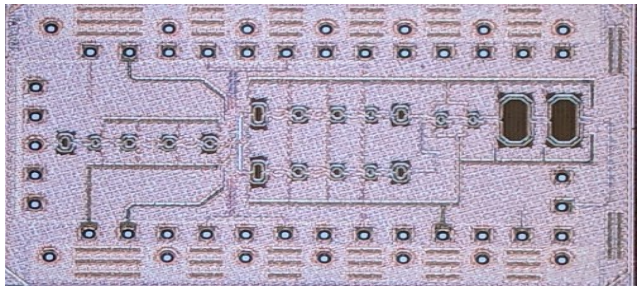
Type	Transition Loss/ Frequency	Technology	Cost	Heatsinking	
(ball) wirebonds	100 GHz ✗	Industry standard	low	good	
ribbon, mesh bond	200 GHz	Handcrafted	high ✗	good	
patch antennas on superstrate	1000 GHz	Straightforward	low	good	
Cu stud flip-chip	>200 GHz	Industry standard	low	OK	

Mark Rodwell, "100-300GHz Wireless: Transistors, ICs, packages, systems."6G Workshop, IEEE RF/Wireless Week (RWW2021), 17 - 20 January San Diego, California, USA

IC and Package Interconnect

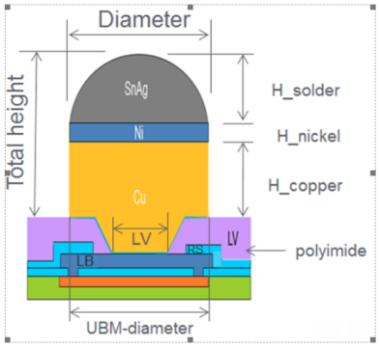


A. Farid at al, **RFIC2019**

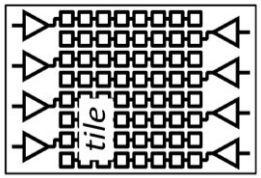


A. Farid at al, **BCICST2021**

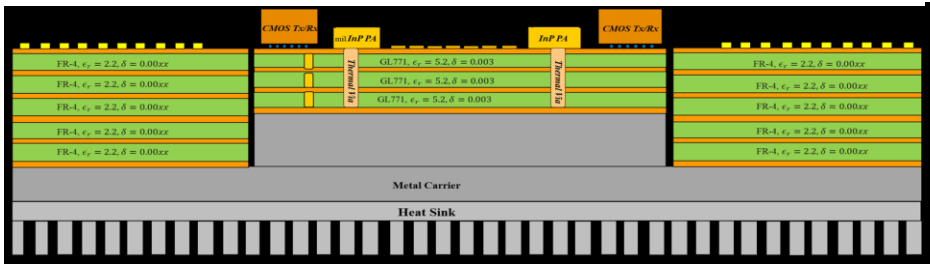
- Chip bonded to LTCC carrier using 50µm diameter copper pillar
- Pillars equally spaced at 125µm
- IC-package transition loss of 1dB



MIMO 1-D Array Tile

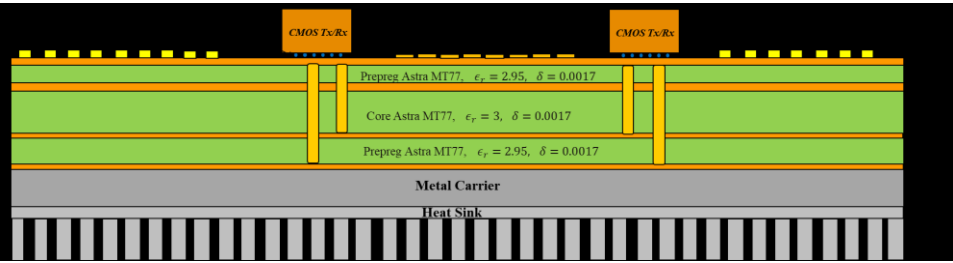


Ceramic Interposer



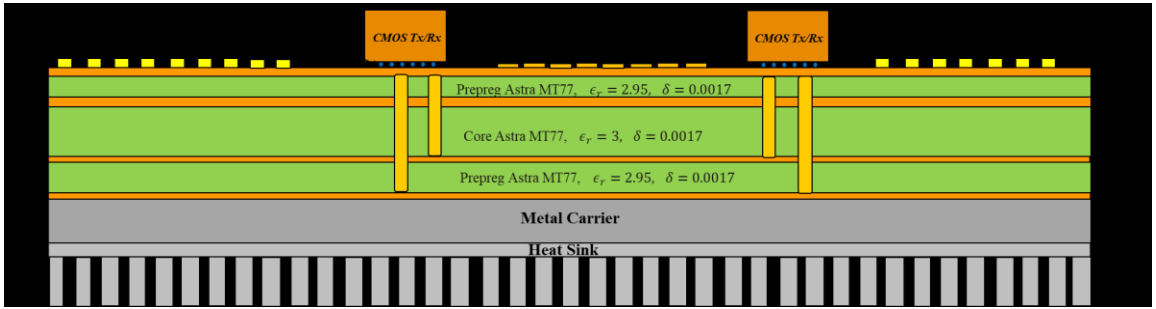
High Lithographic resolution (40µm)	
0.6λ antenna spacing	
Dense wirebond routing from Interposer to carrier board	
Higher Cost and slower turnaround time	

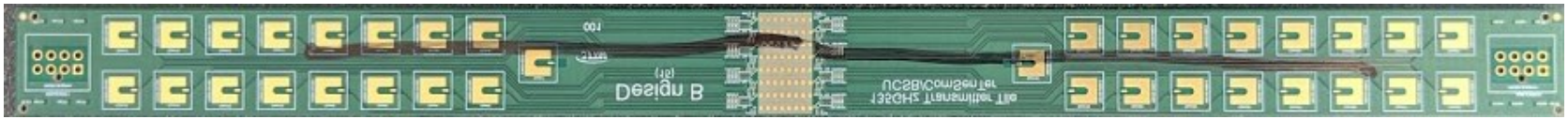
Lower Cost PCB!



Coarse Lithographic resolution (80µm)	
λ antenna spacing	
No need for wire bonding (all solution on one board)	
Lower Cost?	

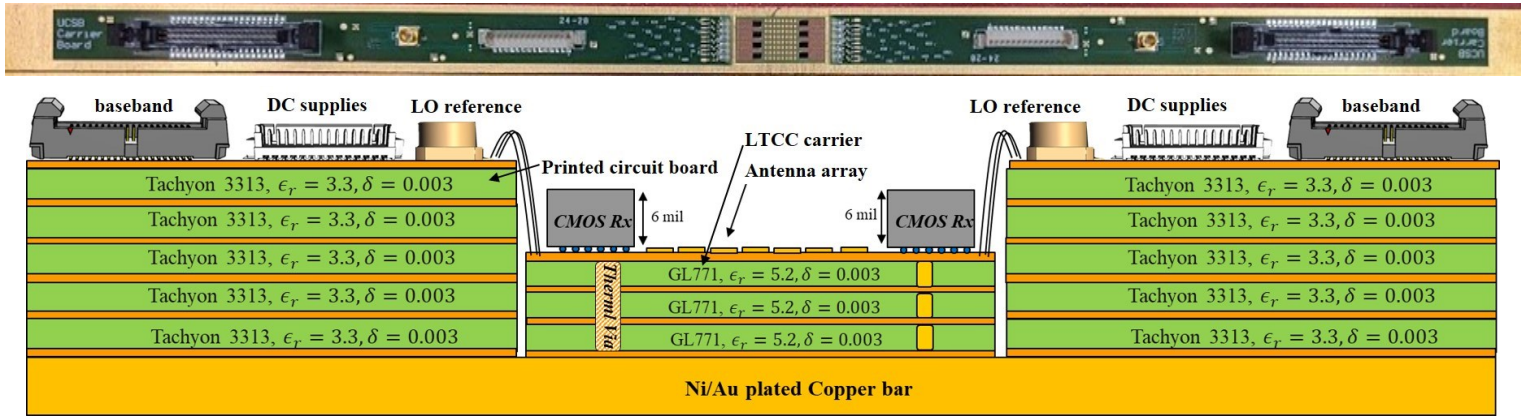
Challenges with the PCB approach



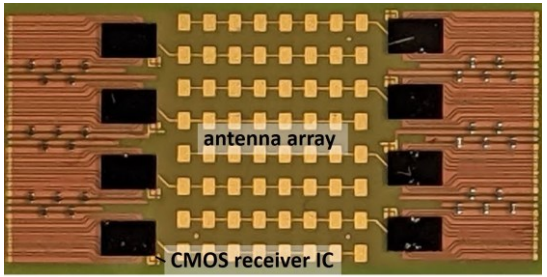


Issues	Lessons learned
Difficulty in bonding copper studs to PCB ▪ Over etched boards/poor quality ▪ Wider solder mask opening ▪ Thick solder mask layers	▪ PCB unsuitable for copper pillars ▪ High resolution PCB is expensive

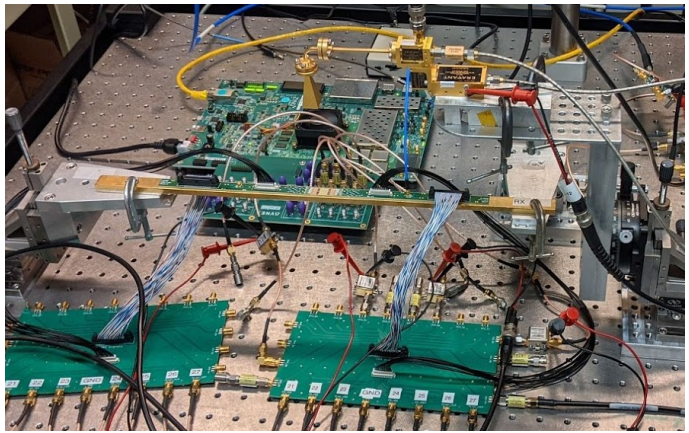
Integrated Receiver Module on LTCC

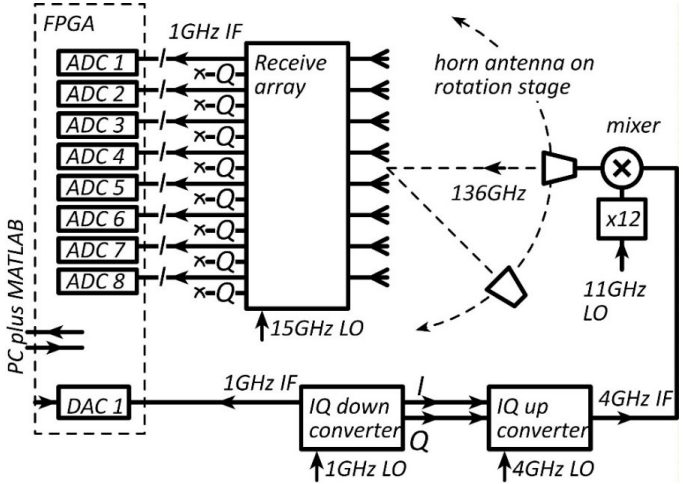


- 4 channels/side
- 8-elements series fed-patch antenna/channel
- 0.65λ antenna spacing
- I/Q , LO, DC signals routed from LTCC to PCB using AL wirebonds (1.25mil)



Module Calibration and Testing Setup

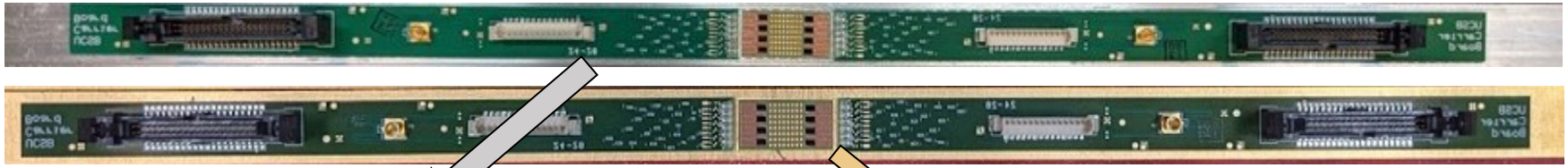


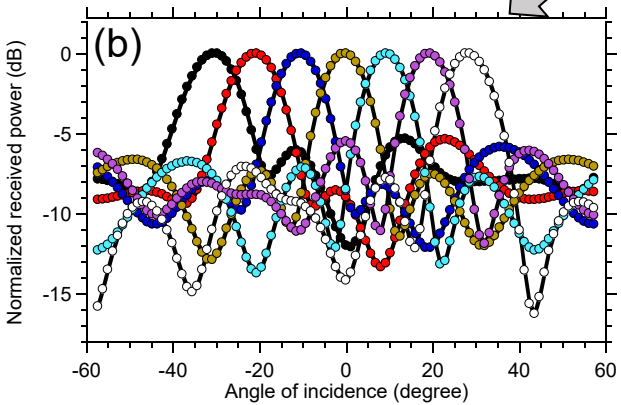


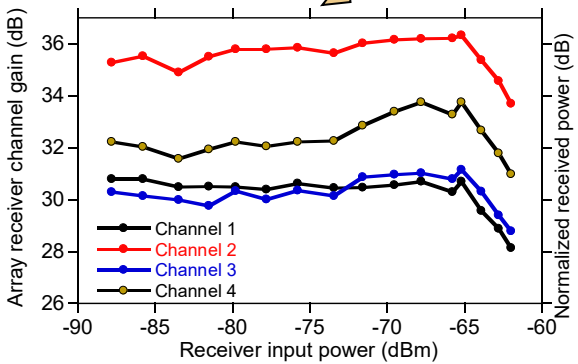
- Rx module connected to ZCU-111 for array calibration and beamforming.
- Test transmitter mounted at 15cm distance on a rotating arm.
- Wideband 1-GHz OFDM signal used for array calibration (explain briefly)

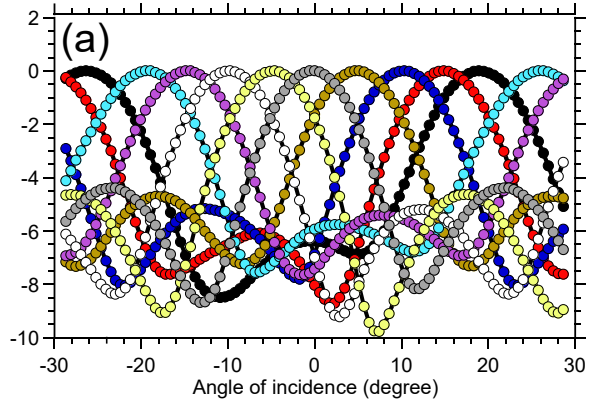
https://github.com/pi-radio/Pi-Radio-v1-NRT
https://dl.acm.org/doi/abs/10.1145/3411276.3412195

Module Conversion Gain & Radiation Pattern





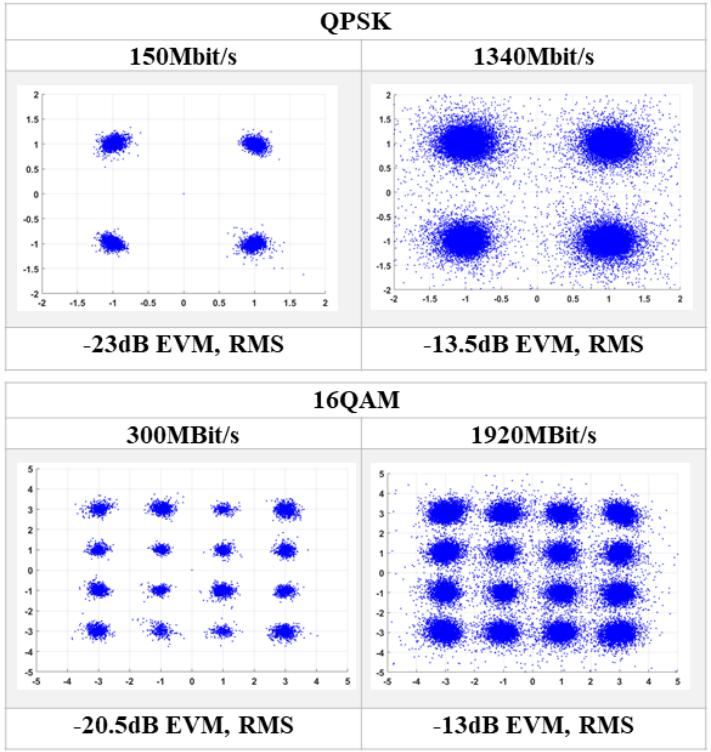


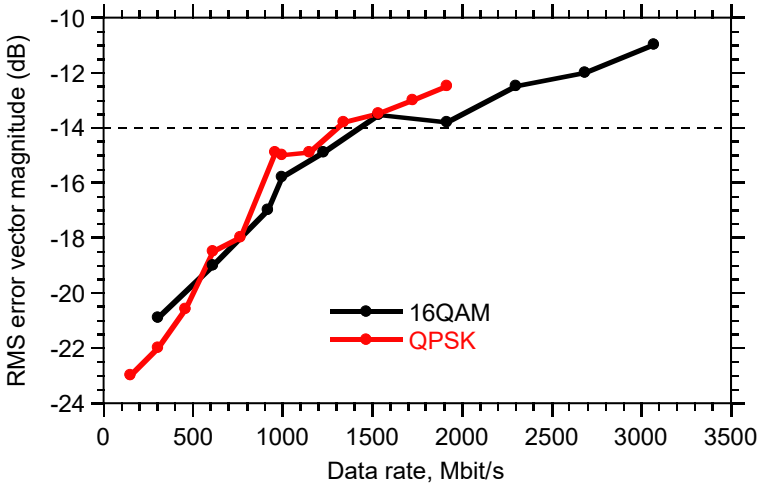


- 8-working channel
- floating ground!

- 4-working channel
- 1.3 λ antenna spacing (Limited F.O.V)

Receiver Module Wireless Link





In single-beam operation: there is –

- 13.5dB RMS EVM in 1.34Gb/s QPSK
- 13dB EVM, RMS in 1.92Gb/s 16QAM

What is limiting Module datarate?

Comparison with state of the art

	Townley CICC2020	Singh RFIC2020	S. Li IMS2021	Abu-Surra ICC2021	Sawaby RFIC2020	
Freq (GHz)	113	115-155 135-170	140	140	135	
IC Technology	28nm CMOS	0.13µm SiGe	45nm SOI	45nm SOI	0.13µm SiGe	
Package Technology	PCB	Radio on Glass	Quartz Superstrate	PCB	PCB + Lens	
Type	1 Channel	1 Channel	Single beam	MIMO$	2x2 LOS MIMO	
# of channels	2	1	8	4,8, and 16	2	
Antenna	Yes	No	Yes	Yes	Yes	
Data rate	80Gb/s	36Gb/s 8Gb/s	16Gb/s 18Gb/s	6Gb/s	2x16Gb/s	
Format	16QAM	64QAM /256QAM	QPSK 64QAM	16QAM	QPSK	
EVM	--	-23dB -30dB	6.25% 5.5%	NA	--	
Link	Air	WR-6	Air	Air	Air	
Distance	10cm	--	--	15m	6cm	

Conclusion

- Packaging approach for massive MIMO arrays in Tile
- Assembly challenges with advanced copper pillars
- Why PCB approach is not the right candidate
- Tile of 8-elements with 3Gb/s per beam

Acknowledgment

Authors would like to thanks

- Kyocera Japan for ceramic interposer fabrication
- Kyocera San Diego for module assembly
- GlobalFoundries for CMOS chip fabrication and free access to advanced copper pillars

This work was supported in part by the Semiconductor Research Corporation and DARPA under the JUMP program.

Questions?