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ABSTRACT

Template-assisted selective area growth techniques have gained popularity for their ability to grow epitaxial materials in prefabricated dielectric templates. Confined epitaxial lateral overgrowth (CELO) is one such technique that uses dielectric templates to define the geometry of the grown nanostructures. Two terminal low-temperature magneto-transport measurements were used to determine electronic properties. For doped $In_{0.53}Ga_{0.47}As$ CELO nanostructures, we observe Shubnikov–De Hass oscillations in the longitudinal magnetoresistance and utilize these to estimate effective mass, carrier density, and mobilities. This analysis both reveals the presence of defects in these nanostructures and material variabilities between growth runs. Electron beam lithography and contact deposition for transport measurements were enabled by parasitic growth removal. In the future, this approach can enable other material systems to be explored for confined lateral epitaxy, improve material quality, and investigate a variety of quantum transport phenomenon in such nanoscale devices.

I. INTRODUCTION

Semiconductor nanostructures have attracted interest for their novel electronic[1] and optical properties.[2] Quantum confinement effects, which dominate in the sub-micrometer length scales of the nanostructures, have potential applications in diverse fields, such as quantum computing,[3–5] high-speed transistors,[6–11] spintronics,[3,12,13] and on-chip integrated photonic circuits.[14–16] For optimal performance of such quantum devices, it is essential to fabricate high-quality nanostructures with custom geometries and integrate them on a wide range of substrates. To this end, confined epitaxial lateral overgrowth (CELO) has emerged as one of the most promising techniques for growing defect-free nanostructures on lattice mismatched substrates.[17,18] CELO is a bottom-up template-assisted growth method that uses epitaxial selective area growth on substrates with prefabricated dielectric templates. Selective area growth restricts the nucleation of precursors to the dielectric-free areas of the substrate.[19] The templates act as defect filters using aspect ratio trapping and thereafter confine the growth and its direction on the substrate. CELO thus allows the growth of nanostructures in pre-determined custom geometries and orientations, eliminating the need for post-growth processing. Channel dimensions can be scaled down to tens of nanometers without the challenges of dry-etch-induced defects, which are common for top–down fabrication routes. As a result, CELO has the potential to fabricate high-quality photonic lasers,[14] transistors,[20] and devices to study quantum transport in low-dimensional nanostructures.[21,22]

Material properties in nanostructures, such as CELO, often deviate significantly from those of planar epitaxial structures grown under similar conditions.[23–25] For example, depending on growth conditions, CELO-grown III–V materials exhibit variations in defect densities,[26] spatial gradients in ternary compositions, and facet-specific group-III incorporations.[27,28] Quantum confinement in these low-dimensional nanostructures can result in a change in band parabolicity leading to changes in carrier effective mass and mobilities. As a result, electrically characterizing CELO nanostructures is crucial for both understanding material qualities and optimizing growth conditions.

Unfortunately, CELO growths often exhibit unwanted III–V nucleation [Figs. 1(a)–1(c)] on the dielectric mask, also known as parasitic growth.[29] Growing CELO nanostructures with no parasitic nucleation is challenging and often requires constraining the growth parameters within a narrow window, which may not yield

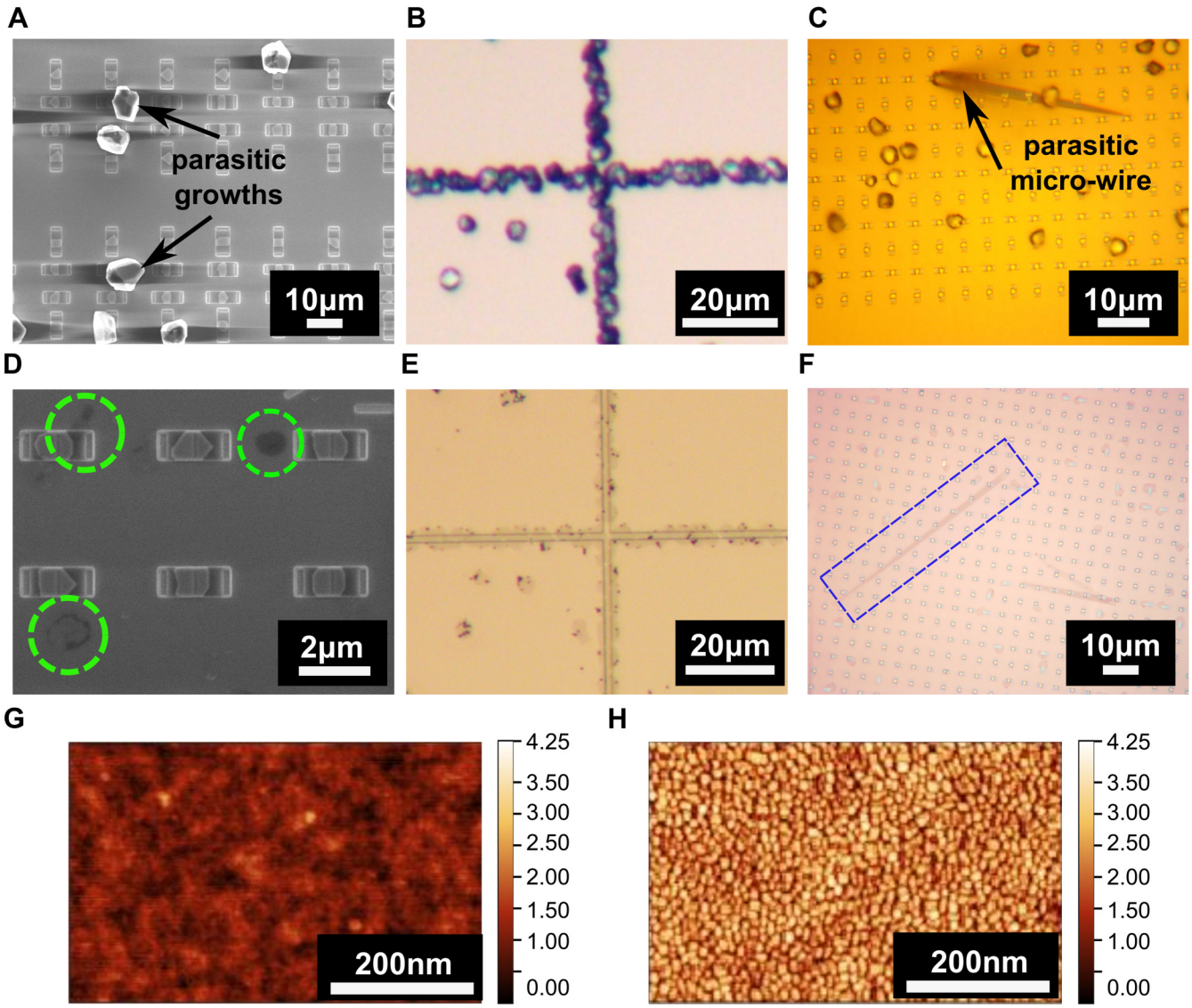

FIG. 1. (a), (b), and (c) show a CELO InGaAs sample and (d), (e), and (f) the corresponding samples after the cleaning processes described in the text. (a) and (d) are SEM images, while (b), (c), (e), and (f) are optical microscope images. Green circles in (d) show where parasitic growths were before the cleaning process. Dashed box in (f) shows a region (different from c) where a parasitic microwire growth existed before etching. (g) shows the surface of SiO_2 after the wet etch process. (h) shows the SiO_2 surface after 20 min of exposure to MHA plasma etch in the RIE.

the highest electronic properties. Clear and precise alignment marks are essential for further device processing requiring sub-micrometer alignments. Epitaxial growths of a few hundred nanometers inside the CELO templates often result in parasitic nucleation that are tens of micrometers in size.[30] Preferential nucleation of parasitic growths on rough edges of the patterned dielectric often covers these alignment marks completely. This makes the sample alignment required for further lithographic processing of CELO structures nearly impossible. In addition, due to the rough oxide topography resulting from nucleation, there is a high failure rate in forming metal contacts to the nanostructures. Hence, a method to circumvent the parasitic growth is required in order to enable further processing of these nanostructures into devices for subsequent electrical characterization.

In this article, we demonstrate a rapid, yet gentle multi-step etch method, which removes the parasitic growths while leaving the growths inside the template undisturbed. With the successful removal of parasitic growths, it is now possible to fabricate devices

and perform electrical measurements, which opens up the possibility of investigating a broad range of materials and growth conditions. In this study, we explore the technologically relevant InGaAs material system. This material's high electron mobility and direct bandgap makes it attractive for a wide range of electronic and photonic applications, especially for telecommunications, high-frequency electronics, and topological quantum computing.[31–37] Electrical transport measurements at low temperatures can allow us to extract parameters important for the use of InGaAs in semiconductor nanowire networks for Majorana fermions,[31] spin field effect transistors,[32–34] high-performance nanoelectronics,[35] terahertz detectors,[36] or optoelectronic devices.[37] Here, we demonstrate the fabrication of devices and measurements of magnetoresistance behaviors at cryogenic temperatures for in-plane InGaAs CELO nanostructures in samples with a high density of parasitic growths. We achieve this with the use of the post-growth parasitic growth removal process, which makes the precise alignment and fabrication of contacts possible. Due to the small size of the nanostructures, a two-terminal device design was chosen over making a more conventional four or six contact Hall device for yielding more reliable contacts. From the observed Shubnikov–De Haas (SdH) oscillations in the magnetoresistance of these two terminal devices, we extract doping concentration, effective mass, and quantum mobility in these nanostructures. These measurements clearly reveal variability in material parameters between different growth runs, which is crucial to understand device performance. Thus, the use of our etching process flow allows one to grow with a wider range of growth conditions and materials and their heterostructures in the CELO geometry, optimize the material quality, and fabricate electronic and photonic devices with greater control. The mechanism outlined here is generalizable and can be extended to investigation of interesting physics in the nanostructures of a broad range of other semiconductors, metals, and topological materials.

II. METHODS

CELO templates were fabricated by depositing a 5 nm Al_2O_3 etch stop layer using atomic layer deposition (ALD) and a 20 nm bottom dielectric SiO_2 via plasma-enhanced chemical vapor deposition (PECVD). Seed holes were lithographically defined, and a 50 nm sacrificial chemically semi-amplified positive electron-beam resist (CSAR) layer was spin coated and patterned using electron beam lithography (EBL). Next, hydrogen silsesquioxane (HSQ) was spin coated as the 100 nm top dielectric, in which source holes were lithographically defined. The sacrificial layer was removed with 1-methyl-2-pyrrolidone stripper (NMP) followed by remote oxygen plasma at 350 °C. A final tetramethylammonium hydroxide (TMAH) wet etch was used to remove the alumina layer exposing the seed, and a dilute HF dip was executed before growth. Growth using metal organic chemical vapor depositions (MOCVD) was done in a horizontal reactor using trimethylindium (TMIn), trimethylgallium (TMGa), tertiarybutylphosphine (TBP), and tertiarybutylarsine (TBA) with H_2 as carrier gas. The samples were grown at 600 °C, with a group III flux of 5×10^{-6} mol/min and a V/III ratio of 570. For the samples discussed in the study, the growth was initiated with a few monolayers of InP before switching the growth to n-doped InGaAs. Si doping is incorporated in the InGaAs layer with a disilane flux of 1.43×10^{-8} mol/min. More details on the fabrication, growths, and structural characterization of CELO can be found in other works.[28,30] Planar epitaxial Si-doped InGaAs samples for carrier density comparison were grown at 600 °C, with a group III flux of 3.82×10^{-5} mol/min, a V/III ratio of 8.8, and a disilane fluxes of 1.43×10^{-8} mol/min.

We used a combination of dry and wet etching to selectively remove the parasitic growths (Fig. 2). After rinsing the sample in acetone and isopropanol, 6 nm aluminum oxide (Al_2O_3) was deposited on the sample in an atomic layer deposition (ALD) chamber using a trimethylaluminum-water (TMA-H_2O) recipe at 300 °C. This conformally coats the sample including the outside surface of the growth inside the CELO templates and the parasitic growth [Fig. 2(c)]. The samples were then etched in an inductively coupled plasma (ICP) chamber using BCl_3/Cl_2 chemistry for 15 s with an approximate etch rate of 80 nm/min. Since ICP etching is highly anisotropic, the etch removes Al_2O_3 that is in line of sight of the ions that are accelerated toward the bottom cathode. The thick silicon dioxide top layer stops the ion beams from etching the Al_2O_3 that covers the outer surfaces of the overgrowths inside the CELO templates [Fig. 2(d)]. Similarly, the Al_2O_3 that is underneath the parasitic growths are protected from incoming ions. The ICP etching effectively exposes the top of the parasitic growths while keeping the nanostructures of interest inside the cavity protected by Al_2O_3. It is important to note here that for the successful use of this process, the outer edge of growth inside the CELO cavity should be under the top dielectric and laterally shorter than the seed holes. Otherwise, the ICP etch will remove the ALD dielectric under the seed hole and expose the active area to subsequent etching steps.

Using a wet etch we then selectively etched these parasitic growths without affecting the overgrowths in the CELO templates [Fig. 2(a)]. For the InGaAs CELO sample, we used a $H_3PO_4/H_2O_2/H_2O$ (1:1:20) solution for 12 min to etch away the parasitic growths. After careful inspection of the samples to make sure that all parasitic growths had been etched completely, the samples were put into AZ 300 MIF (Metal Ion Free 0.261 N tetramethylammonium hydroxide) developer solution for 5 min to etch away any remaining Al_2O_3 (etch rate of 1.6 nm/min). A quick rinse in acetone and isopropanol was used to clean any residues. The samples are thus clean of any parasitic growths and with the original overgrown structures intact [Fig. 2(f)]. Dark outlines are sometimes observed after the entire cleaning process in the positions where the parasitic growths initially existed [Fig. 1(d)]. We hypothesize that these result from local changes in the oxide due to the parasitic growths' nucleation. These dark spots are of negligible thickness and do not pose any problems while aligning samples or depositing contacts.

After achieving selective removal of parasitic growths, we were now able to proceed with the device fabrication on the InGaAs CELO samples. The alignment marks, free of all parasitic growths [Fig. 1(e)], could now be used in the electron beam lithography (EBL) tool. Using CSAR, vias were defined [Fig. 1(g)]. The vias were etched in the silicon dioxide top layer of the CELO templates using a $CHF_3/CF_4/O_2$ recipe in the ICP [Fig. 2(h)]. After cleaning the samples in a plasma asher followed by solvent rinse, contacts were patterned using a bilayer resist process. The resist stack

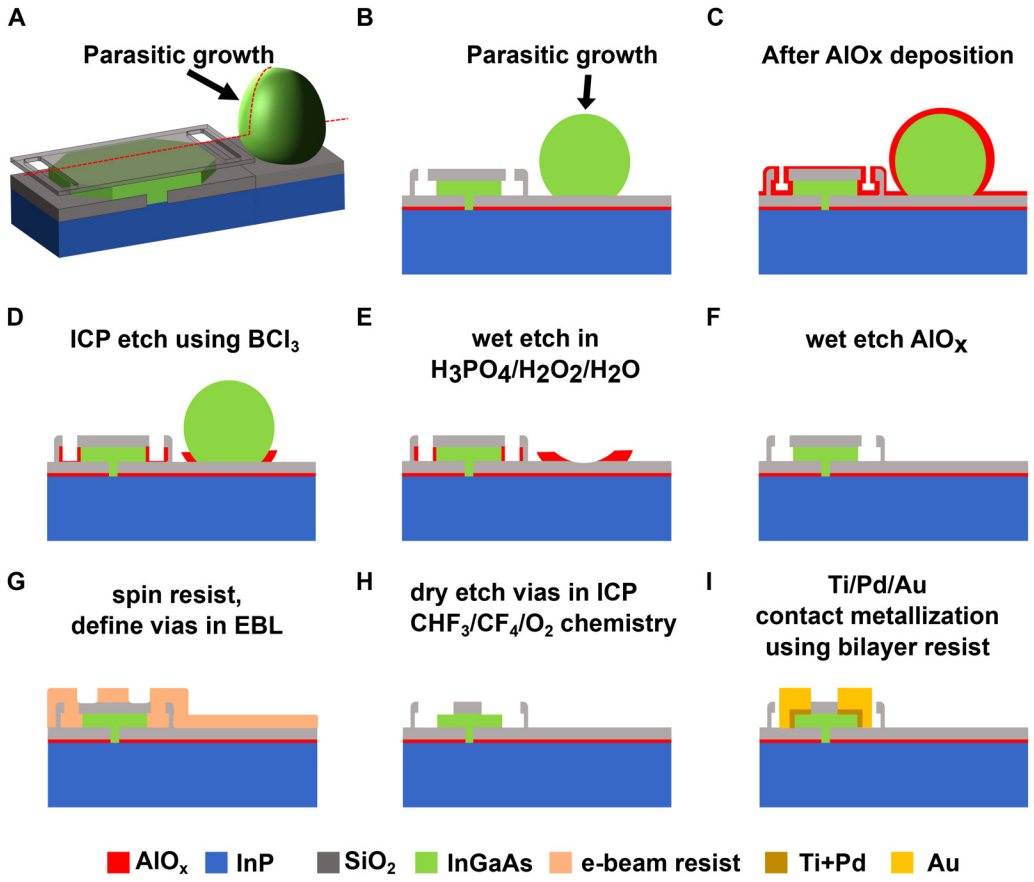

FIG. 2. (a) shows the 3D schematic of InGaAs CELO growth along with a parasitic growth. (b) shows a cross section schematic taken along the red dashed line in (a). (c)–(i) show the process flow for selectively cleaning parasitic growth and fabrication of vias and contacts. It is critical that the outer edge of the active region (green area in c) is protected by the top dielectric for subsequent etching steps.

consists of 100 nm of copolymer EL9 (ethyl lactate 9%) and 400 nm of PMMA 950 K. To ensure that all remaining surface oxides are etched for making an ohmic contact, a 30 s dilute HCl (1:10) etch was performed immediately before metal deposition. To ensure proper adhesion and ohmicity of the contacts, we deposited a metal stack 10 nm of Ti followed by 10 nm of Pd and 200 nm of Au using electron beam evaporation [Fig. 2(i)].

III. RESULTS AND DISCUSSION

Our process flow achieved successful parasitic growth removal on the InGaAs CELO samples as characterized by scanning electron and optical micrographs [Figs. 1(a)–1(f)]. Notably, large micro-wire parasitic growths that were present previously [Fig. 1(c)] were completely removed [Fig. 1(f)]. The contrast from the InGaAs growth inside the templates remains unchanged in the optical microscope and SEM images, indicating that the CELO growths inside the templates are unaffected by this etching process. We compared the effects of our etching process to a conventional plasma-assisted dry etch using a $CH_4/H_2/Ar$ chemistry in a reactive ion etcher (RIE). Although RIE-based etches can partially remove the parasitic growths, the etch rates were found to be low and the time to completely remove thick parasitic growths (which are often tens of micrometers thick) was long (>30–40 min). Atomic force microscopy (AFM) scans revealed that a 20-min RIE etch results in an extremely rough surface oxide [Fig. 1(h)]. Such plasma processes are known to introduce highly mobile defects in semiconductors[38] and deteriorate the quality of the exposed oxide. In comparison, AFM scans of our wet etch processed samples show that the root mean square roughness of the oxide is considerably lower than that of RIE-etched samples [Fig. 1(g)].

To characterize the material properties of these nanostructures after sample cleaning and fabrication of devices, we use linear two-terminal magneto-transport measurements in both two-terminal and four-terminal (separate probes for current and voltage on the same metal/semiconductor contact) configurations (Fig. 3). Such transport measurements can help reveal variations in electrical properties of these nanostructures grown under different growth

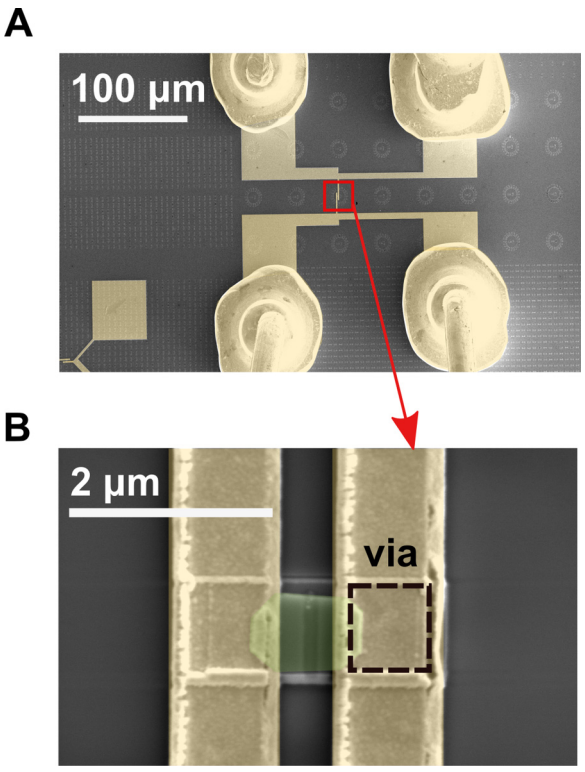

FIG. 3. (a) False color SEM images of device with contacts and (b) magnified SEM image of the InGaAs CELO device (marked in green) with vias and contacts.

conditions and spatial variations in a single sample. Given the small dimensions of the nanostructures, two-terminal devices offer advantages in terms of fabricating reliable contacts,[39,40] compared to a conventional Hall device, which requires at least four terminals. The technique also avoids variabilities in gate dielectric properties for field effect measurements of mobility. The devices were measured in a Quantum Design Physical Property Measurement System (PPMS). The devices were wire-bonded to a PPMS puck using a 25 μm gold wire. The devices were found to be extremely sensitive to electro-static discharge, so caution was taken to ground the sample while bonding and transfer. The InGaAs devices were measured using standard AC low frequency (13 Hz) lock-in technique at temperatures ranging from 2 to 300 K. The contacts were found to be ohmic at all temperatures [Fig. S1(a) in the supplementary material]. The resistance of the device increases with decreasing temperatures [Fig. S1(b) in the supplementary material]. The successful fabrication of contacts on InGaAs CELO samples thus allows us to now perform transport measurements to characterize the material quality in these samples.

Magnetoresistance measurements of two samples grown under the same growth conditions and similar Si doping concentrations are explored (Fig. 4). Sample 1 [Figs. 4(a)–4(c)] was measured using a four-probe configuration, while sample 2 [Figs. 4(d)–4(f)] was measured in a two-probe configuration (for two-probe configuration, total line resistance of 4 kΩ is effectively added to the device resistance). Longitudinal resistance R_{xx} was measured as a function of a perpendicular magnetic field (applied out of plane to the sample surface) at 2 K. The resistance exhibits positive magnetoresistance with well-defined superimposed oscillations at high fields [Figs. 4(a) and 4(d)]. A parabolic background is observed in the magneto-resistance plots, which typically arises from the Drude conductivity being inversely related to [1+ (μB^2)], μ being the mobility and B being the magnetic field. To analyze the observed oscillations more clearly, a third-order polynomial background subtraction was performed [Figs. 4(b) and 4(e)]. At magnetic fields higher than 2 T, ΔR_{xx} oscillates periodically in an inverse magnetic field (1/B). This can be interpreted as Shubnikov–De Haas oscillations due to the formation of Landau levels (LL) in the high magnetic field. Fast Fourier analysis of the oscillations [Figs. 4(c) and 4(f)] reveals frequencies of $B_F = 39$ T and $B_F = 45$ T corresponding to sample 1 and sample 2, respectively. Assuming a spherical Fermi surface, the Fermi wavevector corresponding to these two frequencies are $k_{F1} = 0.3463\,\mathrm{nm}^{-1}$ and $k_{F2} = 0.3695\,\mathrm{nm}^{-1}$ with doping levels of 1.4×10^{18} and $1.9 \times 10^{18}\,\mathrm{cm}^{-3}$, respectively. These two samples were expected to show similar behaviors because of same growth conditions but surprisingly revealed variabilities of doping incorporations between different growth runs. This variability further underscores the importance of characterizing material quality in CELO growths. To compare doping densities in CELO to doping incorporations in conventional planar samples, room temperature Hall measurements were performed on Si-doped planar InGaAs samples. The planar sample was grown with the same disilane flux as for the CELO samples (1.43×10^{-8} mol/min) but with a lower V/III ratio. The doping concentration measured in this sample was $2.53 \times 10^{18}\,\mathrm{cm}^{-3}$. However, it is not straightforward to compare doping densities from planar growth to CELO nanostructures; because compared to planar epitaxial growth, CELO growths typically require a significantly lower group-III flux to lower parasitic growth rates. Since Si doping in planar InGaAs growths decreases significantly with increasing V/III ratio,[41] the Si incorporation at a V/III ratio comparable to a CELO growth is likely lower than this number. As a result, Si doping incorporation in InGaAs CELO appears to be comparable to doping incorporation in planar epitaxial growths.

To obtain electron effective mass, mobility, and scattering length in these nanostructures, the temperature dependence of SdH oscillations in ΔR_{xx} was analyzed. The amplitude of the SdH oscillations decreases with increasing temperature, but the oscillations are observed distinctly up to 50 K [Fig. 5(a)]. Measuring the resistance values at the peak corresponding to $\frac{1}{B} = 0.092\,T^{-1}$, we fit the peak amplitudes to the Lifshitz–Kosevich equation (LK),[42]

$$\frac{X}{\sinh(X)}, \text{ where } X = \frac{\left(2\pi^2 k_B m_e \left(\frac{1}{B}\right) m^* T\right)}{(\hbar e)}.$$

Here, k_B is the Boltzmann constant; m_e is the rest mass of an electron; m^* is the dimensionless effective cyclotron electron mass, i.e., $m^* = m/m_e$, where m is the mass of electrons in InGaAs; T is the

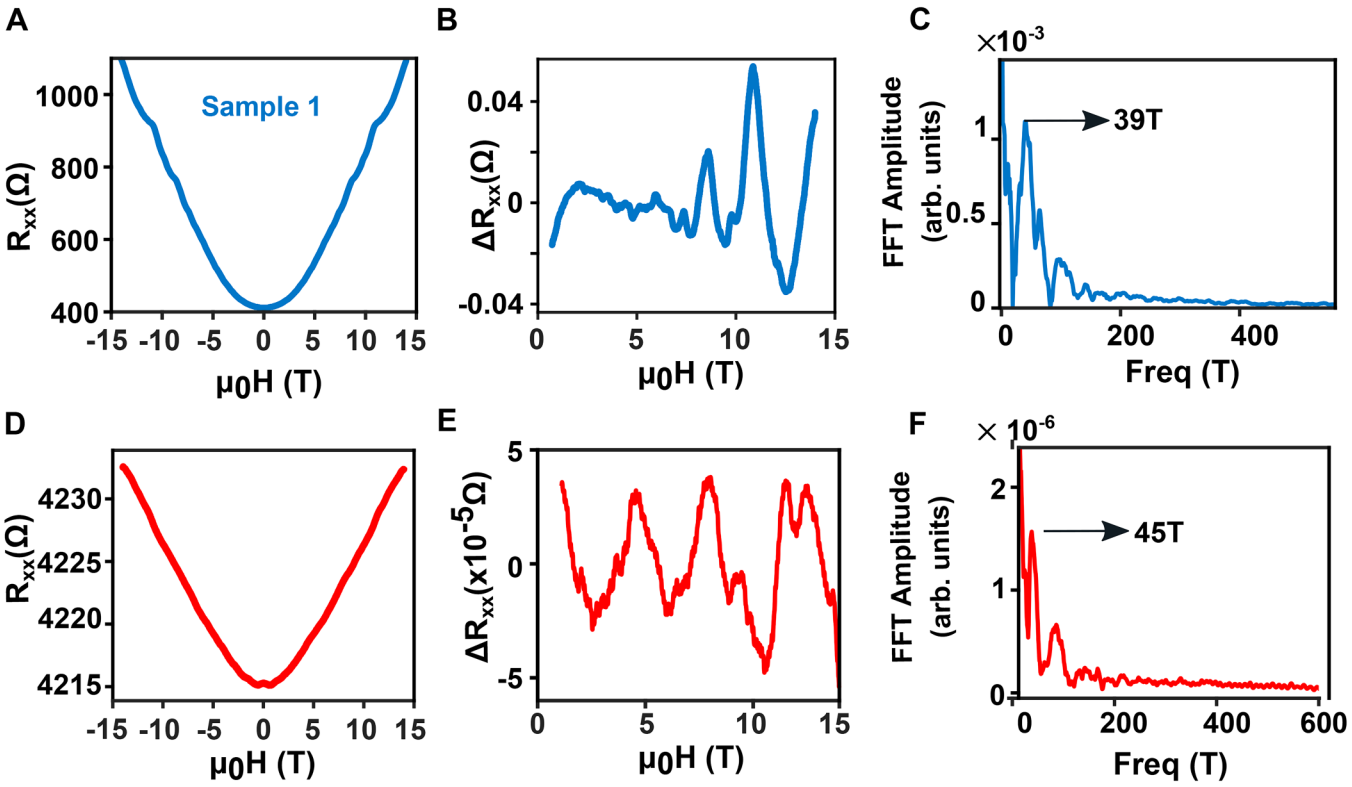

FIG. 4. Low-temperature magneto-transport. (a)–(c) show measurements for sample 1 and (d)–(f) show measurements of sample 2. (a) and (d) show longitudinal magnetoresistance for sample 1. (b) and (e) show data in (a) and (d) after background subtraction, respectively. SdH oscillations are visible in both samples. (c) and (f) show the FFT of ΔR_{xx} vs $(1/\mu_0 H)$ for the two samples. Peaks are observed for subband oscillations corresponding to 39 and 45 T for samples 1 and 2. These correspond to doping concentrations of 1.4×10^{18} and 1.9×10^{18} cm^{-3}, respectively. Sample 1 was measured in a four-probe configuration, while sample 2 was measured in a two-probe configuration (with 4 kΩ series line resistance).

temperature in Kelvin; $\hbar = \frac{h}{2\pi}$, h being the Planck constant; and e is the charge of an electron in Coulombs. From the fit temperature dependence of the peak amplitude to the LK equation [Fig. 5(b)], the effective mass was estimated to be $m = 0.075 \times m_e$. This value is higher than the typical value of electron effective mass in planar $In_{0.53}Ga_{0.47}As$ samples lattice matched to InP reported in other works.[43] The increase in electron effective mass in CELO InGaAs compared to a planar sample can be because of combination of factors such as higher band parabolicity due to quantum confinement in the nanostructures,[44,45] penetration of electron wavefunction into the barrier oxide layers,[46] or possible higher subband occupations.[47] The scattering time τ can be extracted from the slope of the plot of $\ln\left(\frac{\Delta R_{xx}\sinh(X)}{X}\right)$ vs 1/B for the peaks in ΔR [Fig. 5(c)]. The slope value of −45.9 (slope equals to $-\frac{\pi . m}{e . \tau}$) corresponds to an estimated quantum lifetime of $\tau = 2.919\, e^{-14}\, s$ and a Dingle temperature $T_D = h/(4\pi^2 \times k_B\, \tau)$ of 41.6 K. These values of effective mass and scattering time correspond to a quantum mobility of

$$\mu = \frac{e.\ \tau}{m^*.\ m_e} = 684 \frac{\text{cm}^2}{\text{V.s}}$$

and a scattering length of

$$l_F = \tau \times \frac{\hbar\ .\ k_F}{m} = 15.6\,\text{nm}.$$

In comparison, room temperature Hall measurements on 100 nm thick InGaAs films grown on semi-insulating InP yielded mobilities of 3900 cm^2/V s corresponding to a doping density of 3.0×10^{18} cm^{-3}. Similar films grown by molecular beam epitaxy yielded similar Hall mobilities at room temperature.[48] Since mobility generally increases with lower temperature due to reduction in phononic scattering source, we can see that the mobility in the CELO nanostructures is considerably lower compared to planar InGaAs films. InGaAs nanowires with low defect densities have also been reported to show higher mobility values of 7500 cm^2/V s at low temperatures.[35] The low scattering length and low mobility in CELO InGaAs suggests the presence of a large number of defects in this particular sample. This observation correlates well with transmission electron microscopy studies of these nanostructures exhibiting significantly high density of stacking faults at a growth temperature higher than 600 °C.[26] Low-field ΔR_{xx} data show

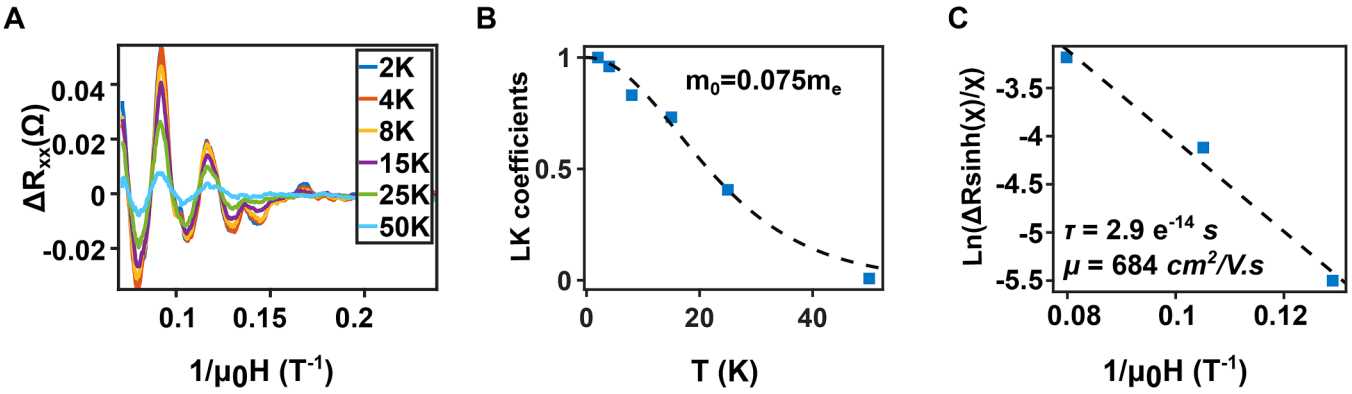

FIG. 5. (a) Shows the background subtracted magnetoresistance for sample 1 [Fig. 4(a)] in the inverse field at temperatures from 2 to 50 K measured in a four-probe configuration. (b) Fit of peak amplitude to Lifshitz–Kosevich equation to extract effective mass of $m = 0.075 \times m_e$. (c) shows the Dingle plot extracted from peak amplitudes in (a). Slope from linear fits gives quantum scattering lifetime and quantum mobility.

signatures of weak localization (WL) in both samples (Fig. S2 in the supplementary material), which also indicate the presence of disorder in these nanostructures. In addition, mobility in the CELO nanostructures can be degraded due to increased surface scattering from sidewall roughness[35] and enhanced charged impurity scattering at lower temperatures. Thus, the magneto-transport measurements serve as a comprehensive feedback for understanding and improving the material quality in CELO nanostructures.

It should be noted that the parasitic growth removal process outlined here for InGaAs nanostructures can be extended to lateral growth of other materials including semiconductors such as GaAs[23] or GaSb[49] that exhibits a large number of parasitic growths. Parasitic growth on the alignment marks makes it virtually impossible to achieve alignment in electron beam lithography (Fig. S3 in the supplementary material), limiting further fabrication of useful device structures for transport measurements. The procedure presented here overcomes this challenge. The technique also removes the constraint on the choice of dielectrics that can be used as a masking material even if they result in the formation of parasitic growths.[50] The crucial mechanism of this technique relies on conformal coating of the CELO nanostructures using an ALD dielectric. If the top of the nanostructure (active region) is protected by an oxide template, a subsequent directional dry etch of the ALD dielectric will always preferentially expose the parasitic growth and keep the nanostructures completely encased and protected. It is critical that the outer edge of the grown nanostructure is protected by the top dielectric in the CELO cavity and is not exposed to seed holes. This helps in selective wet etching the parasitic growth without affecting the CELO nanostructures irrespective of the material used in the active region. Extending the concept of this selective wet etching, future studies can explore growing an etch stop material that completely covers the overgrowth but only partially covers the parasitic growth, such that the wet etchant can selectively etch the parasitic growth. The two-terminal magneto-transport measurement provides a simple yet comprehensive material characterization technique that avoids the unreliability of fabricating multiple contacts on a small nanostructure. In addition, it circumvents common issues in field effect measurements of nanostructures such as gate dielectric leakage, knowledge of the gate dielectric, and thickness that complicates mobility estimates.

IV. CONCLUSION

In summary, we extracted important material parameters in CELO by fabricating two-terminal devices to perform electrical measurements in magnetic fields up to 14 T. The low-temperature magneto-transport measurements showed Shubnikov–De Haas oscillations in the longitudinal resistance of these nanostructures from which doping concentrations were extracted. The dopant incorporations were found to be comparable to the values measured from planar InGaAs growths. We demonstrated how growth variabilities from different growth runs with similar parameters can be revealed using these measurements. We also extracted effective mass, carrier scattering lifetimes, and quantum mobilities from the temperature dependence of SdH oscillations revealing the presence of a high density of defects in the grown nanostructures. This was made possible by the gentle wet etch process that removes micrometers of parasitic growth in InGaAs CELO, without affecting the nanostructures of interest. Even for samples that had alignment marks completely covered by parasitic growth, the parasitic growth removal procedure allowed us to achieve perfect alignment of vias and fabricate contacts on these nanostructures. This, combined with the low-temperature two-terminal magneto-transport measurements, is an extremely powerful approach to characterize material parameters for CELO samples containing parasitic growths. The mechanism outlined here can be extended to the investigation of interesting physics in nanostructures of a broad range of other semiconductors, metals, and topological materials.

SUPPLEMENTARY MATERIAL

See the supplementary material for the following information: (S1) Current voltage sweeps at different temperatures from 300 to 2 K and resistance vs temperature measurements for CELO InGaAs samples. (S2) Signatures of weak localization in longitudinal

magnetoresistance at different temperatures (2–50 K) are shown. (S3) Alignment issues during fabricating devices directly from samples with parasitic growths.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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