A 200 GHz InP HBT Direct-Conversion LO-Phase-Shifted Transmitter/Receiver with 15 dBm Output Power

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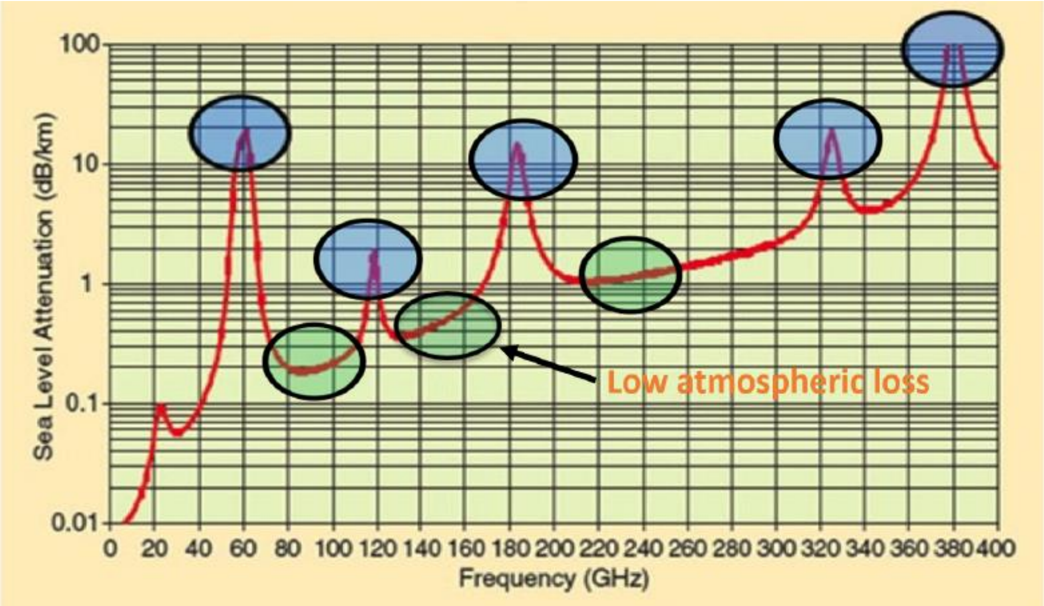
Outline

- Motivation
- Overview
- Transceiver circuit design
- Measured results
- Summary

Wireless Communication @ 200 GHz

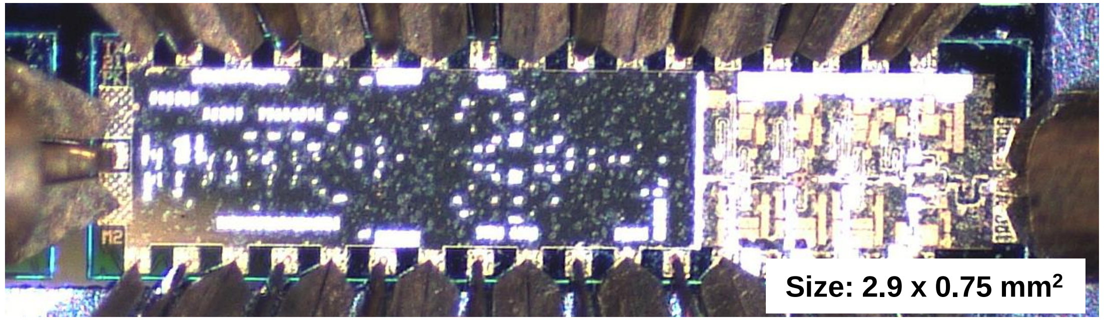


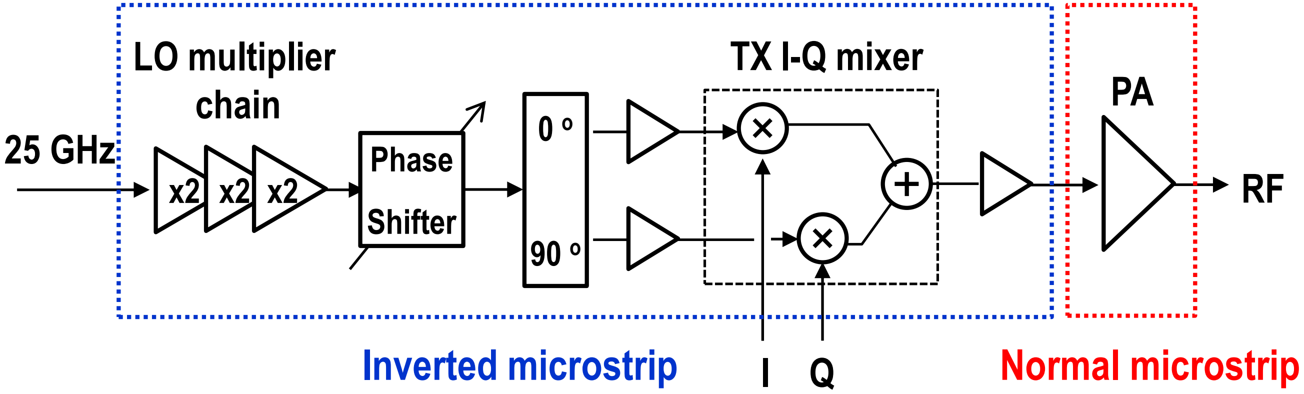
- **Motivation**
  - Large available BW → High data rate (6G)
  - Low atmospheric loss @ 200 GHz band
- **Challenges**
  - Short wavelength → High path loss
  - Low transistor gain → Low efficiency → Low battery life
- **Proposed 200 GHz transceiver**
  - InP-HBT → High P_{out} & high efficiency
  - Mixed use of normal & inverted microstrip
  - Integrated LO phase shifter → Phased-array

Normal microstrip	Inverted microstrip
1.1 dB/mm @200GHz 🙂	2.5 dB/mm @200GHz ☹
Ground holes ☹	Continuous GND 🙂
PA & LNA	High-density blocks

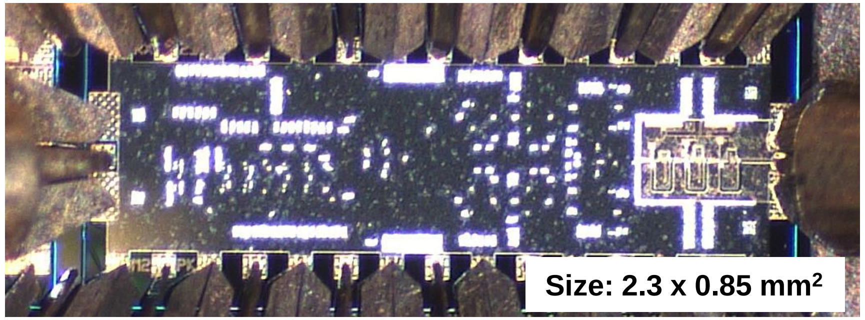
Proposed 200 GHz Transmitter / Receiver

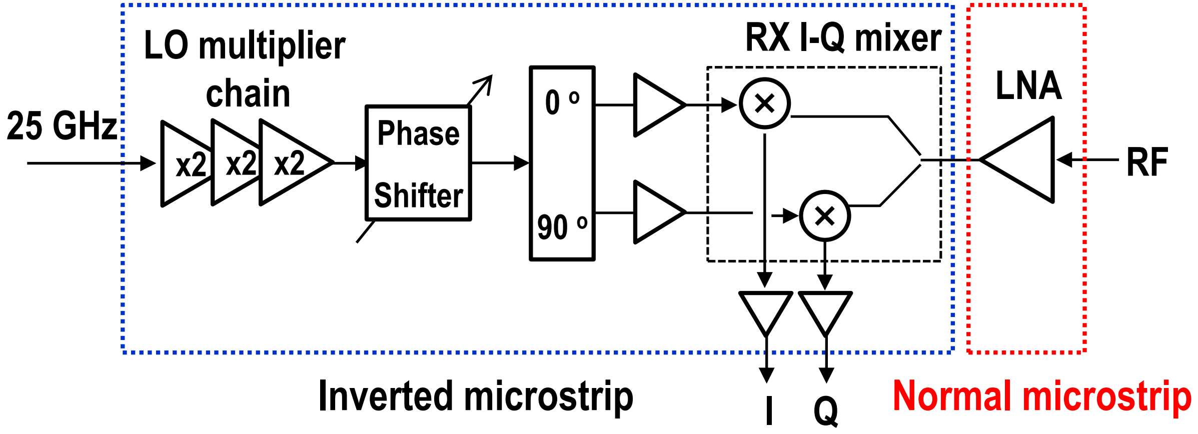
200 GHz direct-conversion TX





200 GHz direct-conversion RX

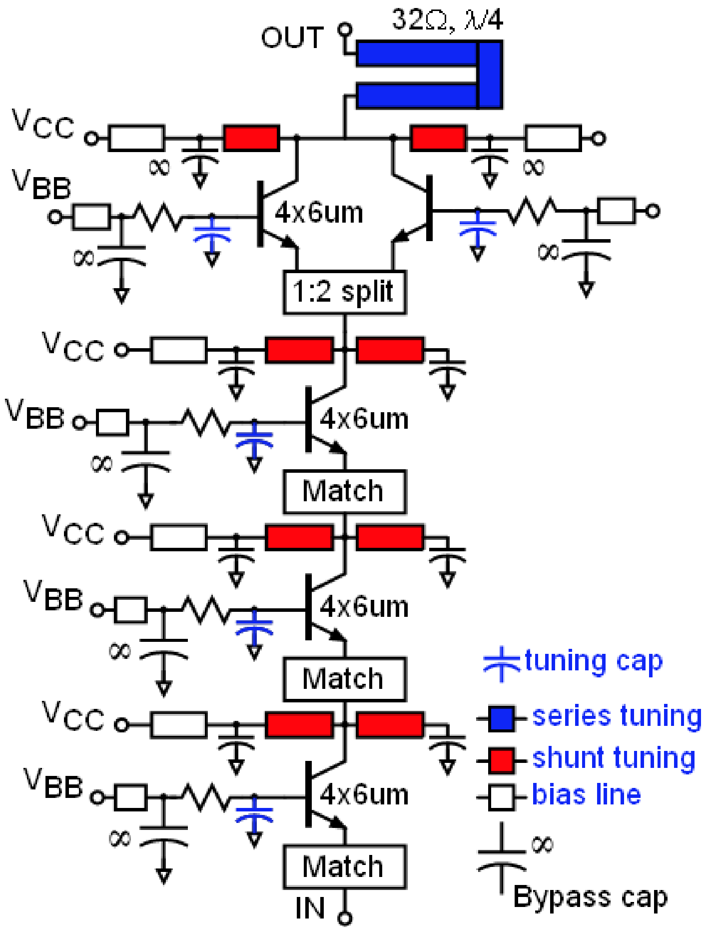




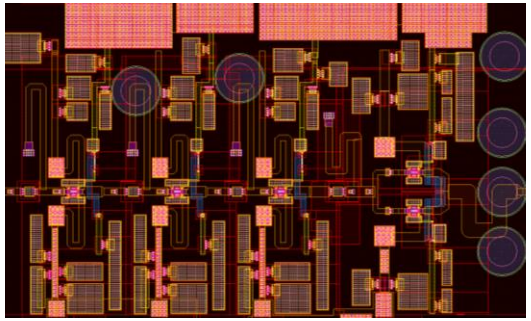
- PA & LNA: Normal microstrip for best PAE and lowest NF
- Mixer, LO multiplier, phase shifter: Inverted microstrip for low-inductance ground
- Integrated LO phase shifter enables phased-array operation of multiple ICs

200 GHz PA Design

PA schematic



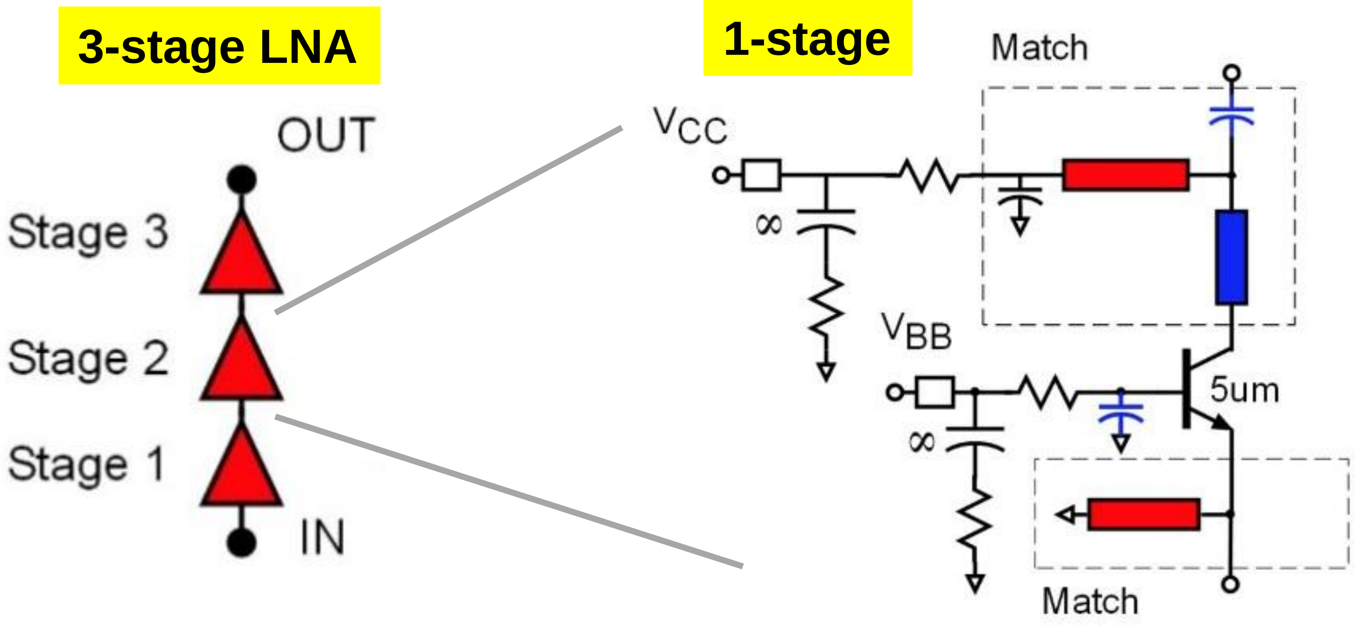
PA layout

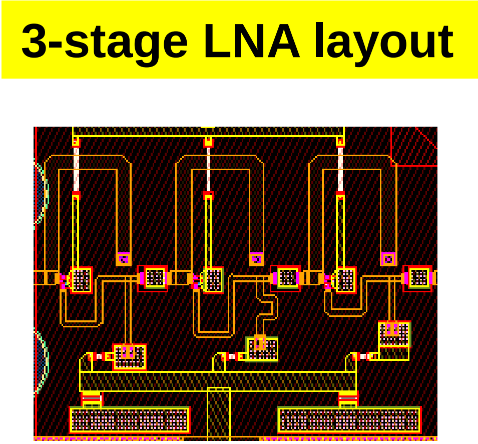


Size: 850 x 550 μm²

- 4-stage common-base w/ C_{base}
  - Higher efficiency @OP1dB than common-emitter
  - Higher efficiency @OP1dB than common-base with no C_{base}
- Low-loss 2:1 combiner w/ a single λ/4 line & shunt L
- Sim: P_{sat} = 17dBm@200GHz, S_{21} > 20dB, P_{DC} = 450mW

200 GHz LNA Design



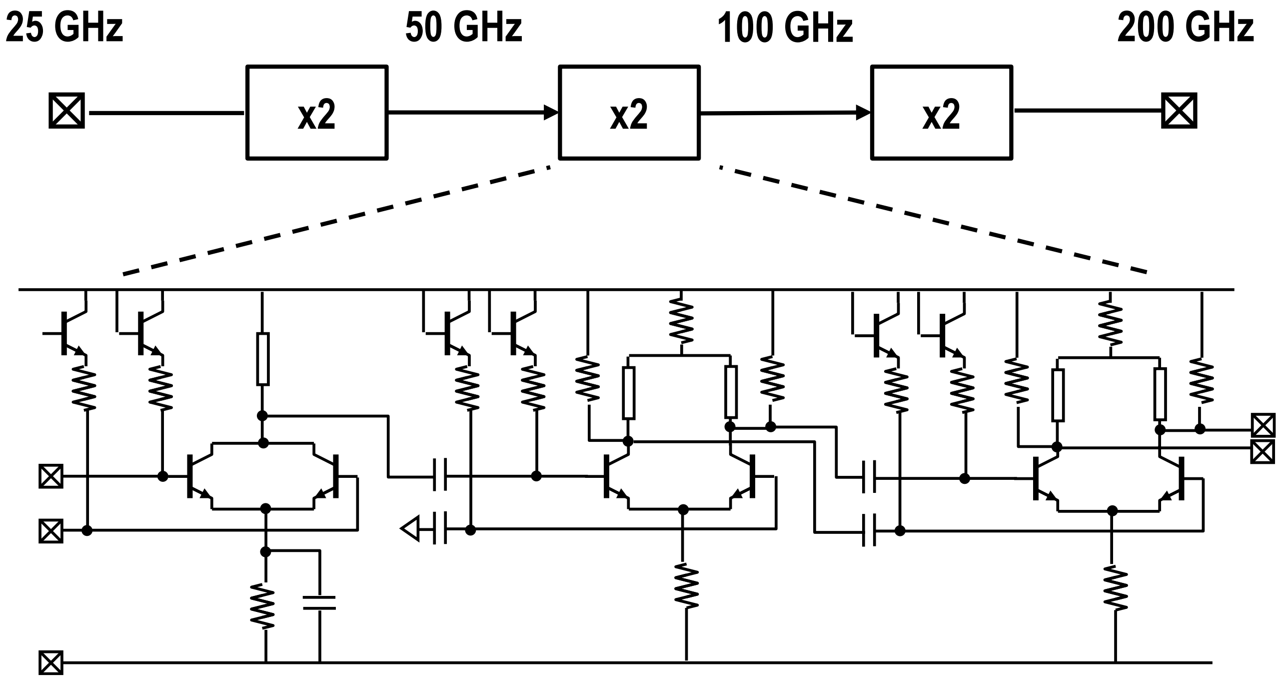


Size: 350 x 250 μm²

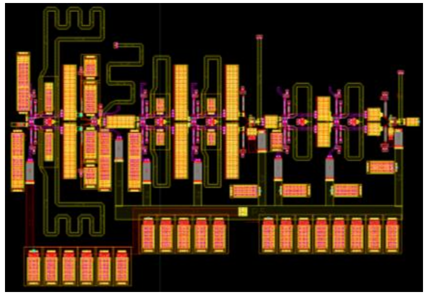
- 3-stage common-base (CB)
- Base cap. adjusted for simultaneous noise & S_{11} matching
- Emitter length scaled for minimum input matching loss
- Simulation: S_{21} = 15dB, 3-dB BW = 35GHz, P_{DC} = 14mW

LO Frequency Multiplier Design

x8 LO multiplier schematic



Multiplier layout

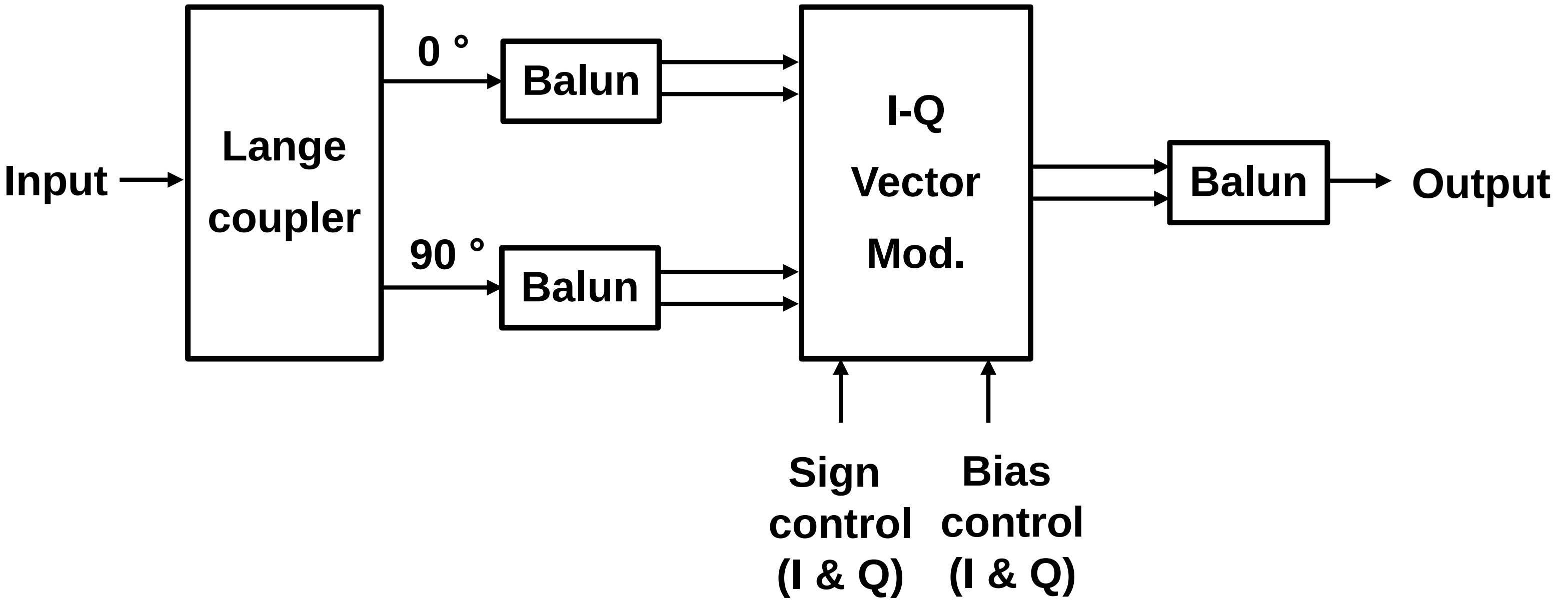


Size: 580 x 400 µm²

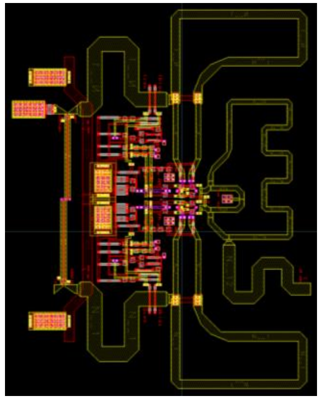
- Cascade of three push-push doublers → x8 LO multiplier
- Capacitive emitter degeneration → Operates with wider ranges of P_{in}
- Simulation: P_{out} > 0dBm for 180-230GHz (BW = 50GHz), P_{DC} = 250mW

200 GHz LO Phase Shifter

Phase shifter schematic



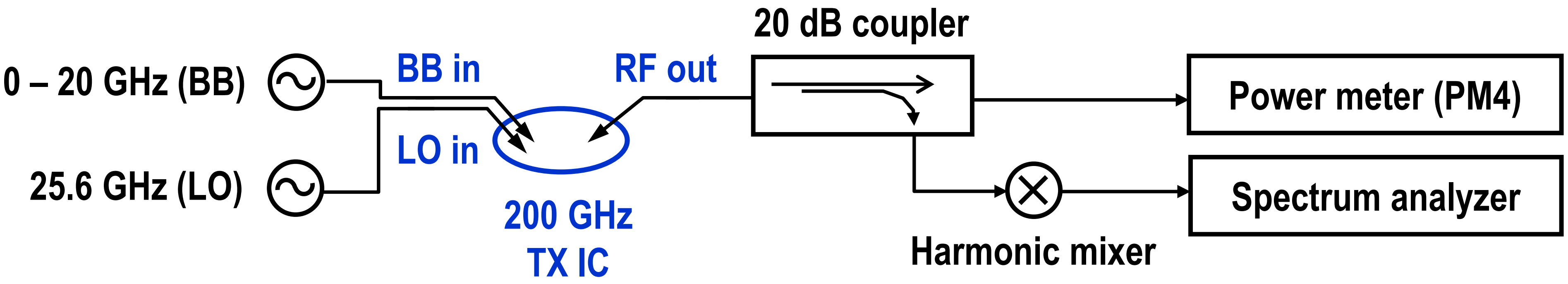
Phase shifter layout

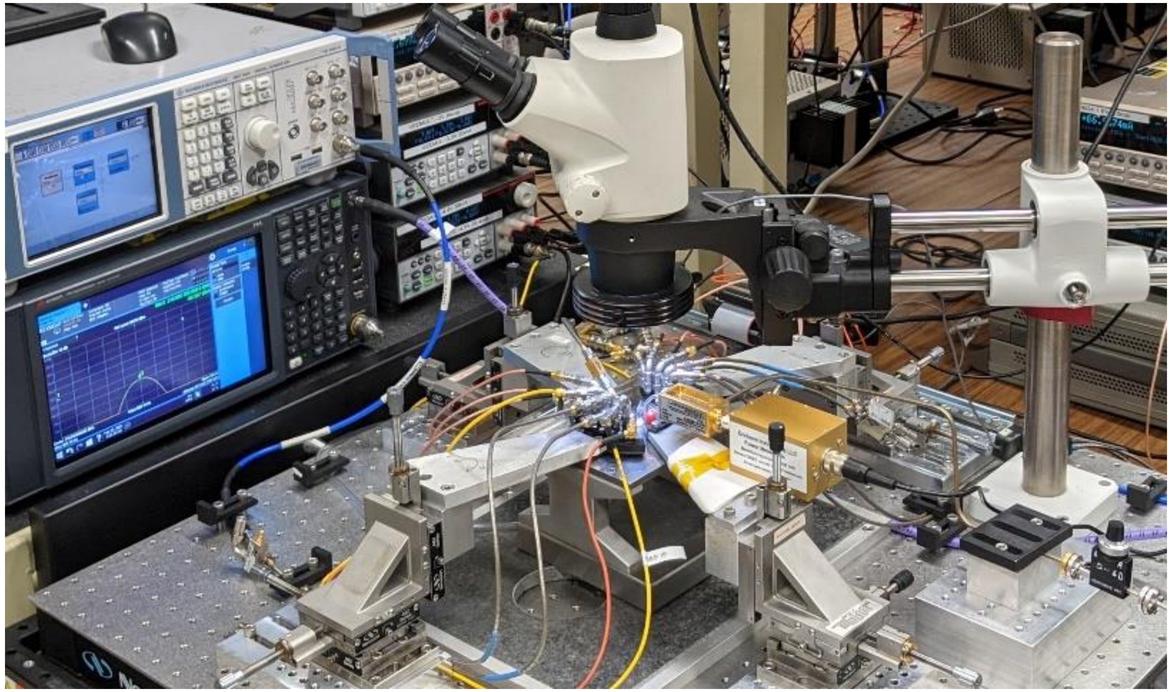


Size: 300 x 400 μm²

- Vector-modulator-based phase shifter
- Wideband operation by using Lange coupler
- Sim: I/Q phase error < 2deg, mag. error < 0.3dB for 170-250GHz, P_{DC} = 100mW

Transmitter Testing Setup

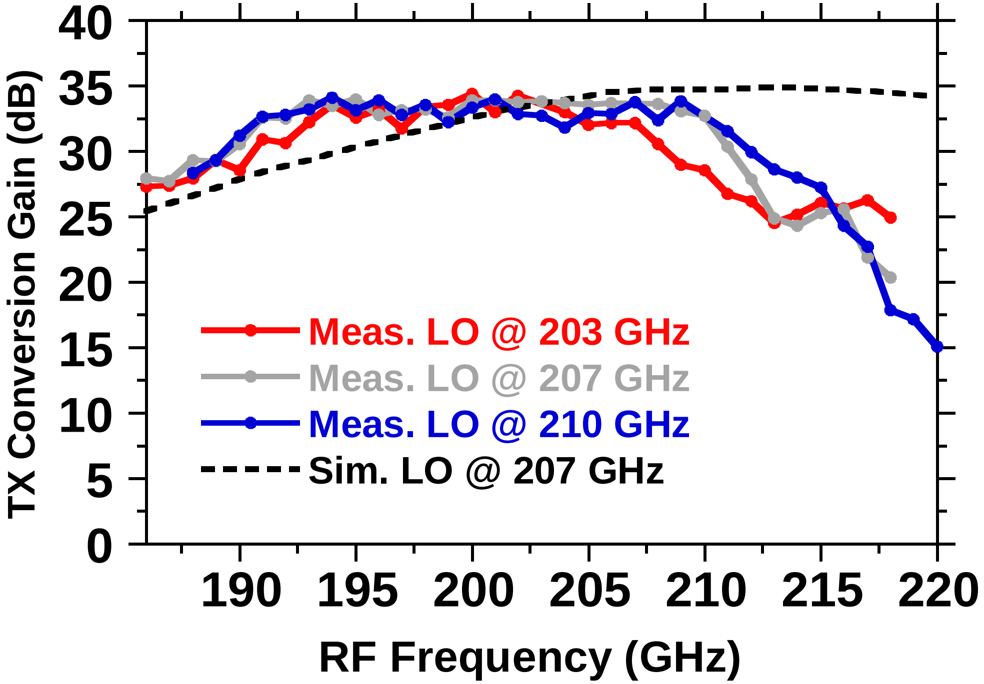




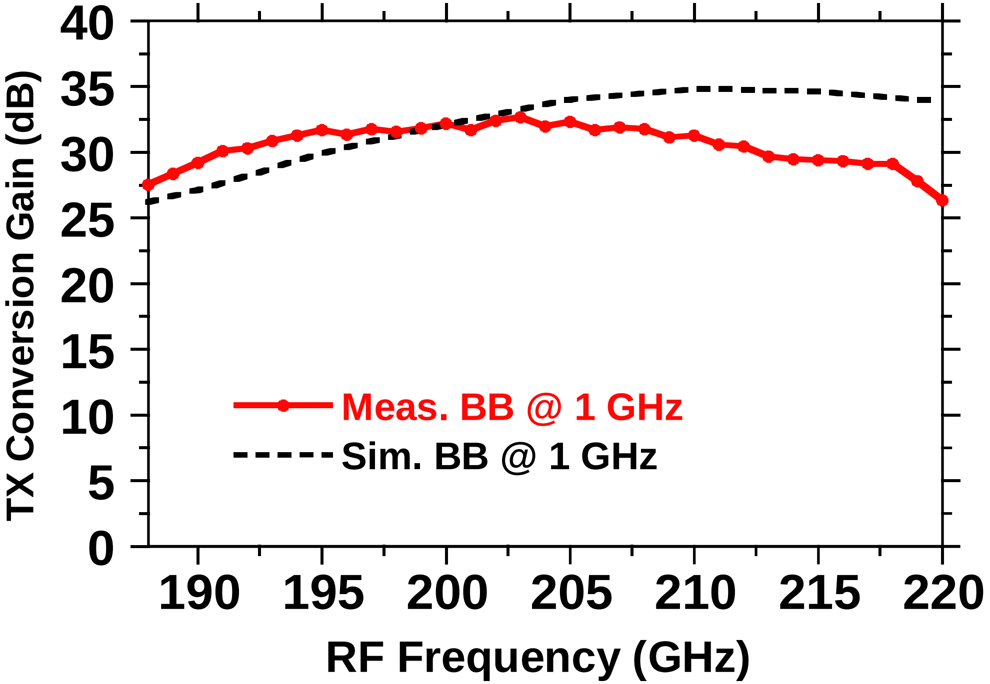
- 140-220 GHz (WR5) on-wafer testing
- Simultaneous freq. & power testing
- TX used as a calibration reference

Measured TX Conversion Gain

Conversion Gain @ fixed f_{LO}



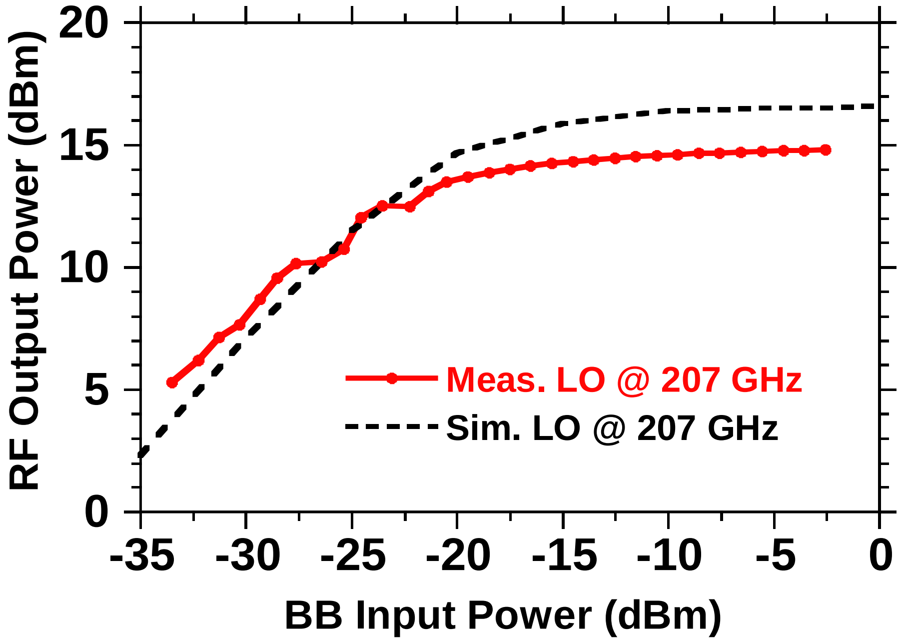
Conversion Gain @ fixed f_{BB}



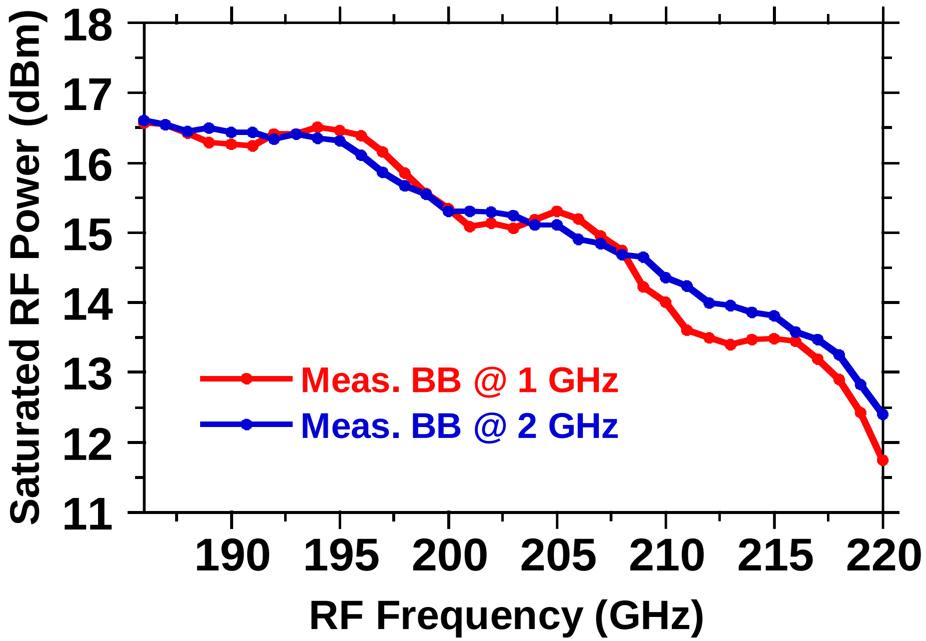
- Peak conversion gain = 34 dB
- 3-dB bandwidth > 20 GHz
- LO multiplier tuning bandwidth > 30 GHz

Measured TX Output Power

P_{out} vs P_{in} @ f_{LO}=207 GHz (f_{BB}=1 GHz)

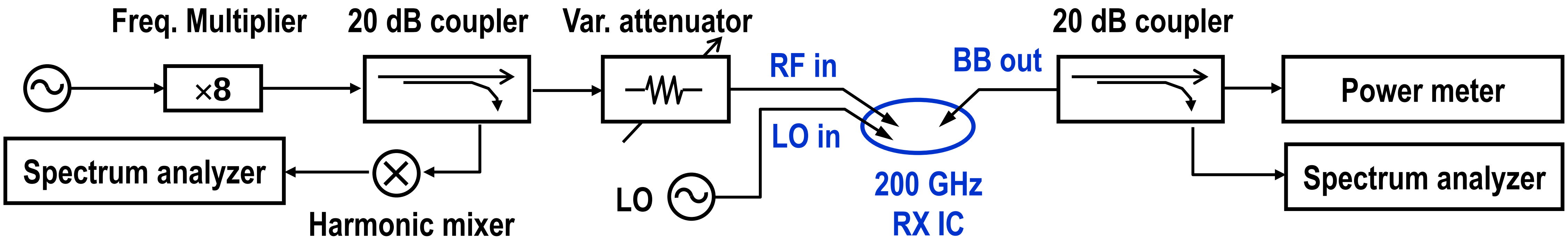


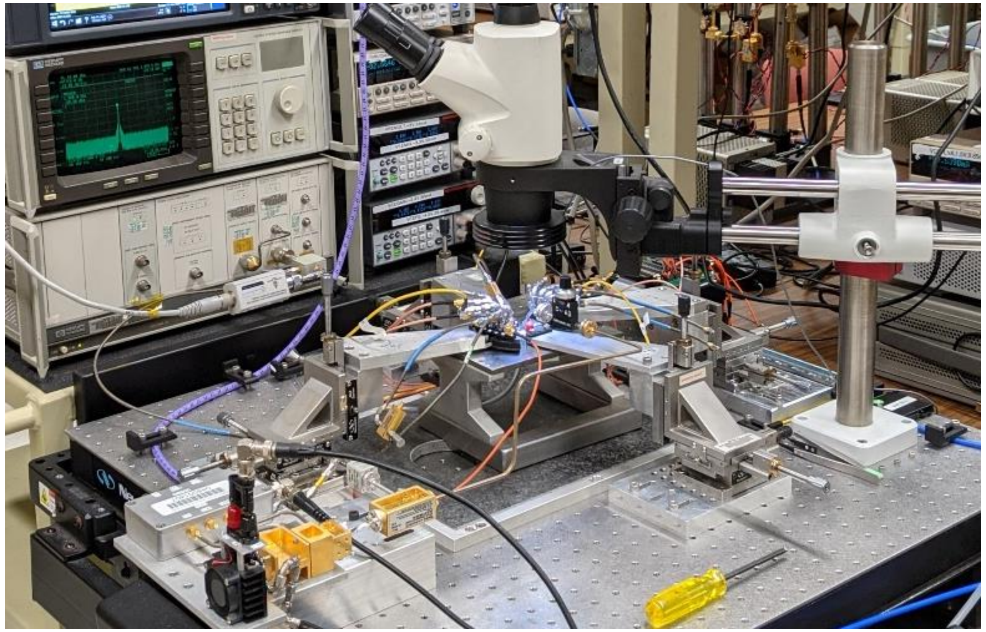
P_{sat} vs f_{RF}



- P_{sat} = 16.5 dBm @ f_{RF} = 195 GHz, 15.3 dBm @ f_{RF} = 200 GHz
- P_{DC} = 1,250 mW

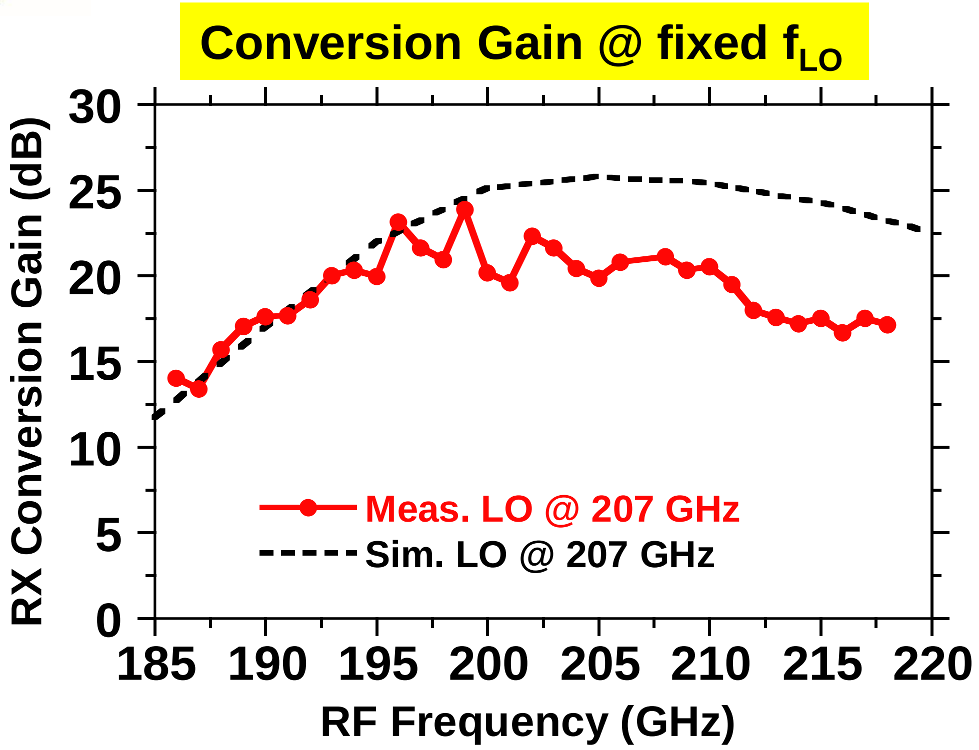
Receiver Testing Setup

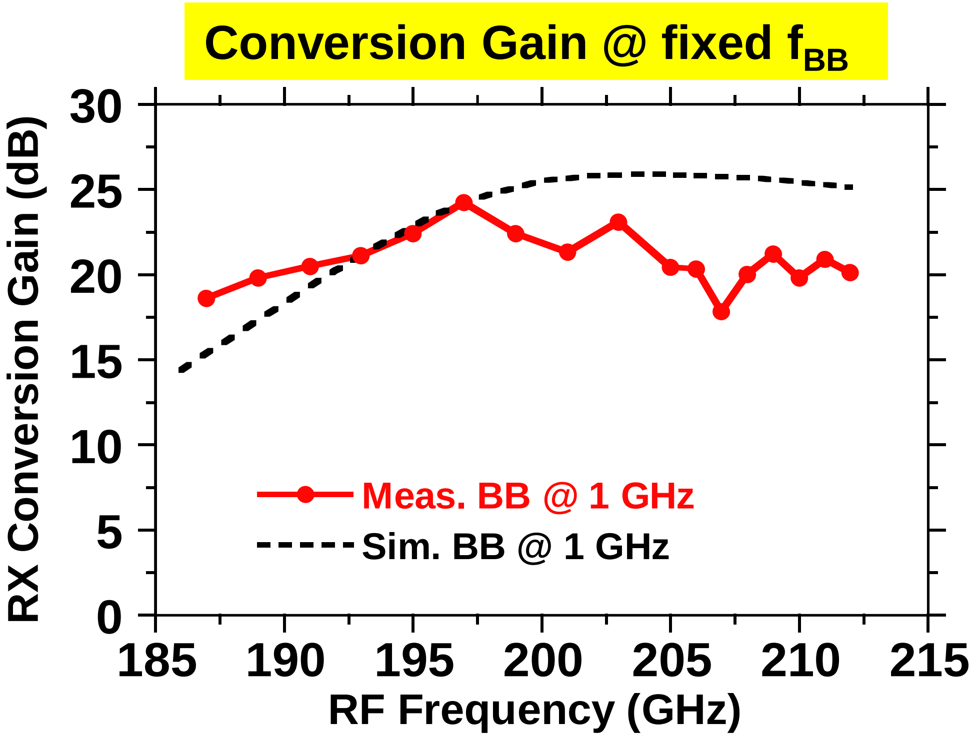




- 140-220 GHz (WR5) on-wafer testing
- Simultaneous freq. & power testing
- RX driven by multiplier & variable attenuator

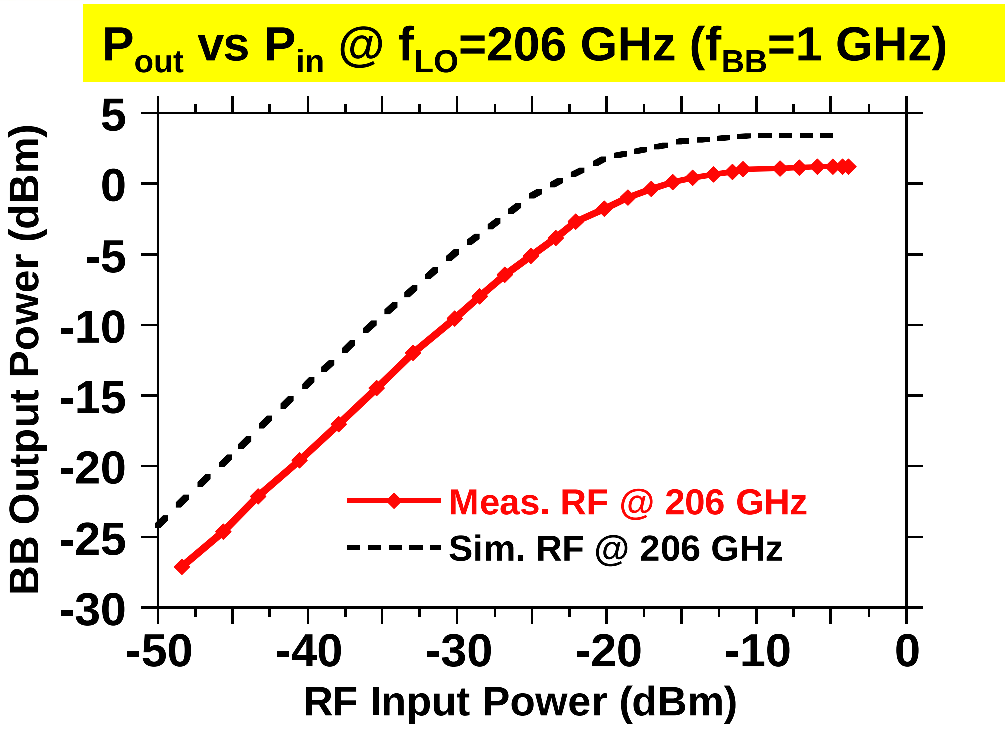
Measured RX Conversion Gain



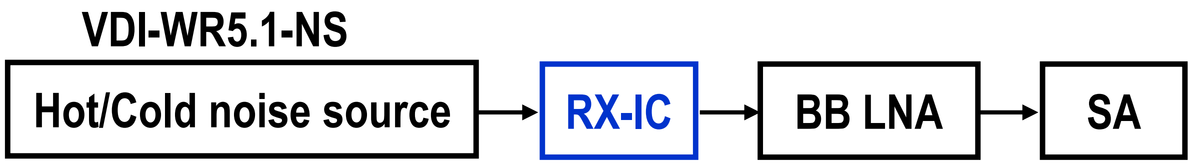


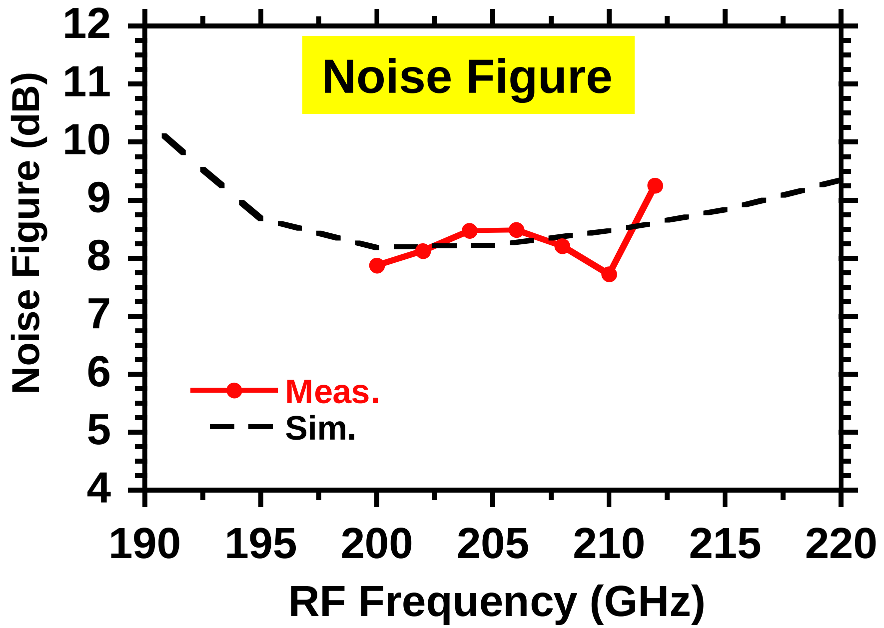
- Peak conversion gain = 25 dB
- LO multiplier tuning bandwidth > 25 GHz

Measured RX Power & Noise Figure



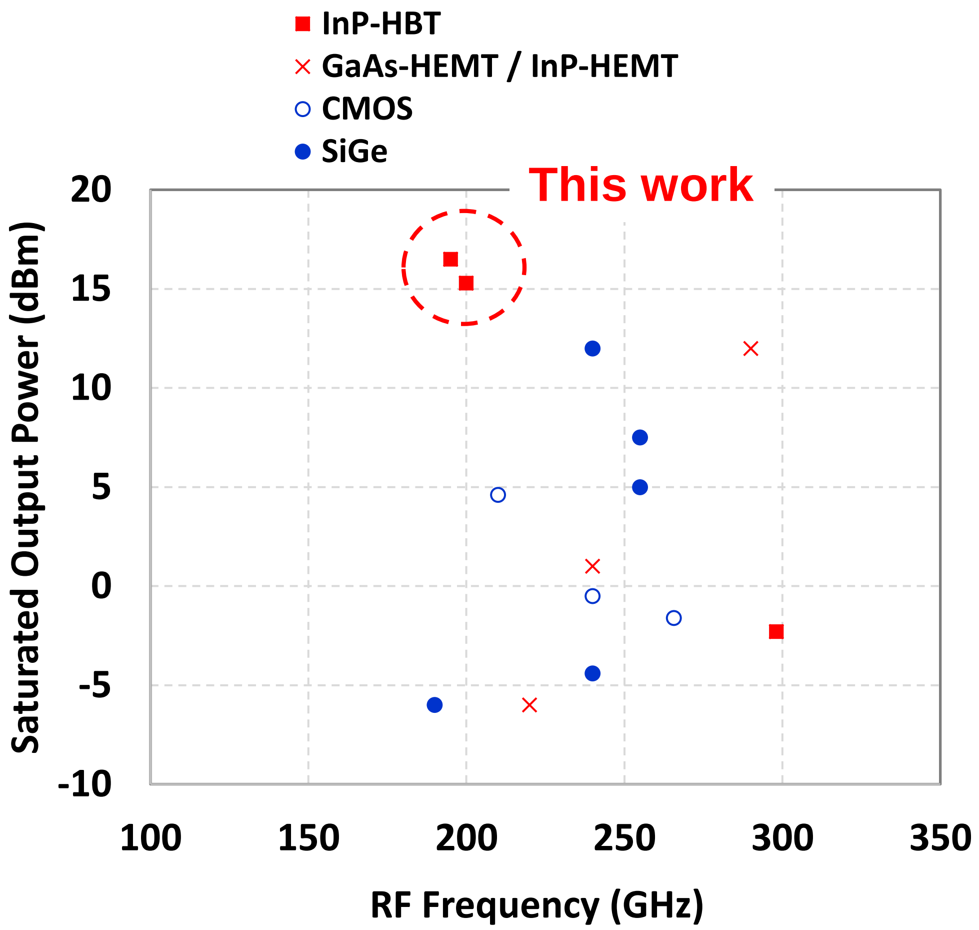
- Input P_{1dB} = -24 dBm
- P_{sat} = +1 dBm
- P_{DC} = 825 mW

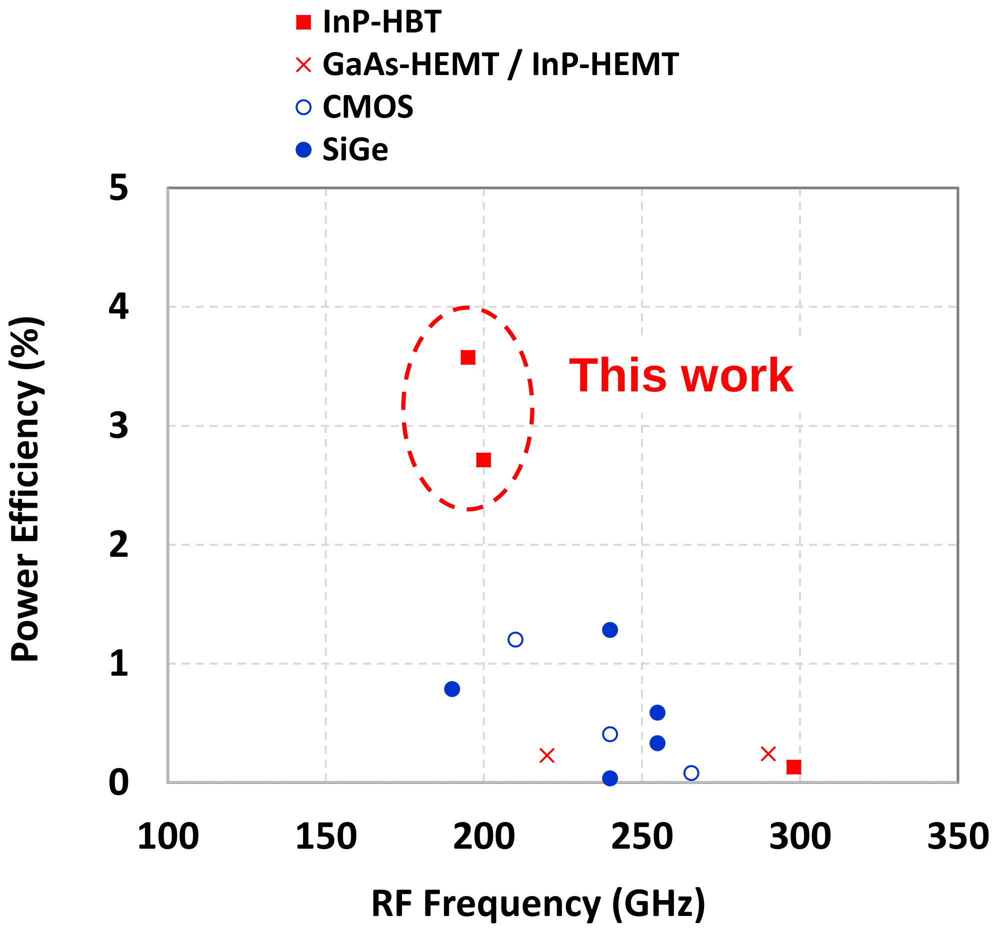




- NF = 7.7 – 9.3 dB (200-212 GHz)

Performance Comparison of Transmitter





$$\left(\text{Power efficiency} = \frac{P_{sat}}{P_{DC}}\right)$$

Summary

- 200 GHz direct-conversion transmitter / receiver in InP HBT
- Highest P_{out} and efficiency, among all integrated TX beyond 200 GHz
- Modulated testing is under way

Acknowledgement

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Thank you very much!

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Performance Comparison

Ref.	Technology	Integrated TX circuit blocks	Freq. (GHz)	P_{sat} (dBm)	P_{DC} (mW)	Efficiency (%)
[2]	0.1µm GaAs mHEMT	IF-mixer, LO multiplier (×2), PA, antenna	220	-6	110	0.23
[3]	50nm GaAs mHEMT	IF-mixer, PA	240	1	N/A	N/A
[4]	32nm SOI CMOS	LO VCO, OOK mod, PA, antenna	210	4.6	240	1.20
[5]	65nm CMOS	IQ-mixer, tripler	240	-0.5	220	0.41
[6]	250nm InP-HBT	IF-mixer, LO driver, LO oscillator	298.1	-2.3	452	0.13
[7]	130nm SiGe	IQ-mixer, LO multiplier (×16), PA	240	-4.4	1,033	0.04
[8]	130nm SiGe	Mixer, LO driver, antenna	190	-6	32[1]	0.78
[9]	40nm CMOS	IQ-mixer, LO multiplier (×3)	265.68	-1.6	890	0.08
[10]	130nm SiGe	IQ-mixer, LO multiplier (×16), PA	220-255	5	960	0.33
[11]	130nm SiGe	IQ-mixer, LO multiplier (×16), PA	225-255	7.5	960[2]	0.59
[12]	130nm SiGe	IQ-mixer, LO multiplier (×8), PA	240	12[4]	1,237	1.28
[13]	80nm InP-HEMT	IF-mixer, LO driver, PA[3]	290	12	6,600	0.24
This work	**250nm InP-HBT**	**IQ-mixer, LO multiplier (×8), phase shifter, PA**	**195**	**16.5**	**1,250**	**3.57**
			200	**15.3**	**1,250**	**2.71**

[1]P_{DC} not including LO generator at 190 GHz **[2]P_{DC} for 1-channel I-Q TX+LO** **[3]Individually packaged, not integrated** **[4]Measured from PA breakout**