A 2-stage, 140-GHz Class-B Power Amplifier Achieving 22.5% PAE at 17.3 dBm in a 250-nm InP HBT Technology

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***Abstract*— We demonstrate a 140-GHz class-B power amplifier (PA) in a 250-nm Indium Phosphide (InP) technology achieving saturated output power of 17.3 dBm with power-added efficiency (PAE) of 22.5%. This two-stage PA design offers more than 10-dB gain using a pseudo-differential topology with base degenerated common-base transistor cells. The power combining and impedance matching are performed with an electrically-short coupled-line balun to provide low impedance at all harmonics.**

***Keywords*— power amplifier, millimeter-wave, D-band, Indium Phosphide, power-added efficiency**

I. Introduction

Next generation millimeter-wave communication and radar systems are focusing on operation in upper millimeter-wave bands above 100 GHz to support higher data rates and improved radar resolution while maintaining comparable high efficiency. In a D-band communication system, the antenna elements are spaced roughly 1 mm and the PA power dissipation greatly impacts the thermal load. Consequently, the efficiency of the PA becomes particularly important above 100 GHz. While silicon based technologies, e.g. SOI and SiGe, offer solutions for large scale integration, the efficiency and output power is constrained due to lower breakdown voltage. Several III-V technologies with high f_{max}/f_T such as Indium Phosphide (InP), Gallium Nitride, and Gallium Arsenide are prime candidates for high power and efficiencies above 100 GHz.

InP has excellent potential for high efficiency because it offers a loadline near 50 Ohms for roughly 15-dBm output power and f_{max}/f_T of about 600/350GHz when biased at a current density of 2 mA/um [1]. Previous work has demonstrated class-B PAs using a 250-nm InP HBT to achieve a power-added efficiency (PAE) of 32% for a single stage PA with a saturated output power (P_{sat}) of 15.3 dBm at 130 GHz [2]. Other work in InP at 140 GHz also show a higher P_{sat} of 20.5 dBm while maintaining a high peak PAE of 20.8% [3]. InP power amplifiers above 200 GHz have also been shown in literature [4]–[6]. In comparison, recent work have presented a 17.6 dBm P_{sat} SiGe PA with 17.5% PAE and a 17.5 dBm PA in 45-nm SOI with 14.2% PAE [7], [8].

This work demonstrates high-efficiency with higher gain (greater than 10 dB) and power than prior work. A 2-stage, class-B PA design is proposed for high efficiency in a pseudo-differential topology using low-loss, compact baluns based on short-section coupled lines. In the next section, the design of the class-B power amplifier is discussed, showing performance of a capacitively-degenerated common-base cell and design of the output balun. Harmonic tuning for class B operation is presented. Section III presents measurements of the InP PA.

II. Class-B Power Amplifier Design

A. Device Cell

A common-base (CB) heterojunction bipolar transistor (HBT) was used for higher gain relative to common-emitter (CE) transistors in spite of equivalent f_{max}. The maximum available gain (MAG) for different 4x6μm device configurations is plotted in Fig. 1 with devices biased for class-B operation (200μA/μm). At 140 GHz, the CB has a MAG of 11.9 dB compared to the CE with a MAG of 5.7 dB. Typically, the base of the CB HBT is grounded with a small inductance [2]. However, this choice requires the use of a negative bias on the emitter and prevents design tradeoffs between gain and 1dB compression.

Instead of a grounded base, the approach presented here uses a finite base capacitance of 480 fF to degenerate the base impedance in the output stage. Since the base capacitance is (ideally) lossless, the base feedback does not reduce PAE. The MAG of the common base with feedback post-layout is also

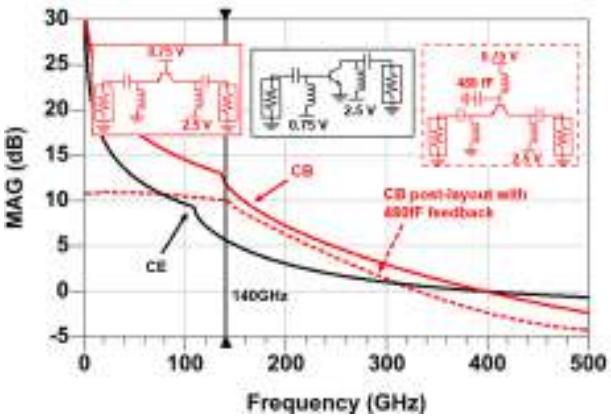

Fig. 1. MAG of 4x6μm HBT biased at 200$\mu A/\mu m$ for common base, post layout with feedback and common emitter. Note that the quiescent bias is reduced for class-B operation at the expense of f_{max}.

shown in Fig. 1 with a MAG of 10 dB at 140 GHz. The layout of the cell is shown on Fig. 2.

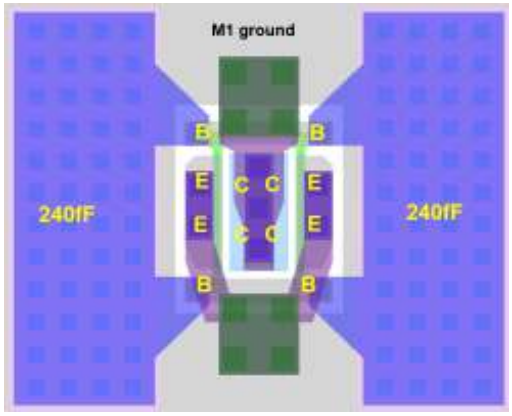

Fig. 2. Layout of 4x6μm device with base capacitance of 480fF.

Since the HBT dissipates significant power, the temperature rise due to heat dissipation can lead to thermal instability, where the temperature rise in the emitter creates a positive thermal feedback that increases the emitter current until device destruction. This can make class-B biasing difficult since the device might be forced into another class of operation. To mitigate this effect, a base ballast resistor of about 80 Ω is added to compensate for the thermoelectric feedback. The base ballast resistor forces the base voltage to decrease with increasing input drive level due to the DC component of the half-wave rectified class-B waveform. As a consequence, the device voltage is biased in class-AB at 0.83 V or 1.17 mA/μm current density at backoff and compresses into class-B.

Loadpull simulations are performed with a base-emitter voltage of 0.75 V at $200 - uA/um$ current density and 2.5-V collector-emitter voltage using an ADS HBT model to find the optimum impedance presented for the fundamental frequency. The constant efficiency and output power loadpull contours are shown in Fig. 3 with a peak PAE of 44.6% and output power of 14.4 dBm. The optimum load for PAE is presented to be about 6.2+j26 Ω.

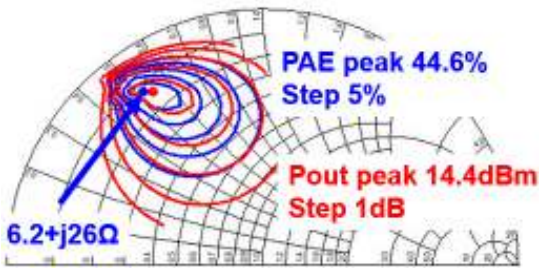

Fig. 3. Loadpull simulation of the PAE and output power of the 4x6μm common base with base capacitance of 480fF.

B. Output Balun Design

A pseudo-differential topology requires a balun at the output and input. With careful design , the balun can simultaneously provide impedance matching and power combining at the output, enabling low-loss solutions for PA design. Additionally, the balun offers an opportunity to tune harmonics in a pseudo-differential circuit for class-B operation.

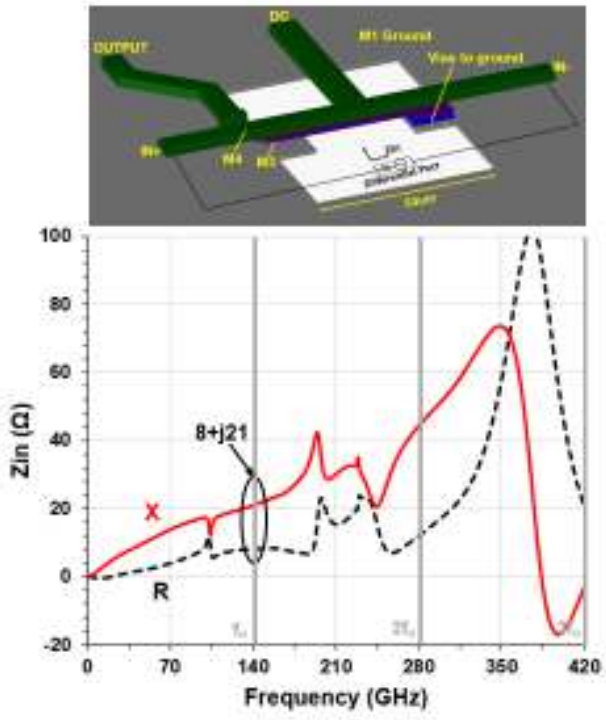

Fig. 4. Short-section coupled-line balun structure

Due to the intrinsic and parasitic capacitance at the collector, the load presented is located at the top left of the Smith chart, implying that the output combiner should present an impedance that is the $R_{loadline}$ in parallel with a shunt inductance of about 35 pH. This work presents a short-section coupled-line balun that achieves both the impedance match as well as 180° power combining. The balun is designed with three metal layers with the coupled line on the thickest metal layers M4 and M3 and a ground layer M1. The coupled line is compact at a length of 54μm and maintains less than 10° phase imbalance and 1-dB amplitude imbalance with insertion loss of 0.82 dB.

The balun structure is shown on Fig. 4. Similar structures have also been shown in previous work [9]. The input balun is designed similarly to the output balun but with added shunt capacitors at the input and output for impedance matching as shown on the circuit diagram on Fig. 6.

The differential impedance presented by the balun to the collector is plotted in Fig. 4 and indicates that the real part of the input impedance is relative small at the fundamental as well as the second and third harmonics. The reactance is absorbed by the output capacitance of the transistor. The collector waveforms are plotted in Fig. 5 as the PA compresses near peak efficiency. The role of the 3rd harmonic helps produce peaking in the current waveform.

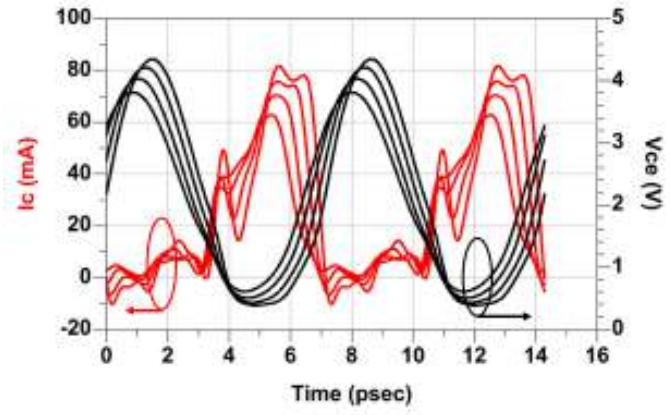

Fig. 5. Class-B collector current and voltage behavior for Pin = 7 to 10 dBm with 1 dB steps

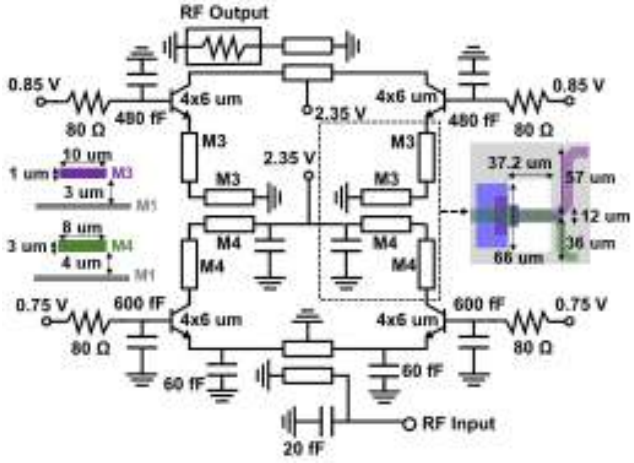

Fig. 6. Two-stage, class-B 140-GHz power amplifier circuit

III. Measurements

The PA was fabricated in a 250-nm Teledyne Scientific InP HBT process and occupies an area of 1.1x0.4 mm^2 as shown in Fig. 7. The S-parameter and power measurements were performed using a PNAX (N5247A) with VDI 110-170GHz frequency extenders and probed with D-band waveguide probes. The saturated output power of the frequency extenders is about 11 dBm at 140 GHz. Power calibration was performed using the Erickson PM5B power meter, measuring a probe loss of about 1.7 dB assuming similar losses for both probes. The S-parameters are measured with 0.75 V and 0.85 V base-emitter voltages for the first and second stages, respectively, and 2.35 V collector voltage.

The S21 at 140 GHz is 10.4 dB with a 3-dB bandwidth from 133 to 147 GHz. Compared to simulation, the S21 at 140 GHz is slightly higher and shifted down in frequency. The peak PAE shown on Fig. 9 is 22.5% with an associated output power of 17.3 dBm and gain of 8.4 dB. At an output power of 10.9 dBm, there is a noticeable drop in gain and efficiency due to the base ballast resistor shift in the bias of the output stage. Due to the lower gain of the first stage and limited saturated output power of the frequency extenders, the highest output power is measured to be about 17.3 dBm.

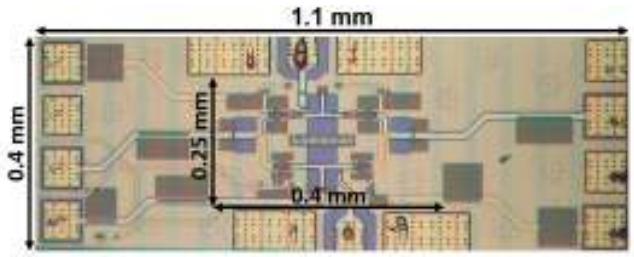

Fig. 7. Chip photo for 2-stage InP PA with a total area of 1.1x0.4 mm^2 and core area of 0.4x0.25 mm^2

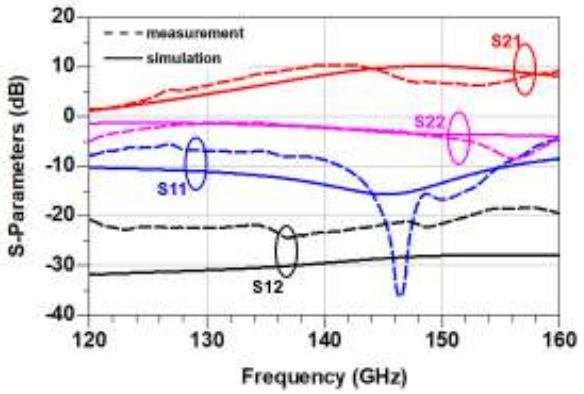

Fig. 8. S-parameters for measurement and simulation

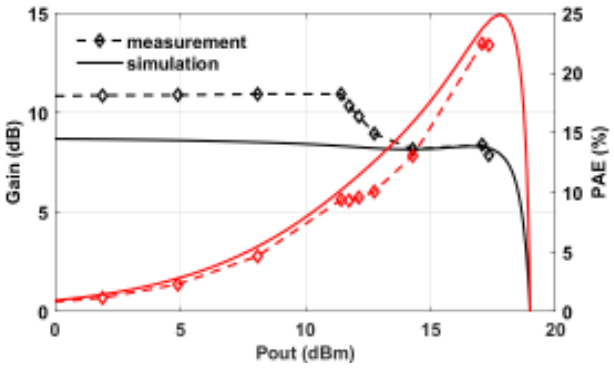

Fig. 9. Large-signal compression and PAE as a function of output power

IV. Conclusion

We present a two-stage amplifier with the highest efficiency for an amplifier at 140 GHz with gain greater than 10 dB. Due to the high-gain of the common base transistor, we demonstrate second and third harmonic tuning in the coupler to realize class-B operation. The peak PAE is 22.5% with an associated output power of 17.3 dBm and gain of 8.4 dB. To our knowledge, this is the highest PAE for a two-stage PA at 140 GHz.

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Table 1. Comparison between State-of-the-Art D-band PAs

Reference	Technology	Frequency (GHz)	Gain (dB)	Psat (dBm)	PAE (%)	Chip Area (mm^2)
This work	**250nm InP HBT**	**140**	**8.4**	**17.3**	**22.5**	**0.44 / 0.1***
[2]	250nm InP HBT	118-148	7	15.3	32	0.2
[3]	250nm InP HBT	125-150	12.3-15.9	18.9-20.5	14.3-20.8	0.69
[7]	45nm CMOS SOI	140	24	17.5	13.4	0.43*
[8]	55nm SiGe	135	24	17.6	17.5	0.18
			22.4	19.3	13	0.26
[10]	130nm SiGe	161	30.7	18.1	12.4	0.42

*core area

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