A Fully Packaged 135-GHz Multiuser MIMO Transmitter Array Tile for Wireless Communications

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***Abstract*— We report a packaging approach for building mm-wave massive multiple-input–multiple-output (MIMO) transmitter arrays in tiles. A single-channel 135-GHz transmitter, having a 22-nm fully-depleted (FD)-silicon on insulator (SOI) CMOS IC for baseband-RF conversion, an InP HBT power amplifier, and a linear microstrip patch antenna array, all packaged on a low-permittivity ceramic interposer (Kyocera GL771, $\varepsilon_r = 5.2$ and $\delta = 0.003$), had 27.5-dBm measured effective isotropic radiated power (EIRP) at saturation and showed 8.5% error vector magnitude (EVM) during 30-Gb/s, 64 quadratic-amplitude modulation (QAM) transmission. An eight-channel transmitter MIMO array tile module constructed on an low-temperature-cofired ceramic (LTCC) interposer, with the same antennas and ICs, after calibration and under the control of a field-programmable gate array (FPGA), had 38.5-dBm measured EIRP at saturation and showed −13-dB EVM in 1.92-Gb/s 16 QAM transmission. Steerable two-simultaneous beam transmission was demonstrated at 34-dBm peak EIRP per beam.**

***Index Terms*— Ceramic interposer, *D*-band antenna, *D*-band transmitter, heterogeneously integrated transmitters, low-temperature-cofired ceramic (LTCC) carrier, massive multi-in–multi-out (MIMO) arrays, millimeter-wave packaging, MIMO tiles, multiuser MIMO arrays.**

I. Introduction

THE rapid growth in wireless communications and the emergence of high-rate media formats [high definition (HD)/ultra HD (UHD), 360 videos, and augmented reality (AR)/virtual reality (VR)] has saturated the spectrum allocated for 4G systems, and industry is moving to 5G, with carriers at sub-6, 28, 38, and 71–86 GHz [1]; further increase of mobile data traffic is anticipated [2]. The 100–300-GHz links can provide very high capacity, because of the wide spectrum and because, given the short wavelengths (λ), compact arrays can have many elements and hence can simultaneously transmit or receive many independent signal beams, i.e., can support massive spatial multiplexing.

Between 100 and 300 GHz, worst case atmospheric attenuation and λ^2/R^2 Friis path losses are high. Reliable, high-capacity communication links of even 50–500-m range must use either highly directional antennas in fixed-aimed links or, for systems needing steerable beams, arrays having many elements. Improved receiver noise figure or transmitter RF output power reduces the number of necessary array elements.

D-band transmitters have been reported in both CMOS [3] and III–V [4] technologies. Reported packaged *D*-band (110–170 GHz) transmitters and receivers include a 142–157-GHz GaAs mHEMT single-channel transmitter on a silica substrate with 8-dBm P_{sat} and 3.5-dB measured packaging loss [5], a 135–170-GHz SiGe BiCMOS single-channel transmitter on a glass interposer with 13-dBm peak output power and 1-dB packaging loss [6], an eight-channel single-beam transmitter array on a quartz substrate with 32-dBm effective isotropic radiated power (EIRP) [7], a two-channel single-beam transmitter on a high-performance printed circuit board (PCB) with 20-dBm EIRP [8], and a link using 4- and 16-element transmitter/receiver arrays on a low-cost PCB with a 6-Gb/s peak data rate [2]. Here, we report eight-element, 135-GHz multi-in–multi-out (MIMO) transmitter array tile modules. This work is an extension of our single-channel *D*-band transmitter reported in [9] and complements our eight-channel *D*-band receiver reported in [10].

II. Massive MIMO Array Architecture

The eight-channel tile modules are designed for use in sets to form a 32-element or larger MIMO horizontal linear transmitter array [Fig. 1(a)] that scans transmitted beams horizontally, simultaneously sending independent signal beams to multiple mobile users. The arrays are designed for use with MIMO digital beamforming [11]–[14], which, from the array's IQ input–output signals, determines the data and direction of a set of transmitted signal beams. MIMO digital beamforming arrays can form many independent signal beams as the number of independent array signal channels; in contrast, arrays using RF phase shifting [15] can only produce one signal beam per array.

The transmitter array tile module [Fig. 1(b)] contains an low-temperature-cofired ceramic (LTCC) carrier with eight

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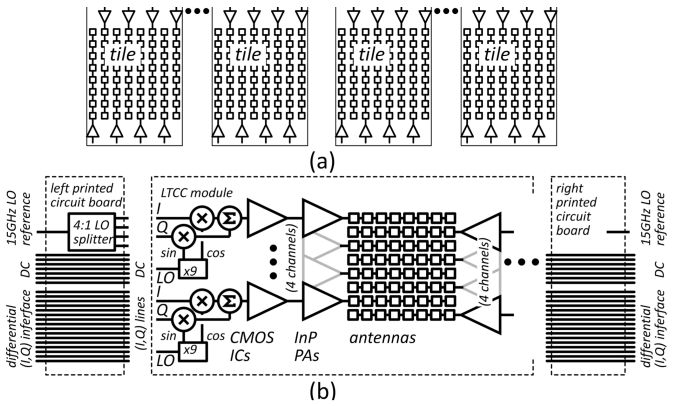


Fig. 1. Spatially multiplexed (MIMO) transmitter (a) network hub MIMO arrays formed from eight-element transmitter tile modules. (b) Each transmitter module contains an LTCC carrier with eight transmitter channels, each having a linear microstrip patch antenna array, a CMOS frequency upconversion IC, and an InP HBT PA IC, plus two PCBs providing baseband signal and dc connections.

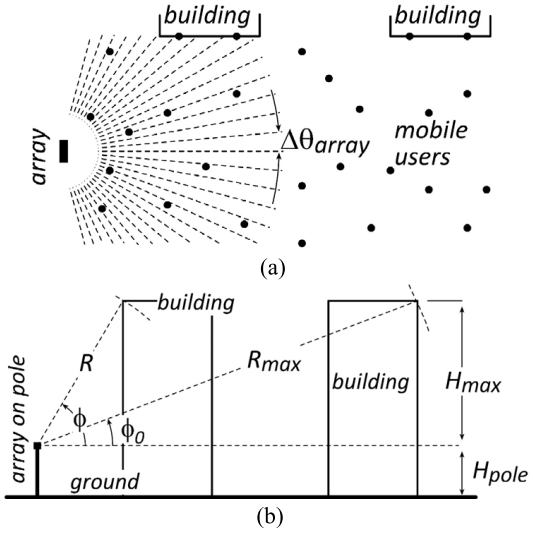


Fig. 2. Linear array field of view (a) with users is primarily distributed laterally over the ground (b) but some distributed vertically in tall buildings.

transmitter channels, each having a linear microstrip patch antenna array, a CMOS frequency upconversion IC, and an InP HBT power amplifier (PA) IC, plus two PCBs providing baseband signals and dc connections.

A. Array Directivity and Field of View

The linear array [Fig. 2(a)] steers the beam horizontally but not vertically and, given 32 elements, provides a narrow lateral and a moderate vertical beamwidth. To justify this design decision, we show in the following that, despite providing only horizontal beam steering, a linear array can communicate to receivers either on the ground or at the tops of moderately tall buildings [Fig. 2(b)]. Given maximum range $R_{\max}$ [Fig. 2(b)], maximum building height above the array $H_{\max}$, and array directivity D_t, because $P_{\text{received}} \propto D_t/R^2$ and $R/R_{\max} = \sin\phi_o/\sin\phi$, we find that

$$P_{\text{received}} \propto \frac{D_t \sin^2\phi}{R_{\max}^2 \sin^2\phi_o}. \tag{1}$$

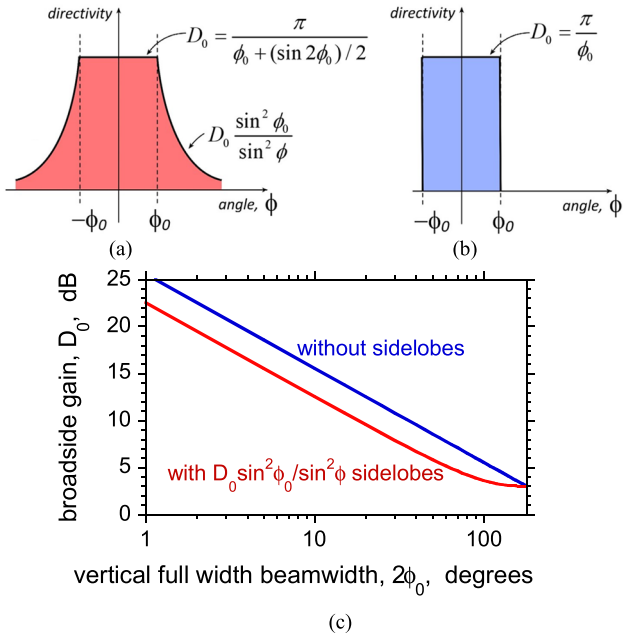


Fig. 3. Antenna vertical directivity patterns (a) for a system providing constant received signal intensity, independent of range up to some maximum $R_{\max}$, for buildings of maximum height $H_{\max}$, and (b) compared to a vertical directivity pattern that provides coverage only over a narrow range of vertical directions. (c) Gains of the two cases, in the horizontal direction.

Consequently, if the antenna's vertical directivity [Fig. 3(a)] D varies with elevation angle φ according to

$$D(\phi) = \begin{cases} D_0, & \text{for } |\phi| \le \phi_0 \\ D_0(\sin^2\phi_o/\sin^2\phi), & \text{for } \phi_0 < |\phi| < \pi/2 \\ 0, & \text{for } |\phi| > \pi/2 \end{cases} \tag{2}$$

then the received signal power at the maximum building height $H_{\max}$ will remain constant for all ranges $R \le R_{\max}$. Here, $D_0 = \pi/\left(\phi_0 + (\sin(2\phi_0))/2\right)$ because $\int_{-\pi}^{\pi} D(\phi)d\phi = 2\pi$, where

$$\begin{aligned}\int_0^{\pi} D(\phi)d\phi &= \int_0^{\phi_0} D_0 d\phi + \int_{\phi_0}^{\pi/2} D_0(\sin^2\phi_o/\sin^2\phi)d\phi \\ &= D_0\phi_0 + D_0 \sin\phi_o \cos\phi_o. \end{aligned} \tag{3}$$

If, instead, the $1/\sin^2\phi$ sidelobes are not present [Fig. 3(b)] and, hence, communication to building tops is not provided, then $D_0 = \pi/\phi_0$. Comparing these expressions, providing service to the building tops reduces the horizontally radiated power by at most 3 dB [Fig. 3(c)].

B. Array Link Budget

Consider the link budget [1], transmitting from base station to handset, for a 32-element array hub array simultaneously communicating to 16 handsets. The ratio of received to transmitted power ratio is $P_{\text{received}}/P_{\text{trans}} = (D_t D_r/16\pi^2)(\lambda/R)^2 \cdot \exp(-\alpha R)$, where D_t and D_r are the transmit and receive antenna directivities, respectively, R is the transmission range, and α is the atmospheric attenuation. The antenna directivities can be computed from the effective aperture areas A_E according to $D = 4\pi A_{\text{eff}}/\lambda^2$. We approximate the arrays as

TABLE I
LINK ANTENNA PARAMETERS AND PATH LOSS

parameter	symbol	value
transmitter array height	H_t	4.8λ
array width	W_t	15λ
vertical beamwidth	θ_t	3.75°
horizontal beamwidth	ϕ_t	12°
directivity	D_t	29.6 dB
receiver array height, width	H_r, W_r	4λ
beamwidth (vert., horiz.)	θ_r, ϕ_r	14.4°
directivity	D_r	23.0 dB
transmission range	R	50 m
free space path loss (α=0)	$D_t D_r \lambda^2/16\pi^2 R^2$	-56.5 dB
atmospheric loss @ 20 dB/km	$exp(-\alpha R)$	-1 dB
total path loss	$P_{receiver} / P_{\text{transmitter}}$	-57.5 dB

rectangles of uniform radiation of height H and width W having area $A = HW$; the vertical and horizontal full-width 3-dB beam widths, in radians, are $\theta = 2 \cdot \sin^{-1}(0.45\lambda/H)$ and $\phi = 2 \cdot \sin^{-1}(0.45\lambda/W)$, respectively.

We now assume that the hub transmitter has $N_t = 32$ channels at 0.5λ channel spacing, giving $W_t = 15\lambda$, that each transmitter channel antenna height is $H_t = 4.8\lambda$, and the receiving handset is an 8×8 array at 0.5λ spacing. Note that 0.5λ element spacing allows for beamsteering over 180° without the appearance of grating lobes, for either the transmitter or receiver; given realizable fabrication dimensions, the fabricated transmitter uses a slightly larger 0.65λ element spacing. Fair-weather, sea-level atmospheric loss [16] is ~1 dB/km at 135 GHz; 50 mm/h rain [17] increases this to 20 dB/km. If we then assume $R = 50$ m the transmission range, the net transmission $P_{\text{received}}/P_{\text{trans}}$ is then −57.5 dB. Table I summarizes the link antenna parameters and path loss; note that subsequent measurements show antenna gains 2–3 dB below these estimates.

For QPSK modulation with orthogonal transmitted symbols, a matched filter receiver, and receiver Gaussian noise with spectral density kTF, the receiver error probability is $P_{\text{error}} = Q(\alpha) = (2\pi)^{-1/2} \int_{\alpha}^{+\infty} \exp(-x^2/2)dx$, where $\alpha^2 = E_b/kTF$ and E_b is the received energy per bit; for 10^{-3} uncoded bit error rate, $\alpha^2 = 9.55$ (9.8 dB) [18]. $F = 7$ dB noise figure can be obtained in CMOS [19]. Assuming bit rate (not receiver bandwidth) $b = 10$ Gb/s, the received power at 10^{-3} uncoded bit error rate is then $P_{\text{received}} = \alpha^2 \cdot kTF \cdot b = -57.0$ dBm.

We allocate 1.5 dB, each, for transmitter and receiver antenna losses, and a further 1.5 dB, each, for transmitter and receiver packaging losses, giving a total of 6-dB antenna and packaging losses. The transmitter array's total radiated power would be $P_{\text{trans}} = -57$ dBm + 57.5 dB + 6 dB = 6.5 dBm if the transmitter were to radiate a single beam. However, to simultaneously transmit 16 such signal beams, the transmitter output power must be increased by 16:1, i.e., by 12 dB. This brings the total transmitter array output power, power combined over 32 RF channels, to 18.5 dBm. The output power per PA is 32:1 (15 dB) smaller than this, i.e., 3.5 dBm.

The time-average RF output power per PA in the 32-element transmitter array is 3.5 dBm. Under the MIMO operation [11] with the system's parameters assumed above, the PA 1-dB gain compression points must be 5 dB above the average operating power. Furthermore, we target 10-dB operating margins for end-of-life degradation, manufacturing variations, and partial beam blockage. With this PA back off and system operating margins, each PA in the transmitter array should have $P_{1\,\text{dB}} =$ 18.5 dBm. Table II summarizes the power-level calculation.

TABLE II
LINK POWER-LEVEL CALCULATIONS

parameter	symbol	value
receiver noise figure	F	7 dB
energy/bit for 10^{-3} error rate	α^2	9.8 dB
data rate	b	10 Gb/s
receiver sensitivity	$\alpha^2 \cdot kTF \cdot b$	-57.0 dBm
path loss	$P_{\text{receiver}}/P_{\text{transmitter}}$	57.5 dB
antenna and packaging losses	--	6.0 dB
number transmitted beams	N_{beam}	16 (12 dB)
total array output power	$P_{\text{transmitter}}$	18.5 dBm
number transmitter channels	$N_{\text{transmitter}}$	32 (15 dB)
output power per RF channel	$P_{\text{trans., 1 channel}}$	3.5 dBm
power amplifier back off	$P_{\text{trans., 1 channel}} / P_{out,1\text{dB}}$	5 dB
total operating margins	--	10 dB
power amplifier 1 dB point	$P_{1\text{dB}}$	18.5 dBm

The corresponding saturated output power might be 3–4 dB greater than this. CMOS technologies [20], [21] can, at 135 GHz, produce output power approaching these design targets; the power levels are readily produced, at high efficiency, using an InP HBT [22] PA driven by a CMOS transmitter (frequency upconversion) IC [3].

Other MIMO transceiver design requirements, including analog-to-digital converter (ADC) resolution, RF/IF and analog component 1-dB gain compression points, phase noise, and digital beamformer design, are addressed in [11]–[14] and [23].

III. SINGLE-CHANNEL TRANSMITTER MODULE

To evaluate the antenna, the IC-package interconnects, and the PA heatsinking, a single-channel transmitter [9] was designed and constructed. This transmitter has an upconversion IC, in GlobalFoundries 22-nm silicon on insulator (SOI) CMOS, with 2.8-dBm saturated output power and 16-GHz 3-dB modulation bandwidth [3]. The CMOS IC is bonded to an LTCC carrier using 50-μm-diameter copper pillars of 30 μm height. The CMOS IC output drives an InP HBT PA having 17-dBm $P_{1\,\text{dB}}$ with 9.7% associated PAE (20.5-dBm P_{sat}) [22]. The InP PA is attached to the carrier using silver-filled epoxy (84-1LMISNB), while its input, output, and power supplies are connected to the carrier using 18-μm-diameter Au wire bonds. The PA output is connected to an eight-element series-fed microstrip patch antenna on the same carrier [Fig. 4(a)].

A. Ceramic Carrier Design

Low carrier permittivity reduces skin-effect and dielectric mode losses in transmission lines and antennas. The carrier should provide narrow (<50 μm) conductors and spaces, both

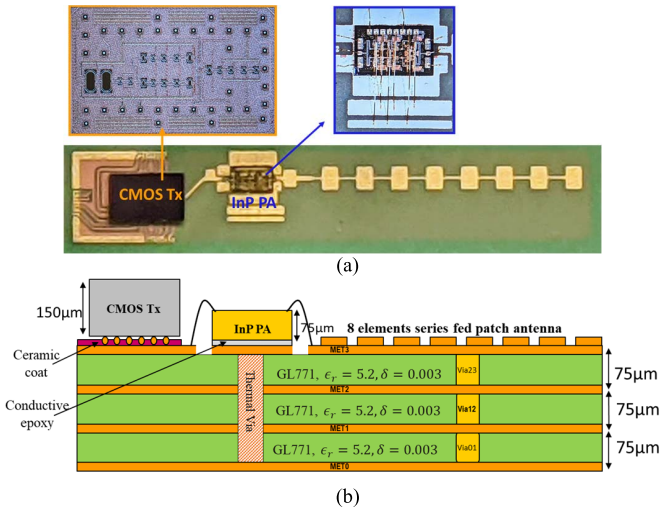


Fig. 4. *D*-band single-channel transmitter module: (a) micrographs and (b) schematic cross section.

for fine antenna features, so that the many low-frequency connections to the CMOS IC fit within the 0.65λ element pitch. The carrier is Kyocera GL771 LTCC, with three dielectric layers, each with $\varepsilon_r = 5.2$ and $\delta = 0.003$, and four metal layers. The minimum trace widths and spacings are 50 μm, and the minimum via diameter is 50 μm. The top metal layer (MET3) forms the antenna and microstrip signal lines routing the mm-wave, I/Q baseband, and local oscillator (LO) reference signals. MET2 and MET0 serve as ground planes, while MET1 routes supply and bias voltages. Because the amplifier output power decreases as it heats, many copper-filled vias were placed in the LTCC below the InP IC to conduct heat from it to the metal carrier below [Fig. 4(b)].

B. IC Mounting to the LTCC Carrier

A ceramic coat, with 75-μm openings at the copper pillar locations, prevents the solder dome on the copper pillar from excessively wicking away during solder bonding. Nevertheless, given the minimum 75-μm ceramic coat openings, for reliable bonding, additional solder on pad (SOP) was added to the ceramic carrier. The IC-package interconnect has a <1-dB measured transition loss, including the copper pillar and a 200-μm-length on-carrier trace [24].

Gold wire bonds provide dc and 135-GHz connections to the InP PAs. The bond parasitics reduce the PA gain and the power it delivers to the antenna. To minimize loss, we considered either mounting the PA within a cavity [Fig. 5(a)] or on the LTCC top surface [Fig. 5(b)]. While cavity mounting avoids the 76-μm bond wire height difference associated with the thickness of the InP die, the $\pm$150-μm lateral tolerance in the cavity dimensions increases the necessary lateral distance spanned by the wire bond. Surface mounting allows a shorter bond and hence was selected. The minimum wire bond length is set by the PA die thickness and by the amount of lateral extrusion of the die-attach epoxy from under the IC.

C. CMOS to InP PA Transition

The InP PA input and output ports are connected using 450-μm-length Au wire bonds of 18 μm diameter [Fig. 6(a)].

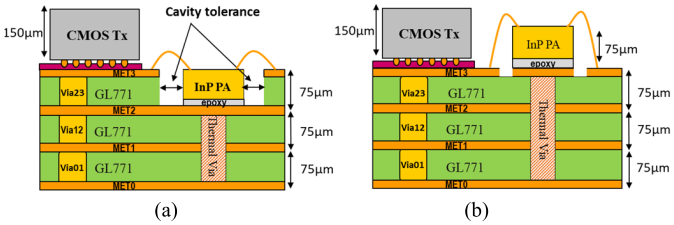


Fig. 5. PA mounting in the LTCC carrier with (a) cavity and (b) without cavity.

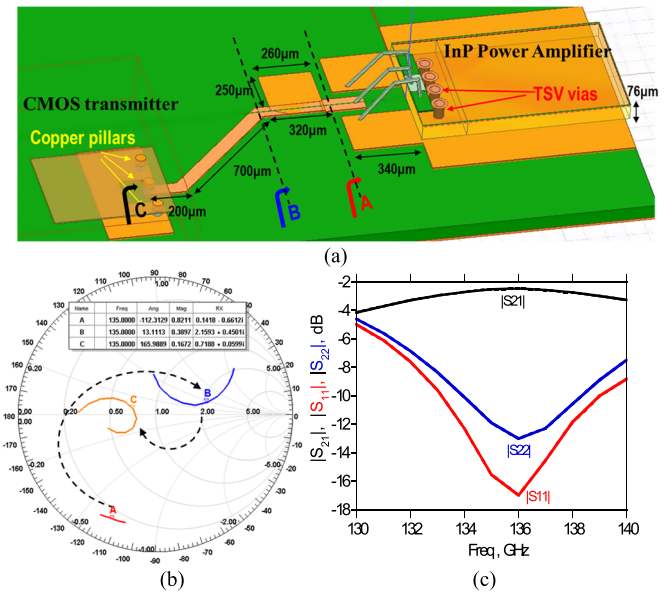


Fig. 6. CMOS transmitter to InP transition design (a) impedance matching network on HFSS. (b) Matching network Smith chart. (c) simulated *S*-parameters.

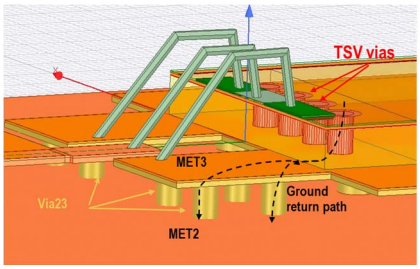


Fig. 7. InP-LTCC transition and PA ground return current path.

Fig. 6(b) shows the amplifier input impedance, including the wire bond, at various points on the carrier. A network [Fig. 6(a)] on the LTCC carrier compensates for the wire bonds, matching the PA input to the CMOS 50 Ω output impedance. The network has 8-GHz simulated 1-dB bandwidth and 2.6-dB simulated insertion loss at 135 GHz [Fig. 6(c)], including the loss from the wire bond, the ~1-mm total interconnect length, and the CMOS copper pillars.

Though wire bonds between the InP PA and the LTCC carrier are provided for both signal and ground, the ground return currents are primarily carried by the through-substrate vias on the InP IC (Fig. 7).

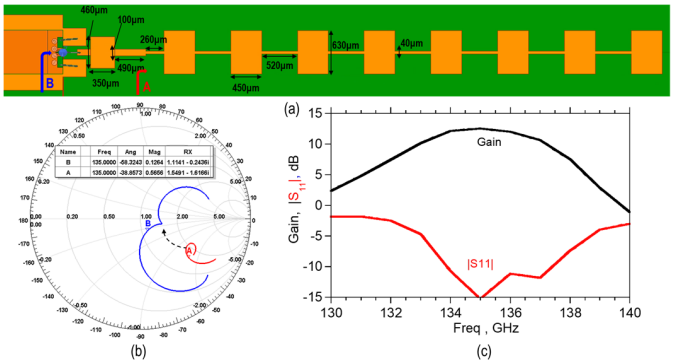


Fig. 8. Series-fed patch antenna (a) design on HFSS, (b) antenna input impedance on Smith chart, and (c) simulated antenna gain and return loss, inclusive of the InP-LTCC wire bonds and the matching network.

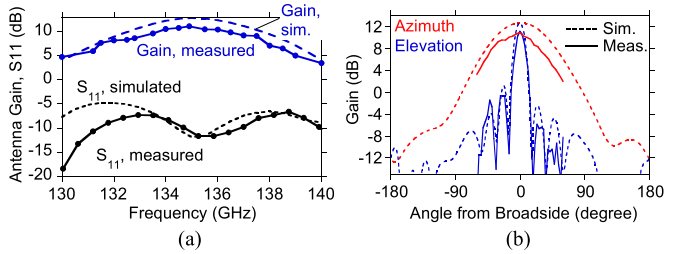


Fig. 9. Series-fed patch antenna: measured and simulated (a) gain and return loss versus frequency and (b) measured and simulated radiation pattern.

D. Antenna Design

The eight-element series-fed patch antenna was designed using Ansys HFSS. The antenna elements are on the top metal layer (M1), while M2 provides the ground plane. The antenna input impedance is transformed to 50 Ω at the PA bond pad using the wire bonds and a stepped-impedance transmission line (Fig. 8). The simulated antenna gain, from the PA output node, is 12 dB with 6-GHz 3-dB bandwidth [Fig. 8(c)] and −15-dB simulated return loss (S_{11}). The antenna bandwidth could be increased by adding slots to each patch [25] and by replacing the series feed network with a corporate feed network.

The radiation pattern for antenna test structure [24] (without input wire bond) was measured using a *D*-band signal source delivered through a wafer probe, with the radiation captured by a horn antenna on a rotation stage, this connected to a spectrum analyzer with external harmonic mixer. The antenna has 11-dB measured gain and 6-GHz 3-dB bandwidth [Fig. 9(a)]. The measured antenna gain is 1 dB below simulation, while the measured return loss (S_{11}) is −12 dB. The antenna has 12° E-plane and 70° H-plane 3-dB beam widths [Fig. 9(b)], while the sidelobes are suppressed by 12 dB.

E. Single-Channel Transmitter Gain, EIRP, and Patterns

The module conversion gain and the modulation bandwidth were measured with a 135-GHz LO, with a 15-GHz external signal source with 0-dBm power driving the on-wafer 9× frequency multiplier, while the baseband (I or Q) signal swept from 100 MHz to 10 GHz. The modulation sidebands

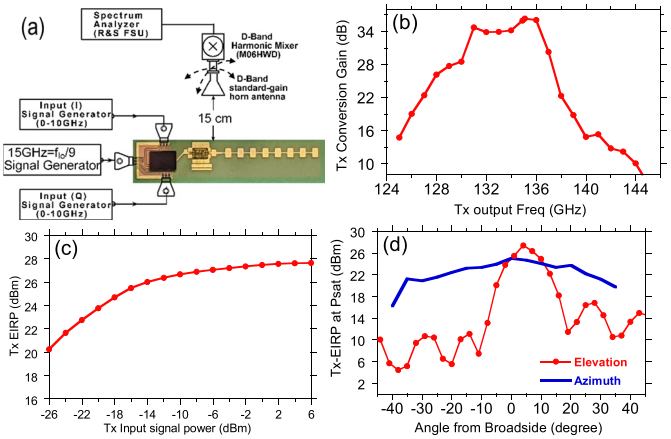


Fig. 10. Single-channel transmitter module (a) measurement setup, (b) module frequency response, (c) P_{out} versus P_{in}, and (d) module radiation pattern in the E- and H-planes.

were captured using a horn antenna and *D*-band harmonic mixer and spectrum analyzer calibrated against a power meter [Fig. 10(a)]. The module has a 6-GHz 3-dB modulation bandwidth [Fig. 10(b)]. The overall module bandwidth is limited by that of the antenna (6 GHz at −3 dB), the CMOS IC (16 GHz at −3 dB), the InP PA (43 GHz at −3 dB), the CMOS-InP transition (>10 GHz at −3 dB), and the InP-antenna transition (8 GHz at −1 dB).

The measured single sideband (SSB) conversion gain is 36 dB. The saturated EIRP, measured with a 135-GHz LO and a 100-MHz baseband signal swept from −26 to 6 dBm, is 27.5 dBm [Fig. 10(c)].

The measured PA P_{sat} is 20 dBm [22], while the antenna gain is 11 dB (Fig. 9). The measured EIRP is less than the anticipated 31 dBm in part because of the wire-bond losses, and the CMOS IC output power is insufficient to drive the PA into saturation. Despite this, 27.5 dBm is the highest reported EIRP from a single-channel *D*-band transmitter. Fig. 10(d) shows the measured far-field radiation patterns. The module consumes 760 mW, with 200 mW from the CMOS and 560 mW from the InP IC.

F. Single-Channel Transmitter Modulation Performance

Modulation performance of the single-channel transmitter was then characterized using an arbitrary waveform generator (AWG) for the transmitter input signals and monitoring the module output at a 15-cm propagation distance using a horn antenna, a *D*-band fundamental mixer for frequency downconversion, and a digital storage oscilloscope (DSO) for signal acquisition. The AWG generated QPSK, 16 quadratic-amplitude modulation (QAM), and 64 QAM constellations modulating a 4-GHz IF. The transmitter module then upconverts this modulated signal to a 134-GHz carrier. The *D*-band fundamental mixer downconverts the received signal to a 4-GHz IF. The DSO demodulates the received signal and, after adaptive equalization, displays (Table III) the modulation constellation and computes the error vector magnitude (EVM). Stated EVM magnitudes are referenced to the constellation's rms amplitude. Under 5-Gbaud, 64 QAM

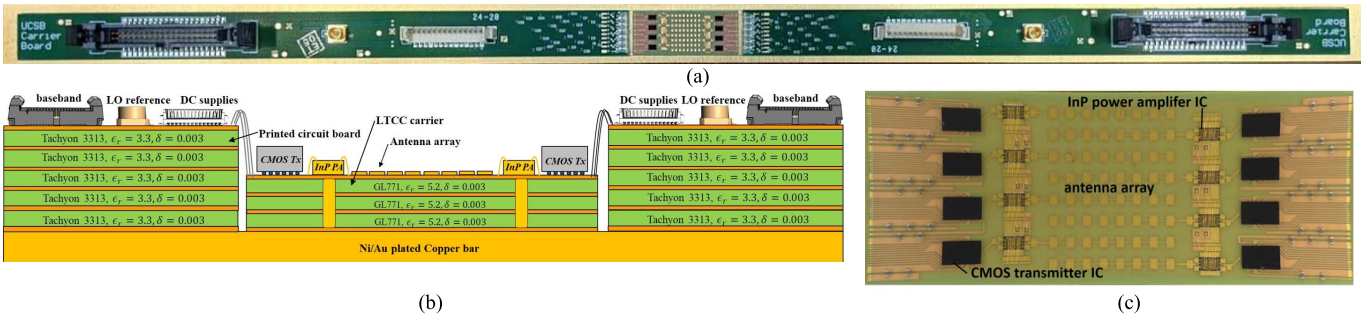
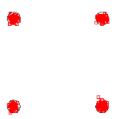
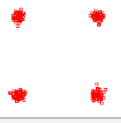
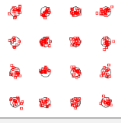


Fig. 11. Eight-channel 135-GHz MIMO hub transmitter array tile module: (a) photograph of the overall module; (b) cross-sectional diagram showing the interface PCBs, the LTCC carrier, connectors, and ICs; and (c) photograph of the LTCC carrier showing the antennas and CMOS and InP ICs. The overall module is 450 mm × 15 mm, while the LTCC carrier is approximately 12 mm × 33 mm. To fit on the page, the figure shows the array with its long axis oriented horizontally; in installation, the long axis, and the individual antennas, would be oriented vertically.

TABLE III
TRANSMITTER MODULE MEASURED MODULATION CONSTELLATIONS AND COMPUTED EVMS

EIRP=24 dBm/ 3 dB Back off from P_{sat}		
QPSK (1GBaud)	16QAM(1GBaud)	64QAM(1GBaud)
		
5.4% (RMS)	6.8% (RMS)	6.5% (RMS)
EIRP=21 dBm/ 6 dB Back off from P_{sat}		
QPSK (5GBaud)	16QAM(5GBaud)	64QAM(5GBaud)
		
7.69% (RMS)	8.4% (RMS)	8.5% (RMS)

modulation (30 Gb/s), the module shows 8.5% rms EVM at 21.5-dBm EIRP. Synthesizer phase noise may contribute to the observed EVM.

IV. EIGHT-CHANNEL MIMO TRANSMITTER TILE MODULE

The eight-channel MIMO transmitter tile module (Fig. 11) contains a Kyocera GL771 LTCC carrier with eight transmitter channels, each having a linear microstrip patch antenna array, a CMOS transmitter IC [3], and an InP HBT PA IC [22], plus two PCBs providing baseband signal and dc connections. Fig. 11(a) shows the photographs of the full module and the assembled LTCC carrier, Fig. 11(b) shows a module cross section, and Fig. 11(c) shows an image of the LTCC carrier with mounted InP and CMOS ICs.

The 15-GHz LO reference and IQ baseband signals are routed on M1 and dc supplies and bias lines on M3. The fine 50-μm LTCC lithographic resolution allows a 1.3λ pitch between ICs on each side of the array, hence a small 0.65λ antenna pitch, which allows for a wide horizontal angular field of view. The simulated antenna array, including the wire bond transitions at the InP PA output, shows 22-dB directivity and 20.5-dB realized gain (Fig. 12).

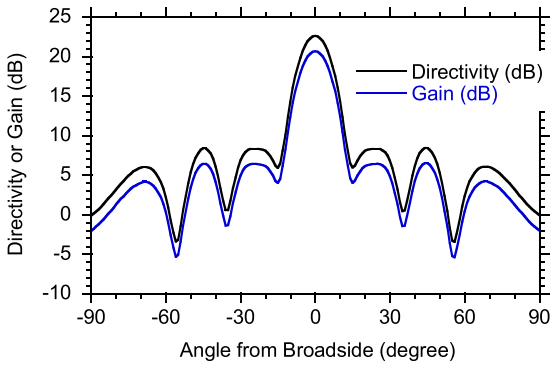


Fig. 12. Simulated directivity and gain for the eight-channel MIMO tile antenna array, with angle varied in the horizontal plane.

A. Transmitter Module/Tile Integration

PCBs on the array's two sides provide dc, baseband IQ signals, and 15-GHz LO reference connections. To tile modules into larger arrays (Fig. 1) without unequal spacings between antennas, the PCB must have the same width (11.6 mm) as the LTCC carrier. On this prototype, the PCB width is 15 mm and, hence, would have larger antenna spacings at the module boundaries than within a module. This will introduce radiation pattern grating lobes. Even at 15 mm, it is difficult to route all the signals within the PCB width. The PCB has five layers of Tachyon 3133 dielectric ($\varepsilon_r = 3.29$ and $\delta = 0.003$) and 75-μm lithographic resolution. IQ baseband and the 15-GHz LO reference signals are routed in stripline or as grounded coplanar waveguide (CPW) in the top metal lane. The LO reference has a dc-to-65-GHz Rosenberger 18S102-40ml5 coaxial connector and drives four CMOS ICs through a 4:1 splitter (Fig. 13) on the PCB having only 0.8-dB simulated excess insertion loss; given the 6-dB loss associated with 4:1 power distribution, the 0.8-dB excess loss, and a ~0-dBm CMOS LO drive power requirement, the simulated LO drive power requirement is 3 dBm. The four differential I/Q signals on each array side are connected by a compact Samtec EHF PCB connector. This limits the IQ bandwidth to ~1 GHz. A new PCB in design uses the Rosenberger 18S102-40ml5 for both LO and IQ baseband connections; the PCB must then be either longer or wider. Each board has a multipin dc connector.

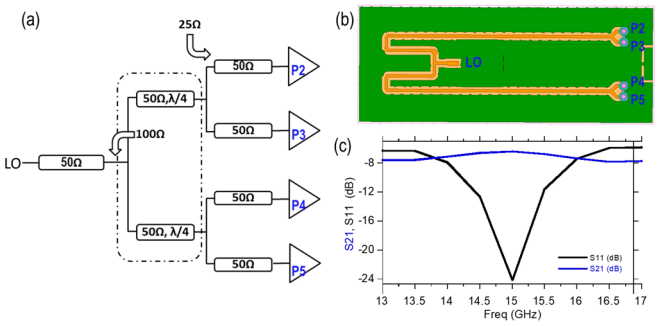


Fig. 13. Design of the LO reference signal splitter on the PCB: (a) splitter schematic, (b) geometry, and (c) simulated insertion loss and input reflection coefficient.

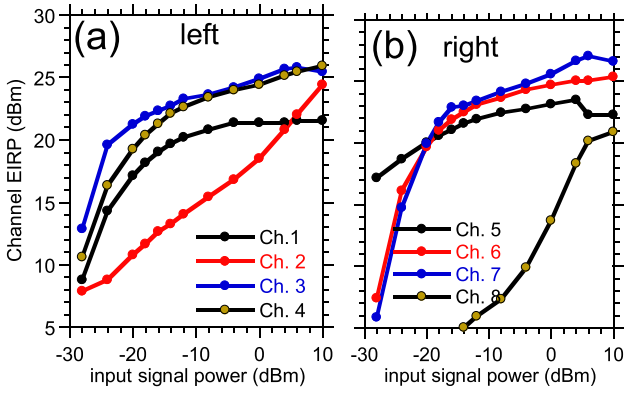


Fig. 14. Measured 135-GHz EIRP versus baseband input power for the four transmitter channels on (a) left and (b) right sides of the module. Because of assembly difficulties, two of the eight channels have low gain and output power.

The LTCC interposer and two PCBs are bonded to a Ni/Au-plated copper bar (Fig. 11), using a conductive adhesive. The bar mechanically supports the LTCC and PCB, connects their ground planes, and removes heat. Aluminum wire bonds connect the PCBs to the LTCC carrier. Supplies are bypassed by MIM capacitors on the LTCC carrier and surface-mount capacitors on the PCB.

B. Transmitter Tile Characterization

Fig. 14 shows the EIRP versus input power for each transmit module channel. Because of assembly difficulties, two of the eight channels have very low gain, and two other channels have EIRP well below 27.5 dBm measured independently on a single-channel test structure [Fig. 10(c)].

C. Transmitter Array Calibration and Beamforming

The MIMO transmitter tile is designed for use with digital beamforming [13]. For prototype testing, a PC running MATLAB generates each channel's baseband transmitted signal and sends this to a field-programmable gate array (FPGA) evaluation kit (ZCU-111). From these signals, the FPGA generates modulated signals at a 1-GHz IF. External IQ demodulators (ADI LTC5594) then convert the 1-GHz IF FPGA outputs to IQ baseband (Fig. 15). The required sixteen baseband

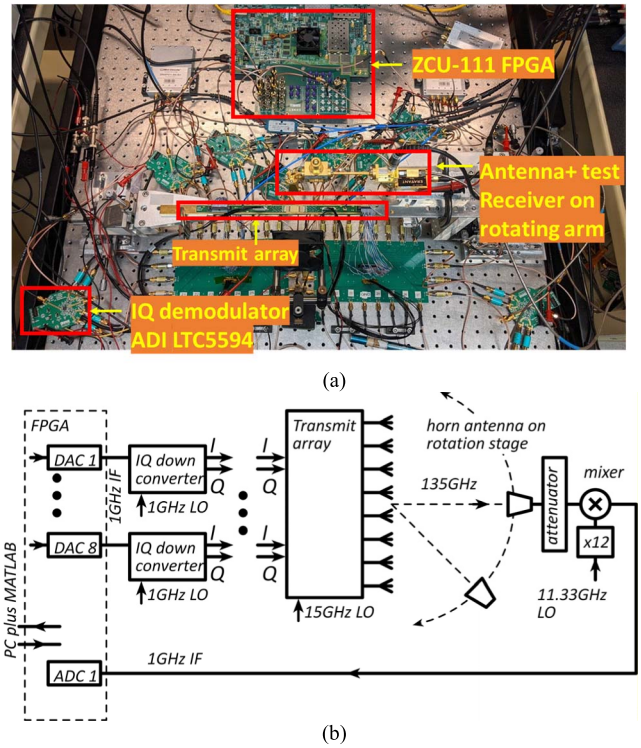


Fig. 15. Experimental configuration for transmitter array characterization. (a) Actual setup. (b) Simplified drawing for the setup. The eight FPGA DACs each generate modulated data on a 1-GHz IF and eight IQ downconverters generate IQ signals that drive the transmitter array.

differential IQ signals are thus generated by an FPGA having only eight digital-to-analog converters (DACs). A commercial-off-the-shelf test receiver, mounted on a rotation stage 15 cm from the array, downconverts the signal to a 1-GHz IF, and an ADC on the FPGA captures this signal.

To form and aim beams, the array must be calibrated, i.e., differences between channel gains and phases are measured and then corrected for. Given the strong differences between channel gains (Fig. 14), only phase errors were calibrated. Device drivers and calibration procedures were adapted from Pi-Radio open-source code [26]. These first measure, with the test receiver in place, the per-channel fractional timing offsets of the modulating data streams and the channel-channel variations in the LO phase. In beamforming and data transmission experiments, the resulting calibration factors are applied to the transmitter waveforms prior to being sent to the DACs.

Having calibrated the array, the drive signals to the eight channels were then set to direct a continuous-wave (CW) signal to broadside [Fig. 16(a)], and the horn antenna then rotated to measure the radiated power density as a function of angle in the H-plane. The 38.5-dBm peak EIRP is a record for an array in *D*-band. From the single-channel EIRP and the number of channels, the EIRP should be 45 dBm at P_{sat}; the disparity is due to assembly yield. Fig. 16(b) shows the array of radiation patterns as the beam is steered; at larger scan angles, the beam pattern degrades. The measured beamwidth is larger than that simulated (Fig. 12); both these disparities arise because only four of the eight transmit channels function properly.

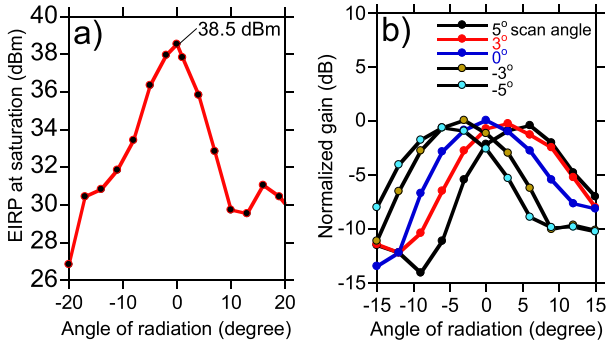


Fig. 16. Measured transmitter array EIRP (a) measured at saturation, as a function of angle of radiation, with the array aimed at broadside, and angle of radiation in the H-plane. (b) Measured beam patterns with the array aimed at 5°, 3°, 0°, −3°, and −5° scan angles.

TABLE IV
TRANSMITTER TILE MODULE MEASURED MODULATION CONSTELLATIONS AND COMPUTED EVMS

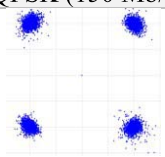
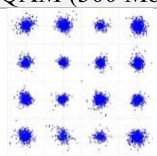
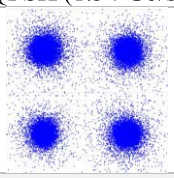
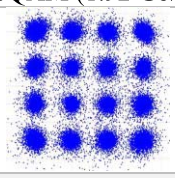
EIRP=35 dBm/ 3 dB Back off from P_{sat}	
QPSK (150 Mb/s)	16QAM (300 Mb/s)
	
-23 dB EVM (RMS)	-20.5 dB EVM (RMS)
QPSK (1.34 Gb/s)	16QAM (1.92 Gb/s)
	
-13.5dB EVM (RMS)	-13dB EVM (RMS)

Table IV shows the results of modulation experiments. The data are transmitted using orthogonal Frequency division multiplexing (OFDM), with 960-kHz subcarrier spacing. The constellation diagrams show the demodulated signal after performing frequency-domain OFDM equalization. The pilot density is approximately 20%. In single-beam operation, there is −13.5-dB rms EVM in 1.34-Gb/s QPSK transmission and −13-dB EVM in 1.92-Gb/s 16 QAM transmission. The average output EIRP during these measurements was 35 dBm.

Fig. 17 shows the EVM as a function of data rate. Data rates are limited both by the FPGA sample rate and by the bandwidth of baseband IQ signal connectors; without these limits, the single-channel module operated to 5 GBaud at 64 QAM (as shown in Table III).

The FPGA was then programmed to generate two simultaneous steerable beams, aimed at angles of −8° and +3°, each carrying a QPSK-modulated signal with 34-dBm peak measured EIRP per beam. In this measurement, an FPGA (ZCU-111) generates drive signals to the eight transmitter array channels, with signals corresponding to two simultaneously transmitted beams, carrying two different data streams,

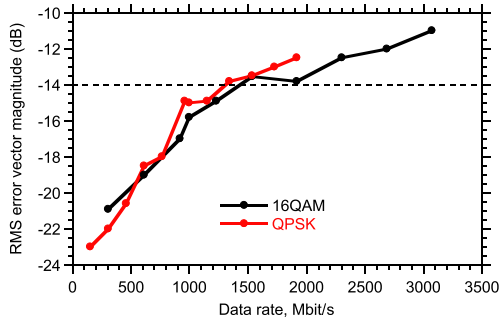


Fig. 17. Computed EVM, in dB relative to the constellation's rms amplitude, as a function of data rate.

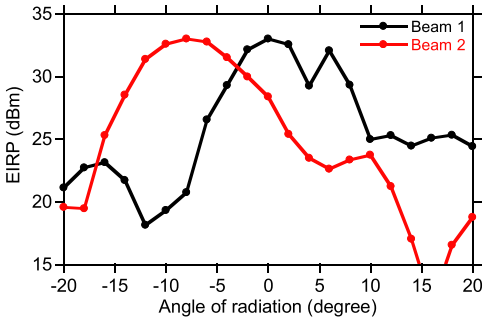


Fig. 18. Measurement of the array simultaneously transmitting two signal beams, the graph shows the power (EIRP) in each of the two signal beams as a function of the angle of radiation.

radiated in two different directions. The signal from the test receiver, as shown in Fig. 15, is downconverted to an IF and connected to one of the input (ADC) channels of the FPGA. The FPGA demodulates this received IF signal and then correlates it against the two different known transmitted data streams. In this manner, as the position of the test receiver is changed, the strength of each of the two radiated signals can be measured as a function of radiation direction. Fig. 18 shows the resulting measured radiation pattern in two-beam operation.

V. CONCLUSION AND COMPARISON

We have demonstrated 135-GHz eight-element MIMO transmitter array tile modules. The module is designed for use in sets to form 32-element or larger MIMO horizontal linear arrays and is designed for use with digital beamforming. A single-channel transmitter module, using a CMOS upconversion IC, an InP HBT PA, and a microstrip patch antenna array on a Kyocera LTCC substrate ceramic interposer, has a record EIRP of 27.5 dBm and can support up to 30-Gb/s transmission using 64 QAM. The data rate is limited by bandwidth of the antenna and the matching network that compensates for wirebond parasitics.

With an eight-channel MIMO transmitter hub array tile module, record 38.5-dBm EIRP, data transmission, beam steering, and two-beam operation have been demonstrated. The present results, both beam steering angle and EIRP, are limited by assembly difficulties; had each of the eight

TABLE V
COMPARISON WITH STATE-OF-THE-ART *D*-BAND TRANSMITTERS

	[2] Abu-Surra ICC2021	[6] Singh RFIC2020	[7] S. Li IMS2021	[27] Hamani RFIC2021	[28] Townly CICC2020	[29] Sawaby RFIC2020	This Work	
Freq (GHz)	140	115-155 135-170	140	148	113	135	135	
IC Tech.	45nm SOI	0.13µm SiGe	45nm SOI	45nm SOI	28nm CMOS	0.13µm SiGe	22FD-SOI + InP HBT	
Package Tech	PCB	Radio on Glass	Quartz Superstrate	PCB	PCB	PCB + Lens	LTCC Interposer	
Type	Multi-beam MIMO[$]	Single Channel	Single beam	Single beam	Single Channel	2x2 LOS MIMO	Single channel	MIMO
Tx/Rx	TX, RX	TX, RX	TX	TX	TX, RX	TX, RX	TX	TX tile
Number of channels	4,8, and 16	1	8	2	2	2	1	8
Antenna Integration	Yes	No	Yes	Yes	Yes	Yes	Yes	
Tx-Psat	2 dBm	13 dBm	--	--	--	2.5 dBm	20.5 dBm	
EIRP@Psat	17-27 dBm	--	32 dBm	3.8 dBm	0 dBm	28 dBm	27.5 dBm	38.5 dBm
Peak data rate	6Gb/s	42Gb/s 8Gb/s	16Gb/s 18Gb/s	85Gb/s	80Gb/s	2x16Gb/s	30Gb/s	3Gb/s Tx
Modulation Format	16QAM	64QAM 256QAM	QPSK 64QAM	64QAM	16QAM	QPSK	64QAM	16QAM
EVM	NA	-23dB -30dB	6.25% 5.5%	--	--	--	8.5%	-13.5dB
Link	Air	WR-6	Air	Air	Air	Air	Air	
Distance	15m	--	--	5cm	10cm	6cm	15cm	
Pdc	--	1350mW	1900mW	600mW	470mW	432mW	760mW	6100mW

transmitter channels functioned with the same performance as the single channel, the EIRP would have been 46 dBm. For the transmitter tiles, the maximum data rate is limited by the FPGA ADC/DAC sampling rate and the limited bandwidth of the compact IQ baseband signal connector.

Table V compares state-of-the-art packaged *D*-band (110–170 GHz) transmitters for single-beam and multibeam arrays. The eight-channel transmitter module has the highest reported EIRP among single-beam and multibeam *D*-band arrays.

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REFERENCES

[1] M. J. W. Rodwell, "100–340 GHz spatially multiplexed communications: IC, transceiver, and link design," in *Proc. IEEE 20th Int. Workshop Signal Process. Adv. Wireless Commun. (SPAWC)*, Jul. 2019, pp. 1–5, doi: 10.1109/SPAWC.2019.8815433.

[2] S. Abu-Surra *et al.*, "End-to-end 140 GHz wireless link demonstration with fully-digital beamformed system," in *Proc. IEEE Int. Conf. Commun. Workshops (ICC Workshops)*, Jun. 2021, pp. 1–6, doi: 10.1109/ICCWorkshops50388.2021.9473600.

[3] A. A. Farid, A. Simsek, A. S. H. Ahmed, and M. J. W. Rodwell, "A broadband direct conversion transmitter/receiver at D-band using CMOS 22 nm FDSOI," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 135–138, doi: 10.1109/RFIC.2019.8701730.

[4] S. Carpenter *et al.*, "A *D*-band 48-Gbit/s 64-QAM/QPSK direct-conversion I/Q transceiver chipset," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1285–1296, Apr. 2016, doi: 10.1109/TMTT.2016.2533491.

[5] M. Ito, T. Okawa, and T. Marumoto, "*D*-band transceiver utilizing 70-nm GaAs-mHEMT technology for FDD system," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nashville, TN, USA, Nov. 2019, pp. 1–4.

[6] A. Singh *et al.*, "A *D*-band radio-on-glass module for spectrally-efficient and low-cost wireless backhaul," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Los Angeles, CA, USA, Aug. 2020, pp. 99–102.

[7] S. Li, Z. Zhang, and G. M. Rebeiz, "An eight-element 136–147 GHz wafer-scale phased-array transmitter with 32 dBm peak EIRP and >16 Gbps 16QAM and 64QAM operation," *IEEE J. Solid-State Circuits*, doi: 10.1109/JSSC.2022.3148385.

[8] A. Simsek, A. S. H. Ahmed, A. A. Farid, U. Soylu, and M. J. W. Rodwell, "A 140 GHz two-channel CMOS transmitter using low-cost packaging technologies," in *Proc. IEEE Wireless Commun. Netw. Conf. Workshops (WCNCW)*, Apr. 2020, pp. 1–3, doi: 10.1109/WCNCW48565.2020.9124890.

[9] A. A. Farid, A. S. H. Ahmed, and M. J. W. Rodwell, "A 27.5 dBm EIRP D-Band transmitter module on a ceramic interposer," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2021, pp. 43–46, doi: 10.1109/RFIC51843.2021.9490491.

[10] A. A. Farid, A. S. H. Ahmed, A. Dhananjay, P. Skrimponis, S. Rangan, and M. Rodwell, "135 GHz CMOS/LTCC MIMO receiver array tile modules," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Dec. 2021, pp. 1–4, doi: 10.1109/BCICTS50416.2021.9682493.

[11] A. A. Farid, M. Abdelghany, U. Madhow, and M. J. W. Rodwell, "Dynamic range requirements of digital vs. RF and tiled beamforming in mm-wave massive MIMO," in *Proc. IEEE Radio Wireless Symp. (RWS)*, Jan. 2021, pp. 46–48, doi: 10.1109/RWS50353.2021.9360362.

[12] M. Abdelghany, U. Madhow, and A. Tölli, "Beamspace local LMMSE: An efficient digital backend for mmWave massive MIMO," in *Proc. IEEE 20th Int. Workshop Signal Process. Adv. Wireless Commun. (SPAWC)*, Jul. 2019, pp. 1–5, doi: 10.1109/SPAWC.2019.8815585.
[13] S. H. Mirfarshbafan, A. Gallyas-Sanhueza, R. Ghods, and C. Studer, "Beamspace channel estimation for massive MIMO mmWave systems: Algorithm and VLSI design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 5482–5495, Dec. 2020, doi: 10.1109/TCSI.2020.3023023.
[14] M. E. Rasekh, M. Abdelghany, U. Madhow, and M. Rodwell, "Phase noise in modular millimeter wave massive MIMO," *IEEE Trans. Wireless Commun.*, vol. 20, no. 10, pp. 6522–6535, Oct. 2021, doi: 10.1109/TWC.2021.3074911.
[15] A. Pallotta *et al.*, "SiGe:BiCMOS technology is enabling D-band link with active phased antenna array," in *Proc. Joint Eur. Conf. Netw. Commun. 6G Summit (EuCNC/6G Summit)*, 2021, pp. 496–501, doi: 10.1109/EuCNC/6GSummit51104.2021.9482432.
[16] J. C. Wiltse, "Corrections to published curves for atmospheric attenuation in the 10 to 1000 GHz region," in *IEEE Antennas Propag. Soc. Int. Symp. Dig.*, vol. 4, Jul. 1997, pp. 2580–2583, doi: 10.1109/APS.1997.625531.
[17] R. Olsen, D. Rogers, and D. Hodge, "The aR^b relation in the calculation of rain attenuation," *IEEE Trans. Antennas Propag.*, vol. 26, no. 2, pp. 318–329, Mar. 1978.
[18] U. Madhow, *Fundamentals of Digital Communcation*. Cambridge, U.K.: Cambridge Univ. Press, 2008.
[19] S. Li and G. M. Rebeiz, "A 134–149 GHz IF beamforming phased-array receiver channel with 6.4–7.5 dB NF using CMOS 45 nm RFSOI," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 103–106, doi: 10.1109/RFIC49505.2020.9218355.
[20] S. Li and G. M. Rebeiz, "A 130–151 GHz 8-Way power amplifier with 16.8–17.5 dBm psat and 11.7–13.4% PAE using CMOS 45 nm RFSOI," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2021, pp. 115–118, doi: 10.1109/RFIC51843.2021.9490507.
[21] B. Philippe and P. Reynaert, "24.7 A 15 dBm 12.8%-PAE compact D-band power amplifier with two-way power combining in 16nm FinFET CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 374–376.
[22] A. S. H. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter, and M. J. W. Rodwell, "A 140 GHz power amplifier with 20.5 dBm output power and 20.8% PAE in 250-nm InP HBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Los Angeles, CA, USA, Aug. 2020, pp. 492–495.
[23] M. Abdelghany, A. A. Farid, M. E. Rasekh, U. Madhow, and M. J. W. Rodwell, "A design framework for all-digital mmwave massive MIMO with per-antenna nonlinearities," *IEEE Trans. Wireless Commun.*, vol. 20, no. 9, pp. 5689–5701, Sep. 2021, doi: 10.1109/TWC.2021.3069378.
[24] A. A. Farid, A. S. H. Ahmed, A. Simsek, and M. J. W. Rodwell, "A packaged 135 GHz 22 nm FD-SOI transmitter on an LTCC carrier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 713–716, doi: 10.1109/IMS19712.2021.9575026.
[25] R. Vincenti Gatti, R. Rossi, and M. Dionigi, "Single-layer line-fed broadband microstrip patch antenna on thin substrates," *Electronics*, vol. 10, no. 1, p. 37, Dec. 2020, doi: 10.3390/electronics10010037.
[26] A. Dhananjay *et al.*, "Calibrating a 4-channel fully-digital 60 GHz SDR," in *Proc. 14th Int. Workshop Wireless Netw. Testbeds, Exp. Eval. Characterization*, Sep. 2020, pp. 40–47, doi: 10.1145/3411276.3412195.
[27] A. Hamani *et al.*, "An 84.48 Gb/s CMOS D-band multi-channel TX system-in-package," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2021, pp. 207–210.
[28] A. Townley *et al.*, "A fully integrated, dual channel, flip chip packaged 113 GHz transceiver in 28 nm CMOS supporting an 80 Gb/s wireless link," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Mar. 2020, pp. 1–4, doi: 10.1109/CICC48029.2020.9075890.
[29] M. Sawaby *et al.*, "A fully integrated 32 Gbps 2×2 LoS MIMO wireless link with UWB analog processing for point-to-point backhaul applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 107–110, doi: 10.1109/RFIC49505.2020.9218371.

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