200 GHz Low Noise Amplifiers in 250 nm InP HBT Technology

Utku Soylu[*1], Ahmed S. H. Ahmed[*], Munkyo Seo[#], Ali Farid[*], Mark Rodwell[*]
[*]Department of Electrical and Computer Engineering, University of California, Santa Barbara, USA
[#]Department of Electrical and Computer Engineering, Sungkyunkwan University, South Korea
[1]utkusoylu@ucsb.edu

***Abstract* — We report 200 GHz InP DHBT low noise amplifiers in common base (CB) and common emitter (CE) topologies, together with a design procedure based on minimum noise measure. The CB design shows 7.4±0.7 dB noise figure over 196-216 GHz, 14.5 dB gain and -21.1 dBm Pin1dB at 200 GHz, and dissipates 9.2 mW, while the CE design shows 7.2±0.4 dB noise figure over 196-216 GHz, 13 dB gain and -18.2 dBm Pin1dB at 200 GHz, and dissipates 19.22 mW. To the authors' knowledge, these results demonstrate record noise figure for bipolar transistor amplifiers operating near 200 GHz.**

***Keywords* —G-band, millimeter wave, noise figure (NF), noise measure (M), low noise amplifier (LNA), indium phosphide (InP), double heterojunction bipolar transistor (DHBT).**

I. Introduction

There is increasing interest in the 200-300 GHz frequency band as the wide spectrum can support very high data rate wireless communications [1]. At these frequencies, greater integration scales have been demonstrated for receivers in SiGe and InP HBT than in III-V HEMT technologies, but HEMTs exhibit lower noise [2]-[8]. Reducing HBT LNA noise figure will make all-HBT 200-300 GHz receivers more competitive and, in hybrid receivers using a HEMT LNA and an HBT IC for the post-LNA and remaining receiver mm-wave stages, will minimize the required gain, hence number of stages, in the HEMT LNA. Here we present 200 GHz LNAs with low DC power consumption and record low noise for HBTs. We report common-base (CB) (Fig. 1) and common-emitter (CE) designs (Fig. 2). The CB design shows 7.4±0.7 dB noise figure over 196-216 GHz, 14.5 dB gain and -21.1 dBm P_{in1dB} at 200 GHz, and dissipates 9.2 mW. The CE design shows 7.2±0.4 dB noise figure over 196-216 GHz, 13 dB gain and -18.2 dBm P_{in1dB} at 200 GHz, and dissipates 19.2 mW.

In designing a multi-stage LNA for low total (cascaded) noise figure, the individual stages should be designed for lowest noise measure (M), not lowest noise figure (F), as this minimizes the total noise contribution of input and subsequent LNA gain stages. Passive element losses at 200GHz can significantly contribute to the LNA's total noise contribution, hence the LNA should be designed for minimum loss in the input matching network. The design procedure is therefore critical.

II. Low Noise Amplifier Design

LNAs were fabricated in the Teledyne 250 nm InP technology [1], which has four Au interconnect layers, 50 Ω/square thin film resistors and 0.3 fF/μm^2 MIM capacitors.

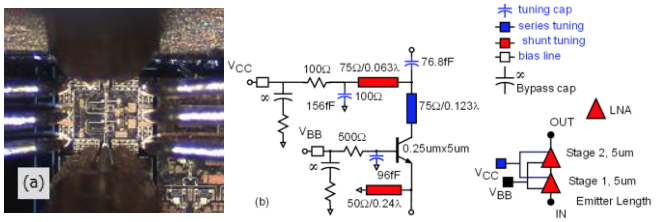

Fig. 1. Common-base amplifier: die photo (a) and amplifier circuit diagram (b). The die area, including DC routing and pads is 0.49 mm x 0.425 mm.

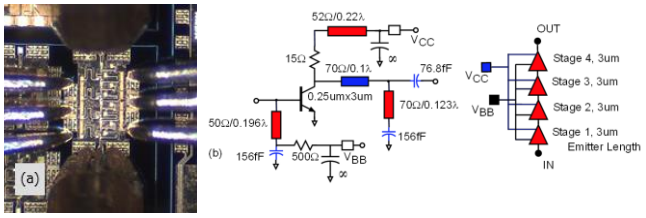

Fig. 2. Common-emitter amplifier: die photo (a) and amplifier circuit diagram (b). The die area, including DC routing and pads is 0.450 mm x 0.630 mm.

The HBT has a maximum 650 GHz power gain cut-off frequency (f_{max}), a maximum 3 mA/μm current density and the 4.5 V BV_{CEO}.

A. Noise Measure Technique

Transistor noise measure $M = (F-1)(1-G^{-1})^{-1}$ [10], where G is the gain, sets a lower bound for the cascaded noise figure F_{cascade} of a multi-stage LNA.

$$F_{\text{cascade}} = M + 1 = F + \frac{F-1}{G} + \frac{F-1}{G^2} + \cdots = \frac{F-G^{-1}}{1-G^{-1}}$$

Further, if the embedding circuit is passive, lossless, and reciprocal, the minimum noise measure is independent of the surrounding circuit [10]. In particular, if passive element losses are negligible, the minimum F_{cascade} and M are identical in common-emitter and common-base configurations, and do not change if the stage is unilateralized or capacitively neutralized, or if gain is maximized using Singhakowinta's technique [11].

Given that F_{cascade} is independent of the stage configuration, we instead select the stage configuration based on either high feasible bandwidth or high gain per stage. The CB stage provides greater gain/stage, hence noise contributions associated with loss in the output matching network are reduced. Further, with greater gain per stage, fewer stages are required, reducing DC power. Because the CE stage has lower output impedance, its output matching network is more readily designed for wide bandwidth.

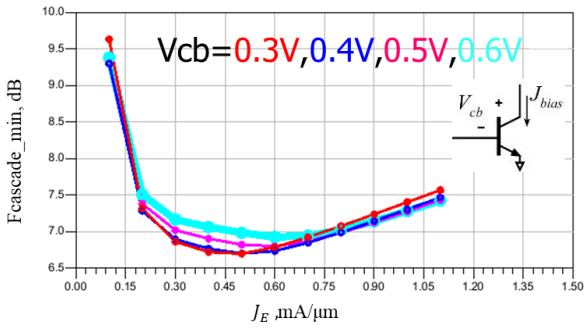

Fig. 3. Minimum F_{cascade} as a function of emitter current density (J_E) and collector-base voltage (V_{CB}) for a 0.25 μm x 5 μm HBT.

B. Determining Bias Condition

Most widely-used RF computer-aided design programs compute $F_{\min}$ but not $M_{\min}$, and compute F but not M as a function of source impedance. As will be subsequently described, Python scripts were written to compute these quantities from the output of the CAD simulation software. Given this, the first step in the design is to determine, from CAD simulation, the emitter current density and collector-base voltage giving the lowest $M_{\min}$, hence the lowest F_{cascade}, at 200 GHz (Fig. 3). For the IC technology used, at 210 GHz, the simulated minimum F_{cascade} is 6.7 dB with $J_E = 0.5$ mA/μm and $V_{CB} = 0.4V$.

C. Area Scaling, Base Capacitive Degeneration, and Input Matching Network

In common-emitter LNAs, an appropriate nonzero emitter inductive reactance $j\omega L_E$ allows input tuning for zero input reflection coefficient simultaneously with tuning for minimum F_{cascade}, doing so without increasing the minimum F_{cascade}. In common-base, a nonzero base capacitive impedance $1/j\omega C_{base}$ plays exactly the same role.

Subsequently, the HBT junction area is scaled, together with the DC current and the base capacitor, so that the source conductance for minimum noise measure is 20 mS (Fig. 4); this permits the input stage to be noise-matched to 50 Ω with a single inductive shunt element (Fig. 5), avoiding the added attenuation, hence the added noise, of a series matching element.

D. Displaying source impedance for minimum M

As with F and G_A (available gain), M can also be represented as a function of source reflection coefficient, displaying circles as contours of constant M [12]. Because widely-used RF computer-aided design programs do not provide this capability, a Python script was written to

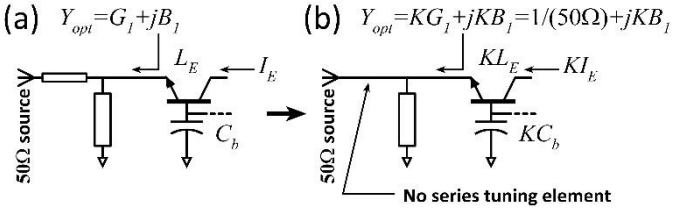

Fig. 4. (a) Input matching network without proper emitter junction area scaling (b) Input matching network with proper emitter junction area scaling.

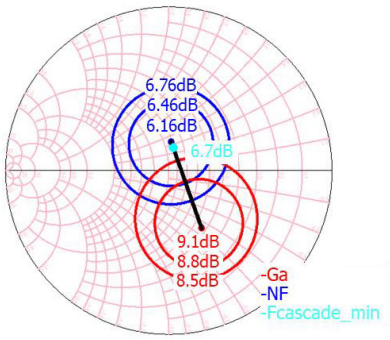

Fig. 5. CAD display, in Keysight ADS, of the contours of constant noise figure and available gain (G_A) in the plane of the source reflection coefficient. A Python script draws a line (black) between the centers of the F and G_A circles, computing the minimum noise measure along this line. Data is for an (0.25 x 5 μm^2) HBT in CB configuration with 200 fF base capacitance biased at V_{CB}=0.4 V and J_E=0.5 mA/μm.

approximately determine the minimum noise measure, and the associated source impedance, from the contours of constant F and G_A (Fig. 5). The script draws a line between the centers of the F and G_A circles, calculates M for each point on this line, and determines the point on the line having the smallest M.

If the F and G_A circles were exactly concentric, the impedance for minimum M would lie along the line so constructed, and this simple graphical algorithm would exactly determine $M_{\min}$ and the associated impedance. Graphically, we observe (Fig. 5) that the circles do not strongly deviate from this assumption. A more exact procedure would use the relationships of [12].

E. Output Matching Network

In a multistage LNA design, for lowest noise, each stage output is matched to the minimum noise measure impedance of the cascaded stage. This can be accomplished in a stage-by-stage design procedure in which each stage is designed to have minimum M for a 50 Ω external source impedance and maximum associated gain for a 50 Ω external load impedance.

LNA design must however balance noise against bandwidth and dynamic range. Consequently, the output tuning of the CB design was adjusted to increase the stage bandwidth and the 1dB gain compression point.

III. MEASUREMENT RESULTS

A. S-Parameter Measurements

Fig.1-2 show the chip micrographs. Measurements are performed on the 3-mil thinned die. S-parameters were measured using a Keysight network analyser with 220-325 GHz Oleson WR-03 frequency extender modules and 325 GHz GGB wafer probes. A short-open-load-thru (SOLT) calibration standard on an external substrate moves the reference plane to the probe tips.

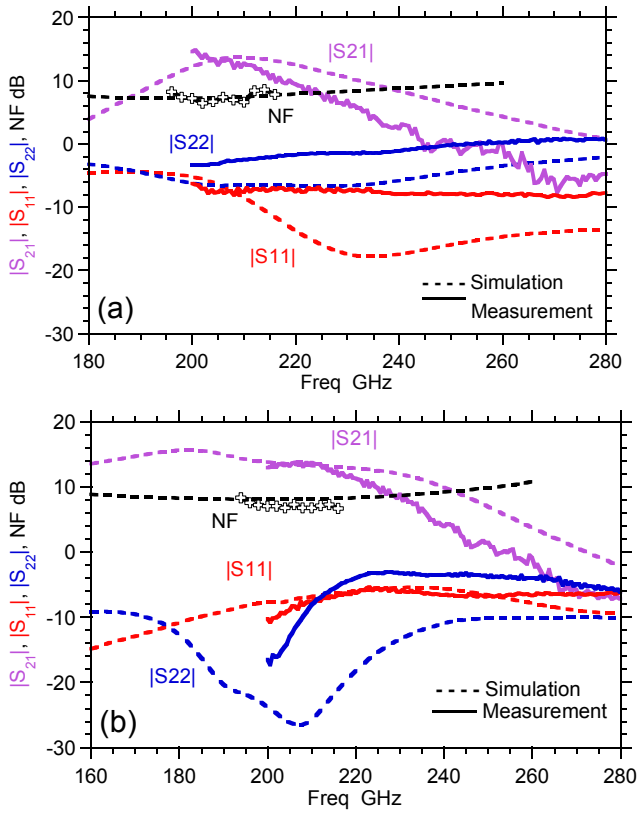

Fig. 6. Measured (solid) and simulated (dashed) S-parameters and NF: (a) common-base and (b) common-emitter amplifier.

Approximately 5% frequency downshift is observed between the amplifier's measured and simulated S-parameters (Fig. 6). The device model does not include base inductance, which is the main reason of the frequency shift. By adding extra series inductance to the base, the device model is adjusted.

The CB amplifier (Fig. 1) was biased at (V_{CCLNA}=1.5 V, I_{CCLNA}=6.03 mA, V_{BBLNA}=0.85 V, I_{BBLNA}=0.264 mA). The peak measured small-signal gain ($|S_{21}|$) is 14.5 dB at 200 GHz, in good agreement with simulation. The CE amplifier (Fig. 2) was biased at (V_{CCLNA}=1.6 V, I_{CCLNA}=11.68 mA, V_{BBLNA}=0.87 V, I_{BBLNA}=0.436 mA). The peak measured small-signal gain ($|S_{21}|$) is 13.69 dB at 206 GHz. The CB amplifier has a narrower bandwidth due to the higher CB output impedance.

B. Power Measurements

Fig. 7 shows the procedure for gain compression measurements [13], and the setup in the calibration and measuring phases are shown in Fig. 7. The ~200 GHz DUT excitation signal is generated by a synthesized microwave signal generator (N5183B) and an 8:1 VDI frequency multiplier. The signal is passed through a directional coupler to monitor the input power, and is passed through a G-band fixed attenuator to obtain power levels within the desired range to drive the LNA. By placing an Erickson power meter (PM4) at the attenuator output, and comparing its power measurement to that of the spectrum analyzer, the measurement of input power is thereby calibrated (Fig. 7a). The signal source is then

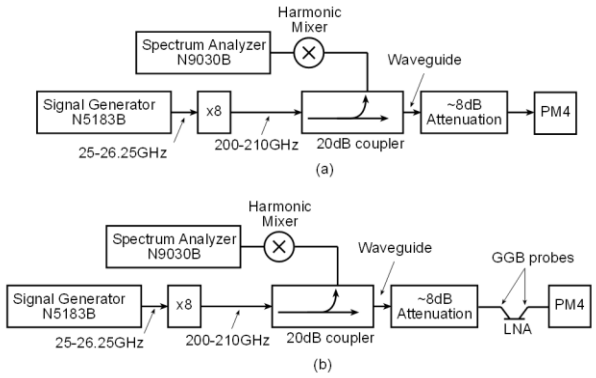

Fig. 7. Power measurement setup: a) calibration phase b) measurement phase.

connected, via GGB probes, to the amplifier input, and the amplifier output monitored by the PM4 power meter.

The CB and CE amplifiers are biased at (V_{CCLNA}=1.5 V, I_{CCLNA}=5.98 mA, V_{BBLNA}=0.864 V, I_{BBLNA}=0.268 mA) and (V_{CCLNA}=1.6 V, I_{CCLNA}=11.73 mA, V_{BBLNA}=0.87 V, I_{BBLNA}=0.522 mA) respectively. The CB and CE amplifiers have -21.1 dBm, and -18.2 dBm input referred P_{1dB} with 12.69 dB and 13.3 dB associated gain, respectively, at 200 GHz (Fig. 10a). At 210 GHz, the input referred P_{1dB} is -17.47 dBm (CB) and -19.08 dBm (CE) with 10.31 dB (CB) and 13.07 dB (CE) associated gain. The CB amplifier consumes 9.2 mW while the CE amplifier consumes 19.22 mW.

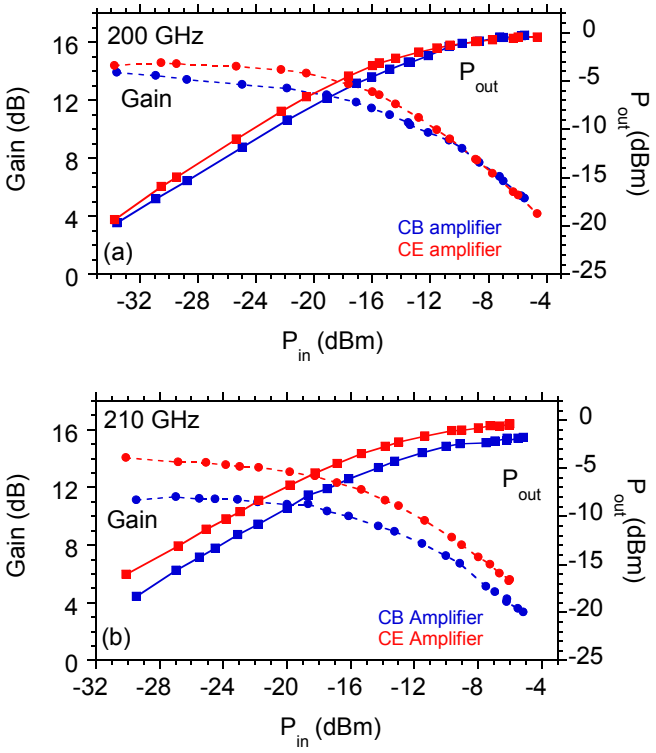

Fig. 8: Gain compression characteristics at (a) 200 GHz and (b) 210 GHz.

Table 1. Comparison of recently published >150 GHz low noise amplifiers

Ref.	Technology	Topology	Freq (GHz)	Gain (dB)	Gain/stage (dB)	NF (dB)	P_{DC} (mW)
[2]	250nm SiGe HBT	Cascode, diff. mode	156	26	8.7	8.5	-
[3]	50 nm mHEMT	CS	178-185	24.5	4.9	3.5	24
[4]	50 nm mHEMT	CS	206	16	4.0	4.8	-
[5]	32nm CMOS	CS	200-220	10-18	1.4-2.6	11	44.5
[6]	130nm Sige HBT	Cascode, diff. mode	220	18	6	16	151.2
[8]	250nm InP HBT	CE	265	24	4.8	10	81.7
[9]	250nm InP HBT	Cascode	288	8.4	8.4	11.2 at 300 GHz	-
This work	**250nm InP HBT**	CE	200	13	3.25	7.2	19.22
		CB	200	14.5	7.25	7.4	9.2

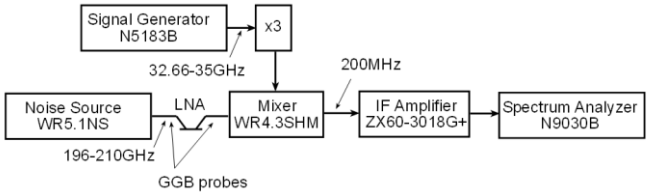

Fig. 9. Noise measurement setup.

C. Noise Measurements

The LNA noise figure is measured using the hot/cold Y-parameter method (Fig. 11). A VDI-WR5.1NS hot/cold noise source connected to the LNA input using a GGB 140-220 GHz wafer probe. The G-band probe loss is measured by landing probes on the through structure on the impedance standard substrate. The probe loss is found to be 2.0 dB loss at 200 GHz, and is deembedded from the measured noise figure. A ~20 dB low-noise post-amplifier (Mini Circuits, ZX60-3018G+) used to reduce the noise contribution from the spectrum analyzer. The subharmonic mixer's (VDI-WR4.3SHM) LO-signal was supplied by a QuinStar x3 WR-8.0 multiplier chain (QMM-933510030) and a signal generator (N5183B). The output noise power spectral density was measured at 200 MHz using a spectrum analyser (N9030B). The CB amplifier (Fig. 6a) shows 7.4±0.7 dB noise figure over 196-216 GHz, while the CE amplifier (Fig. 6b) shows 7.2±0.4 dB noise figure over 196-216 GHz.

Table 1 compares the performance of the low noise amplifier designed above 150 GHz. The amplifiers in Table 1 are the best reported in their respective transistor technology to the authors' knowledge.

IV. Conclusion

200 GHz low noise amplifier ICs in common-base and common emitter topologies were presented with record noise figure 7.4±0.7 dB over 196-216 GHz (CB) and 7.2±0.4 dB over 196-216 GHz (CE) in HBT technology.

Acknowledgment

This work was supported by ComSenTer, a JUMP program sponsored by the Semiconductor Research Corporation. The authors thank Teledyne Scientific & Imaging for the IC fabrication.

References

[1] M. J. W. Rodwell et al., "100-340GHz Systems: Transistors and Applications," in Proc. IEEE IEDM, 2018, pp. 14.3.1-14.3.4

[2] Y. Zhao, E. Ojefors, K. Aufinger, T. F. Meister and U. R. Pfeiffer, "A 160-GHz Subharmonic Transmitter and Receiver Chipset in an SiGe HBT Technology," in IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 10, pp. 3286-3299, Oct. 2012.

[3] G. Moschetti et al., "A 183 GHz Metamorphic HEMT Low-Noise Amplifier With 3.5 dB Noise Figure," in IEEE Microwave and Wireless Components Letters, vol. 25, no. 9, pp. 618-620, Sept. 2015.

[4] A. Tessmann, A. Leuther, H. Massler, M. Kuri and R. Loesch, "A Metamorphic 220-320 GHz HEMT Amplifier MMIC," 2008 IEEE Compound Semiconductor Integrated Circuits Symposium, Monterey, CA, USA, 2008, pp. 1-4.

[5] Z. Wang, P. Chiang, P. Nazari, C. Wang, Z. Chen and P. Heydari, "A CMOS 210-GHz Fundamental Transceiver With OOK Modulation," in IEEE Journal of Solid-State Circuits, vol. 49, no. 3, pp. 564-580, March 2014.

[6] E. Ojefors, B. Heinemann and U. R. Pfeiffer, "Subharmonic 220- and 320-GHz SiGe HBT Receiver Front-Ends," in IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 5, pp. 1397-1404, May 2012.

[7] K. Eriksson, S. E. Gunnarsson, V. Vassilev and H. Zirath, "Design and Characterization of HH-Band (220–325 ~~GHz) Amplifiers in a 250-nm InP DHBT Technology," in IEEE Transactions on Terahertz Science and Technology, vol. 4, no. 1, pp. 56-64, Jan. 2014.

[8] J. Hacker et al., "THz MMICs based on InP HBT Technology," 2010 IEEE MTT-S International Microwave Symposium, Anaheim, CA, USA, 2010, pp. 1126-1129.

[9] M. Urteaga, Z. Griffith, M. Seo, J. Hacker, M. Rodwell, "InP HBT Technologies for THz Integrated Circuits", Proceedings of the IEEE, Vol. 105, No. 6, pp 1051-1067 June 2017.

[10] H. A. Haus and R. B. Adler, "Optimum Noise Performance of Linear Amplifiers," in Proceedings of the IRE, vol. 46, no. 8, pp. 1517-1533, Aug. 1958.

[11] A. Singhakowinta & A. R. Boothroyd, "Gain Capability of Two-port Amplifiers", International Journal of Electronics, Volume 21, Issue 6, 1966, pages 549-560.

[12] H. Fukui, "Available Power Gain, Noise Figure, and Noise Measure of Two-Ports and Their Graphical Representations," in IEEE Transactions on Circuit Theory, vol. 13, no. 2, pp. 137-142, June 1966.

[13] A. S. H. Ahmed, U. Soylu, M. Seo, M. Urteaga, J. F. Buckwalter and M. J. W. Rodwell., " A 190-210GHz Power Amplifier with 17.7-18.5dBm Output Power and 6.9-8.5% PAE.," in press, Proc. IMS2021.