An 18-GHz Continuous-Time Σ–Δ Analog–Digital Converter Implemented in InP-Transferred Substrate HBT Technology

Shrinivasan Jaganathan, Sundararajan Krishnan, Dino Mensa, Thomas Mathew, Yoram Betser, Yun Wei, Dennis Scott, Miguel Urteaga, and Mark Rodwell

***Abstract*—We report an 18-GHz clock-rate second-order continuous-time Σ–Δ analog–digital converter (ADC) implemented using InP-transferred substrate HBTs. Under two-tone test conditions, the ADC achieved 43 dB and 33 dB SNR at signal frequencies of 500 MHz and 990 MHz, respectively. The IC occupied 1.95 mm^2 die area and dissipated ∼1.5 W.**

***Index Terms*—ADC, delta–sigma, heterojunction bipolar transistor, substrate transfer.**

I. Introduction

HIGH speed analog-to-digital converters (ADCs) find widespread applications in wideband communications and radar receivers. Efforts are being made to move the ADC forward in the signal chain, closer to the antenna. Such efforts depend critically on the ability to digitize wideband signals with very high resolution. This modified architecture should result in a more robust receiver implementation consisting of the ADC followed by DSP hardware and software.

A popular oversampling ADC architecture is based on Σ–Δ modulation. These achieve high signal/noise ratio (SNR) without requiring high precision in component values or device matching. Moreover, the requirements on the analog anti-aliasing filter are significantly relaxed. Σ–Δ modulators achieve high resolution by utilizing high sampling rates; a second-order ADC achieves a 15-dB improvement in SNR for every octave increase in sampling rate.

The SNR of a Σ–Δ modulator depends on the order of the loop filter and the oversampling ratio [1]. While a high-order loop-filter results in a high SNR, it is difficult to design a stable modulator with order greater than two. High SNR can be obtained by using a second-order filter and as high an oversampling ratio as permitted by the technology of implementation. This is our approach. We seek as high a clock rate as is feasible in the technology, so as to obtain a high resolution; an ideal second-order ADC at 18-GHz clock would exhibit 10 effective number of bits (ENOB) resolution at 200 MHz and 6.8 ENOB resolution at 500 MHz.

InAlAs/InGaAs transferred-substrate heterojunction bipolar transistors (HBTs) have achieved very high device bandwidths [2], [3], permitting very high speed digital circuits [12]. In bipolar processes, fast, low-offset switches are difficult to implement, and the continuous-time architecture [4] is more readily implemented than the discrete-time, switched-capacitor architecture prevalent in CMOS Σ–Δ ADCs. Continuous-time Σ–Δ modulators have been reported with clock rates as high as 3.2 GHz [5] and 5 GHz [6]. Raghavan *et al.* [7] recently reported a fourth-order bandpass delta–sigma modulator operating at a clock rate of 4 GHz. Here we report an 18-GHz clock-rate, second-order continuous-time Σ–Δ ADC.

II. Device Technology

We obtained high ADC clock frequencies by using very wide bandwidth bipolar transistors. As with MOS transistors, high HBT cutoff frequencies are obtained by scaling. Scaling for high current-gain cutoff frequencies f_τ requires thinning the base and collector epitaxial layers, increasing the bias current density, and decreasing the extrinsic emitter resistance [8]. HBTs are typically fabricated using a series of mesa etches; this produces a device whose collector-base junction lies beneath both the emitter stripe and the base Ohmic contacts. Reducing the collector junction width results in reduced base contact dimensions, and the base contact resistivity must then be greatly decreased if low base resistance is to be maintained. By using a substrate transfer step, HBTs can be fabricated with narrow emitter-base and collector-base junctions on opposing sides of the base epitaxial layer [2].

Single heterojunction bipolar transistors (SHBTs) fabricated in the transferred-substrate process use InAlAs emitters, InGaAs base layers, and InGaAs collectors. Devices fabricated using electron-beam lithography have obtained 200 GHz f_τ [9], over 800 GHz $f_{\max}$ [2], and 21-dB unilateral power gain at 100 GHz [9]. ICs fabricated in the process to date have used 0.5-μm-resolution optical projection lithography, and have obtained simultaneous 295 GHz f_τ and $f_{\max}$ [3] for devices with thin base and collector layers. The SHBTs have a low ∼1.5-V common-emitter breakdown $V_{\mathrm{br,ceo}}$, which requires careful control of bias voltages within the ADC. We have recently fabricated double heterojunction bipolar transistors (DHBTs) with InP collectors using the substrate transfer process, and

Manuscript received January 15, 2001; revised April 12, 2001. This work was supported by the ONR under Grant N00014-98-1-0830.

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Publisher Item Identifier S 0018-9200(01)06105-4.

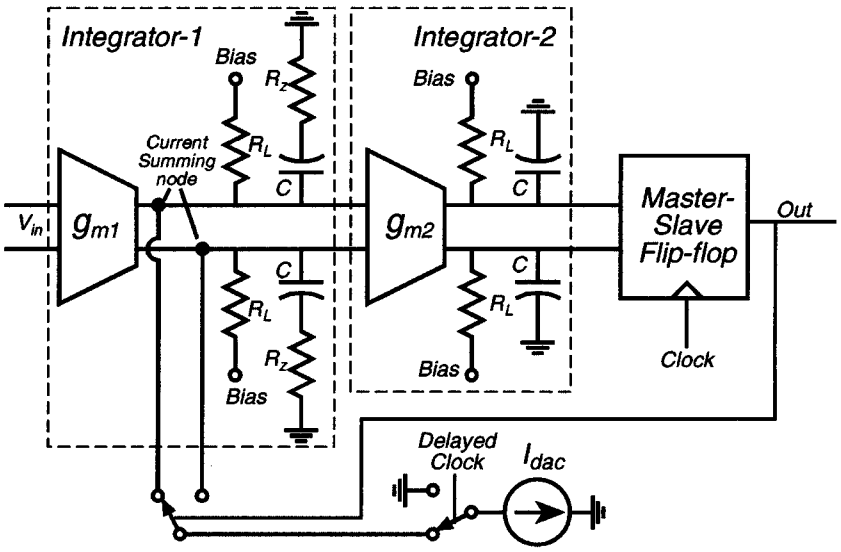

Fig. 1. A block diagram of second-order continuous-time Σ–Δ ADC.

have obtained $V_{\mathrm{br,ceo}} > 5$ V at 10^5 A/cm^2, 165 GHz f_τ, and 300 GHz $f_{\max}$ [10], but have not yet fabricated ADCs with these transistors. The ADCs reported here use SHBTs with a 4×10^{19} cm^{-3} Be-doped base of 300 Å thickness and with $2kT$ band-gap grading. The collector has a 2000 Å thick InGaAs depletion layer, and uses a Schottky collector contact. The HBTs have $\sim$0.6-μm emitter junction width and 1.5-μm collector junction width.

In mixed-signal ICs, digital circuit switching transients couple to the analog circuits through the power supply or ground connections, degrading the ICs dynamic range. Differential circuits reduce—but do not eliminate—such coupling. In small-scale millimeter-wave ICs [11], circuit–circuit coupling through ground circuit common-lead inductance ("ground bounce") is greatly reduced through use of a microstrip wiring environment, in which all circuit ground-return currents are carried on a low-inductance ground plane on the back surface of the IC. In the substrate transfer process, a continuous, unbroken, ground plane lies under the full IC area, providing a low inductance ground system for low circuit–circuit coupling. The wiring dielectric is a 5-μm-thick Benzocyclobutene (BCB) layer with $\epsilon_r = 2.7$. All interconnects are microstrip lines, and have a well-controlled and predictable characteristic impedance; a 3-μm-width conductor forms a $Z_0 = 100\ \Omega$ transmission line.

III. Circuit Design

Fig. 1 shows a simplified block diagram of the IC. The ADC consists of two transconductance (g_m) cells, each followed by a passive integrator. The quantizer is a master–slave flip-flop, while the feedback DAC is a current steering differential amplifier. The error signal is generated by current summing at the output nodes of the first transconductance cell. The entire implementation is differential for low even-order harmonic distortion, high power supply rejection ratio and reduced clock switching noise.

In computer simulations of Σ–Δ ADCs, several thousand clock cycles must be simulated to obtain, by fast Fourier transformation (FFT), spectra with the required dynamic range. At the time of IC design, available computers were inadequate for full transistor-level loop simulations, and the preliminary design was instead carried out using system-level simulations using MATLAB. Such simulations indicated the required parameters for each loop element for a desired ADC signal/noise ratio. These parameters were translated into circuit component values using a transistor-level circuit simulator. Fig. 2 shows a simulation of a near-ideal second-order Σ–Δ ADC with a 20-GHz clock rate. The effects of comparator metastability and dynamic hysteresis, thermal and shot noise, and integrator excess delay are neglected, but the simulation does include the effects of integrator leakage (finite integrator gain), with the integrator transfer functions being modeled as $A_{int} = A_{\mathrm{DC}}/(1+jf/f_0)$, with $A_{\mathrm{DC}} = 30$ dB and $f_0 = 50$ MHz. Integrating the noise and signal density from MATLAB over frequency results in 55 dB of SNR for a 312.5 MHz signal. The various circuit imperfections should, however, reduce this SNR considerably.

Fig. 3 shows the circuit schematic for the second integrator in the loop. Since noise shaping near dc is limited by the finite dc gain of the integrators [1], high gains are desired. Integrator excess phase delay limits the high frequency noise-shaping and hence limits the maximum oversampling ratio. Low excess phase delay and hence wide integrator bandwidth are desired in addition to high dc gain for high oversampling ratio Σ–Δ ADCs.

In the absence of PNP transistors in an HBT technology, achieving a high dc gain is challenging. Usually, designers overcome this limitation by employing bootstrapped [5] or negative-resistance loads. These techniques introduce higher order poles, resulting in excess phase delay and thus limiting the oversampling ratio. They also increase the transistor count in the high frequency signal path, which is undesirable in very wideband circuits. Here, high dc gain is obtained simply by using a large pull-up resistive load. This necessitates a large positive power supply voltage and an (off-wafer) common-mode-feedback (CMFB) loop that controls the integrator dc bias. This is

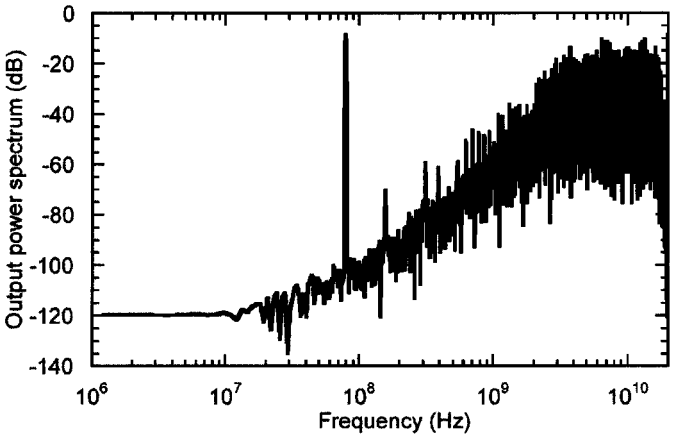

Fig. 2. Simulation result: FFT of the output of an ideal second-order Σ–Δ modulator loop for $f_{\rm clock} = 20$ GHz, $f_{\rm signal} = 78$ MHz, 1.22 MHz FFT bin (resolution). Integrator leakage is modeled.

important given the small breakdown voltage of the InGaAs collector HBTs.

The integrator is a g_m stage whose output is loaded by a grounded capacitor (Figs. 1 and 3). Active integrators (using a cascaded pair of g_m stages whose second stage has a Miller-connected integrating capacitor), used commonly in Σ–Δ modulator designs, obtain a very high dc gain ($g_m^2 R_L^2$ vs. $g_m R_L$) but have a lower feasible bandwidth due to the loop-bandwidth and loop-stability considerations associated with the Miller feedback loop. In contrast, the integrator reported here uses a simple g_m stage loaded by a capacitor, achieving a high bandwidth.

Excess delay due to higher order integrator poles associated with transistor parasitics is partly offset by a zero in the transfer function introduced by placing a resistor in series with the capacitor. Emitter followers (Fig. 3) buffer the integrator inputs, increasing the input impedance and the dc gain. Because the output impedance of the emitter follower is higher than that of the drive point ($1/j\omega C_{int}$) at high frequencies, the emitter followers are removed from the signal path at high frequencies by feed-forward compensation. The common-mode voltage at the output for CMFB, is sensed with high value on-chip resistors. SPICE simulations (Fig. 4) of the integrator, with all layout parasitics modeled, show a ($g_m/j\omega C_{int}$) behavior from 40 MHz to ∼100 GHz.

The goal of this design is to use the maximum possible clock frequency. Limits to the clock frequency include the uncompensated excess delay accumulated in the signal path , metastability and dynamic hysteresis errors in the quantizer. The excess delay in the signal path includes the delay due to integrator higher order poles, the delay in the interconnects, and the delay in the quantizer decision and the feedback DAC.

A fully differential DAC eliminates feedback errors associated with unequal DAC rise and fall times [5]. However, the DAC is still vulnerable to quantizer metastability errors. Such errors result in the output edge of the quantizer being modulated by the input amplitude. For small quantizer inputs, the quantizer output can take several circuit time-constants to reach the correct logic level. For strong inputs, this delay is reduced. For a quantizer output corresponding to logic **1**, the DAC charge delivered to the integrating capacitor varies with the strength of quantizer input

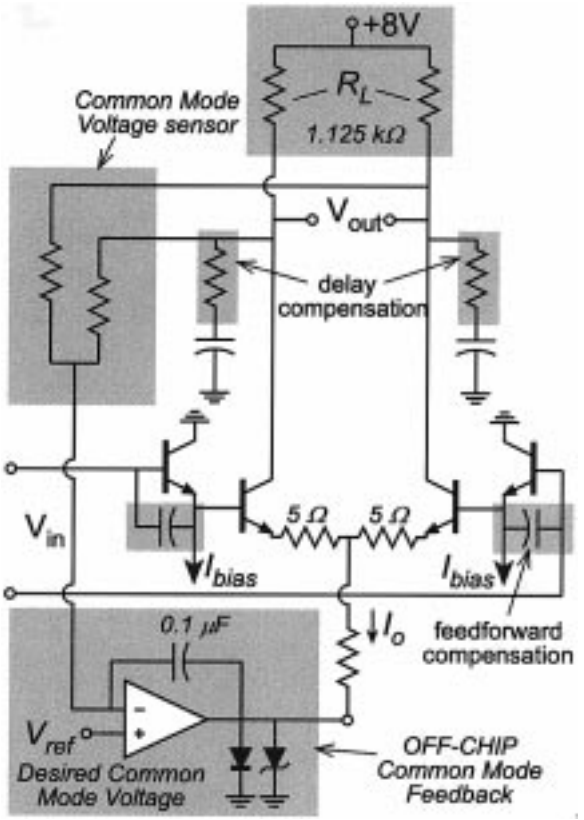

Fig. 3. A schematic of the second integrator in the loop.

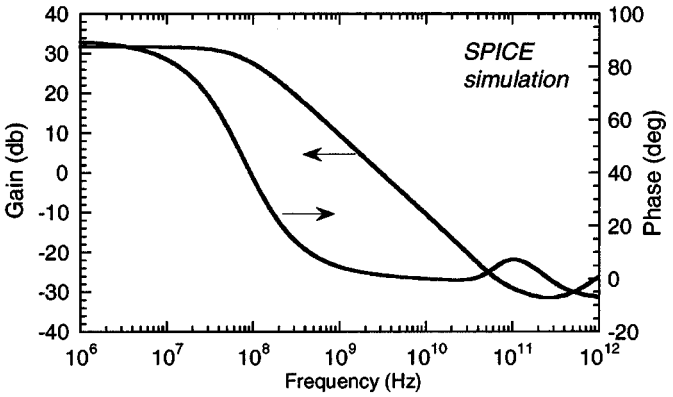

Fig. 4. Plot of frequency response of the second integrator.

(shown qualitatively in Fig. 5). One method to reduce such errors is to add another latch stage for further regeneration [5]. A second method, used here, is a delayed return-to-zero (RTZ) DAC. The RTZ DAC is gated with a clock pulse delayed such that the DAC is active only in the final 50% of the clock period (Fig. 5). We use a gated DAC because less additional transistors (∼6) are required than for an extra latch stage (∼25).

The use of either an RTZ DAC or an extra latching stage results in an extra half-clock cycle delay in the feedback path, adding to other excess loop delays, and thus limiting the clock rate. Using MATLAB, we observed a 12-dB reduction in SNR with the addition of a half-sample delay (25-ps delay for a 20-GHz clock) in the loop. Together with the excess loop delays

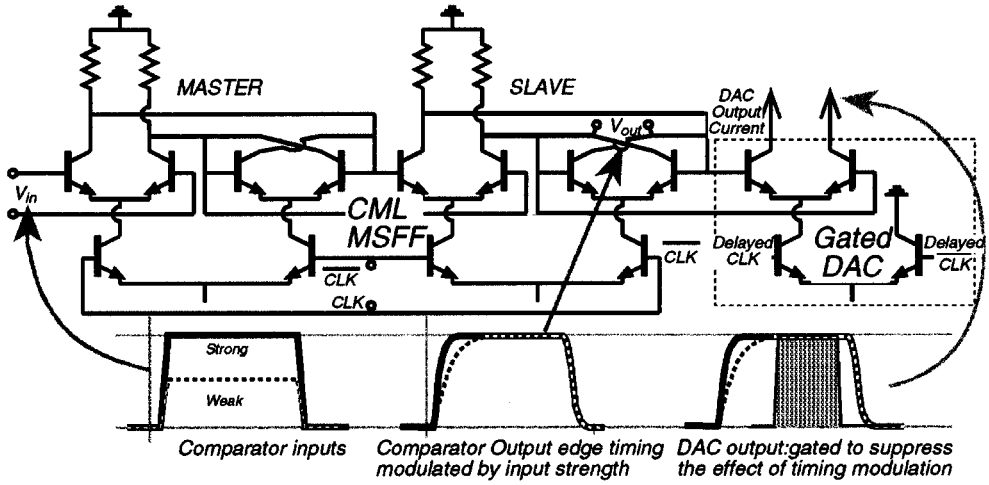

Fig. 5. A qualitative description of metastability in the flip-flop, with RTZ DAC as the proposed solution. While CML flip-flop is shown for simplicity, the circuit uses an ECL flip-flop.

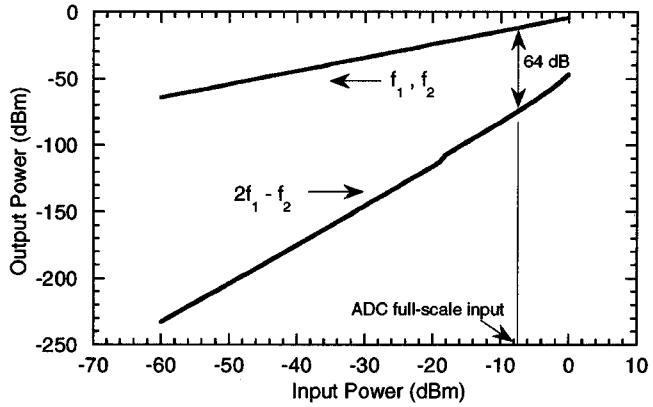

Fig. 6. Circuit simulation results for the linear response and third-order distortion $(2f_1 - f_2)$ of the input transconductance stage, given input signals $(f_1,\ f_2)$ of approximately 100 MHz.

associated with the integrators and the interconnects, this delay is compensated to first order in frequency by introduction of a zero in the transfer function, through addition of a resistor in series with the second-stage integration capacitor. Given compensation of loop delays with insertion of a zero in the loop transmission, MATLAB simulations indicate <3-dB SNR degradation for <30-ps loop delay, given a 20-GHz clock.

The first g_m stage is outside the Σ–Δ loop, hence its nonlinearity directly degrades the ADC linearity. Jensen [5] reported a linearized g_m stage using Caprio's cell. The Σ–Δ modulator reported here eliminates this in favor of a differential pair with its smaller transistor count (yield limits in a university process). Given this simple input stage, intermodulation is reduced by selecting an input stage bias current (6 mA) significantly larger than the switched current of the feedback DAC (2 mA). Given that the DAC is gated on only for 50% of the clock period, the input stage overloads at signal levels 6:1 larger than that of the subsequent Σ–Δ loop. Overload and resulting intermodulation distortion in the input stage is thus reduced. Circuit simulations (Fig. 6) indicate 64 dBc suppression of two-tone intermodulation arising from the input stage. For input signal levels near the ADC full-scale input, intermodulation is then dominated by distortion in the subsequent loop.

The input stage also contributes thermal and shot noise, and can limit the SNR. Referring to the partial circuit schematic of Fig. 7, the ADC total input-referred noise voltage arising from thermal and shot noise has a spectral density given by

$$\begin{aligned}\frac{d\langle E_n^2\rangle}{df} \simeq\ & 4kT(kT/qI_c) \\ & + 8kT(R_{\rm deg} + R_{ex} + R_{bb} + Z_0/2) \\ & + 4qI_b(R_{\rm deg} + R_{ex} + R_{bb} + Z_0/2)^2 \\ & + (8kT/R_{cs})\gamma^2(R_{\rm deg} + R_{ex} + kT/qI_c)^2 \\ & + 4kT\left(\frac{kT}{qI_{\rm DAC}/2}\right)\frac{(R_{\rm deg} + R_{ex} + kT/qI_c)^2}{R^2_{\rm cs,\,DAC}} \\ & + 8kT\frac{(R_{\rm deg} + R_{ex} + kT/qI_c)^2}{R_{\rm cs,\,DAC}},\end{aligned}$$

where

I_c	input stage bias current;
I_b	base current;
R_{bb}	input-stage base resistance;
$Z_0 = 50\,\Omega$	input interface impedance;
$I_{\rm DAC}$	DAC switched current;
γ	fractional imbalance in dc bias currents in the input differential pair.

Comparing this input noise to the maximum input voltage before ADC overload, $V_{\rm in,\,max} = I_{\rm DAC}(R_{\rm deg} + R_{ex} + kT/qI_c)$, ($P_{\rm in,\,max} = -7.5$ dBm) given the IC design values, the thermal and shot noise limits the SNR to 153 dB (1 Hz). This should be compared to the quantization-noise limited SNR, 143 dB (1 Hz) at 200 MHz signal frequency, for an ideal second-order Σ–Δ ADC at 20-GHz clock rate (Fig. 2). Comparing this input-referred noise to kT, -173.8 dBm (1 Hz), the input stage has a calculated 14-dB noise figure. In the present design, thermal noise from the DAC current mirror and thermal noise in the input degeneration resistance $R_{\rm deg}$ dominate.

A simple ECL master–slave flip-flop (demonstrated to operate as a divide-by-two at 75 GHz [13]) was used as the quantizer. The gated DAC is a simple ECL OR gate with open-col-

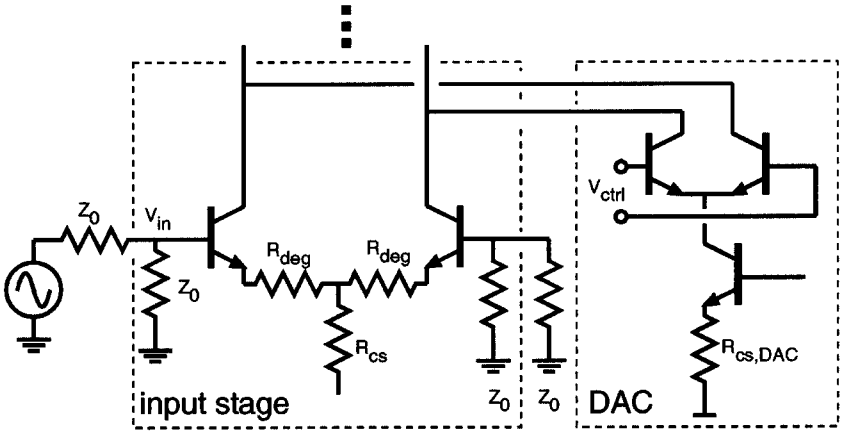

Fig. 7. Detail of input g_m stage and RTZ DAC for noise analysis.

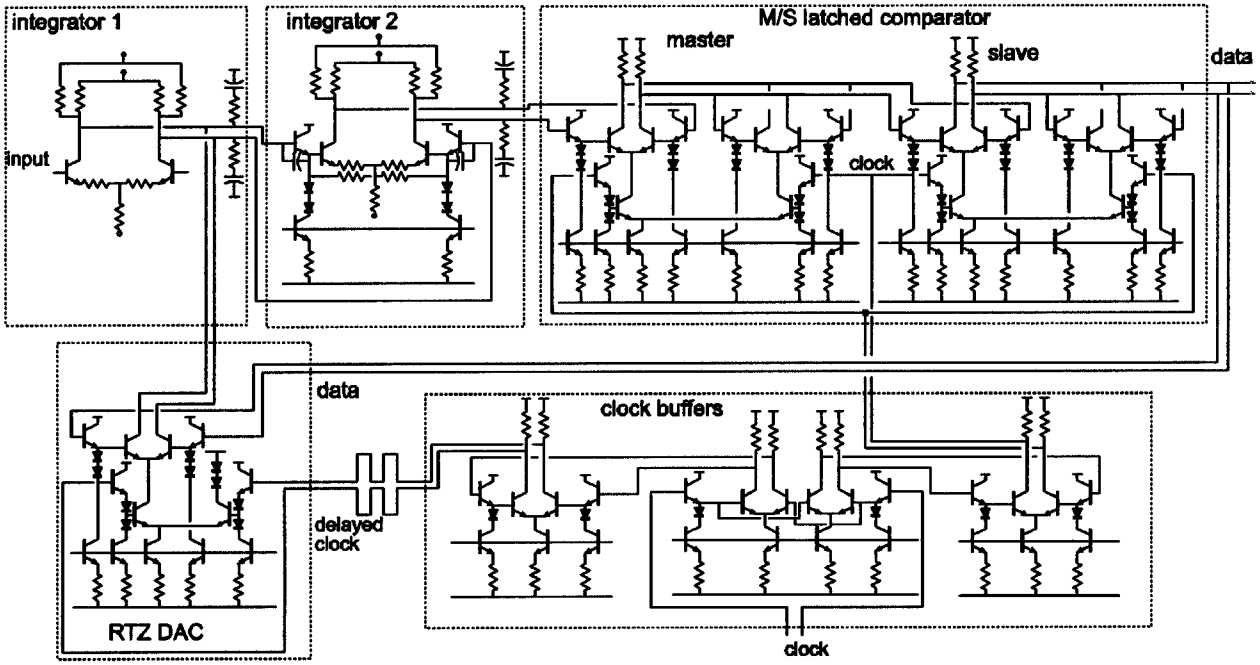

Fig. 8. Simplified ADC circuit diagram (omitting current mirror references and microstrip-line terminations).

lector outputs. The final design parameters were: $g_{m1} = 15$ mS, $g_{m2} = 65$ mS, average DAC feedback current $I_{\rm DAC} = 2$ mA, nominal pull-up resistors $R_L = 1.125\,\text{k}\Omega$, clock frequency $f_c = 20$ GHz and integrating capacitors $C = 3$ pF. A simplified IC schematic is shown in Fig. 8.

IV. Measurement and Results

The HBTs on the fabricated IC wafer had a typical dc current-gain, $\beta \geq 100$, current gain cut-off frequency, $f_\tau \approx 190$ GHz, and power gain cut-off frequency, $f_{\max} \approx 200$ GHz at an emitter current density of $\sim 10^5$ A/cm^2. The common-emitter breakdown voltage, $BV_{\rm CEO}$, was $\sim$1.4 V. Nichrome resistors had resistance approximately 20% lower than design values.

The IC was tested by on-wafer probing using 40 GHz probe cards. The photograph of the die is shown in Fig. 9. The standard technique for testing Σ–Δ modulators uses a fast logic analyzer to acquire the digital data stream. Testing under two-tone conditions permits simultaneous measurement of SNR and two-tone third-order distortion. The captured data is analyzed by FFT for its spectral content. Due to the lack of a logic analyzer with sufficient bandwidth for capturing 18-GHz data, we were forced to use an analog spectrum analyzer to view the spectrum of the digital output. Note that the measured ADC output is then corrupted by the spectrum analyzer noise figure and third-order distortion products. The measurement setup is shown in Fig. 10. The ADC is driven simultaneously with a pair of synthesizers, and the output measured on the analog spectrum analyzer. The spectrum analyzer noise-figure was improved by adding an input low-noise high-gain preamplifier with input precision switched attenuators. The attenuators are used for measurements with large ADC input signals, reducing the spectrum analyzer input amplitude in order to avoid intermodulation effects in the analyzer.

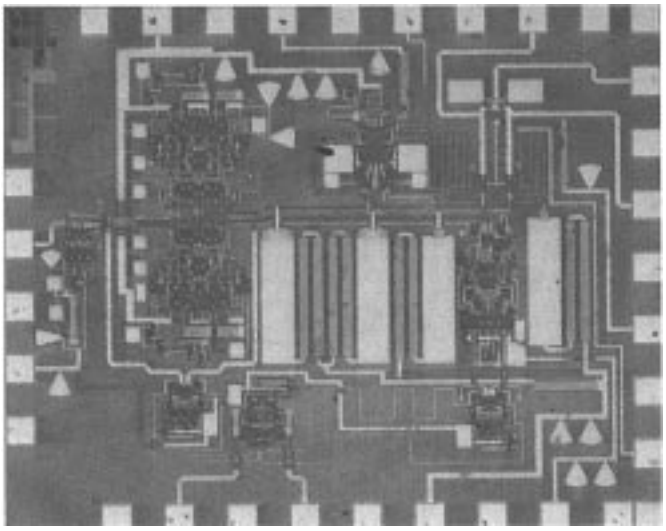

Fig. 9. Die photograph of the completed Σ–Δ modulator.

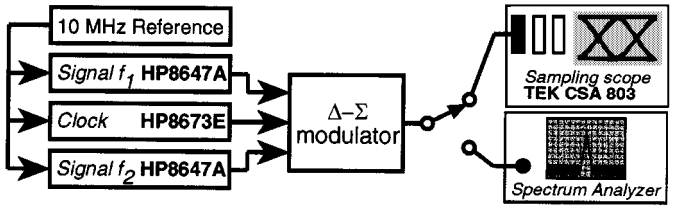

Fig. 10. The setup used for testing the Σ–Δ modulator.

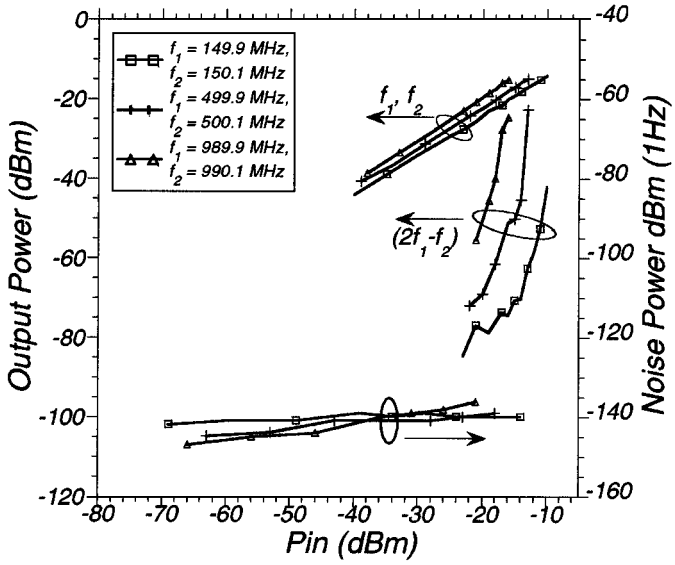

Fig. 11. Noise floor and third-order distortion power as a function of input power for different signal frequencies.

For small ADC inputs, the attenuators are removed, and the ADC output noise spectrum measured on the spectrum analyzer. For large ADC inputs, ADC intermodulation products are measured with the attenuators present, avoiding intermodulation distortion from the spectrum analyzer and its preamplifiers. The ADC low-signal noise floor and third-order intercept can thus both be measured.

Because the spectrum analyzer has dynamic range smaller than that of the ADC under test, it is difficult to measure the

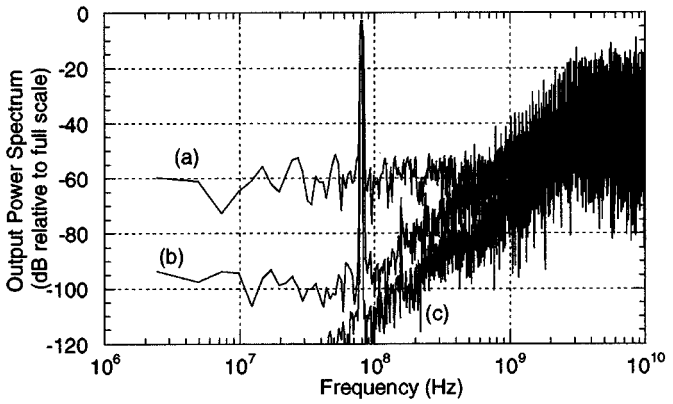

Fig. 12. Full-loop transistor level simulations on SPICE of (a) present ADC and (b) ADC with 3 stage latched comparator and a preamplifier, as compared to (c) MATLAB system level simulation.

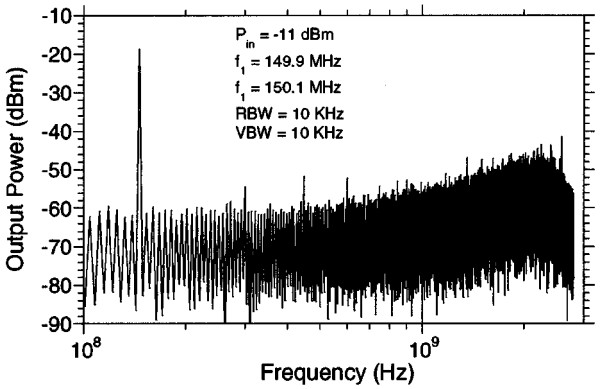

Fig. 13. Spectrum of the Σ–Δ modulator output for a two-tone input at 150 MHz.

ADC output noise given full-scale ADC input signals. Under strong ADC input drive, with the attenuators present, the ADC output noise falls below the kTF noise floor of the spectrum analyzer; with the attenuators absent, the spectrum analyzer input is driven into gain compression.

The Σ–Δ modulator was tested with an 18-GHz clock and two-tone measurements were performed at signal frequencies of 150 MHz, 500 MHz, and 990 MHz. The results for variation of the output power in the fundamental and the third-order distortion component are shown in Fig. 11. The observed increase in ADC noise with increased input signal power may be due to instrument effects, as discussed above or ADC nonidealities. The noise floor shows little variation from 150 MHz to 1 GHz. This suggests that the modulator does not shape the quantization-noise below 1 GHz. This is in contrast with our MATLAB simulations, which do not model comparator metastability. The measured ADC SNR is, however, consistent with full-loop transistor-level circuit simulations we have recently performed (Fig. 12). Because of these simulation results, we have recently redesigned the ADC. The modified ADC adds an additional stage of regeneration in the latched comparator and adds a two-stage Cherry–Hooper [15] limiting preamplifier at the comparator input. In SPICE simulations, this improved design exhibits much higher SNR at frequencies below 1 GHz. Hence, we believe that the poor measured noise

is due to quantizer metastability and dynamic hysteresis errors. Fig. 13 shows the spectrum of the output for a two-tone input at 150 MHz. The modulator achieved a two-tone SNR of 48 dB, 42 dB, and 33 dB for input signals at 150 MHz, 500 MHz, and 990 MHz, respectively.

V. Conclusion

We have demonstrated a second-order continuous-time Σ–Δ modulator fabricated in a 200-GHz f_τ, $f_{\max}$ InAlAs/InGaAs HBT process. The chip is clocked at 18 GHz with signal bandwidths ranging from 150 to 990 MHz. The modulator achieved a two-tone SNR of 48 dB, 42 dB, and 33 dB for input signals at 150 MHz, 500 MHz, and 990 MHz, respectively. Poor noise-shaping was observed below 1 GHz. Transistor level full-loop simulations of the ADC and a modified ADC, with additional comparator regeneration and preamplification, suggest that the poor noise shaping is due to quantizer metastability and dynamic hystersis errors. Our analysis further suggests that low hystersis can be obtained at 18-GHz clock rate in a 200 GHz f_τ process. Confirmation of the analysis must await testing of the revised ADC design. The modified ADC is now in fabrication.

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