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# High Speed InP-based Heterojunction Bipolar Transistors

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**Abstract.** Wideband HBTs are obtained by thinning the base and collector, increasing current density, decreasing emitter contact resistivity, and reducing the emitter and collector junction widths. In digital ICs, increased emitter current density and reduced emitter resistivity are critical requirements. We have fabricated submicron HBTs using substrate transfer processes, and have obtained devices with extremely high mm-wave gains. Amplifiers with 6.3 dB gain at 175 GHz have been fabricated, and 75 GHz true static frequency dividers demonstrated.

## 1. Introduction

Device scaling is central to high frequency semiconductor device design. Compared to silicon, III-V compound semiconductors offer higher electron mobilities and higher saturation drift velocities. Yet III-V devices must be aggressively scaled to deep submicron dimensions if they are to remain competitive with silicon. III-V heterojunction bipolar transistors (HBTs), in particular, have not been adequately scaled. GaAs- and InP- based HBTs are typically fabricated at 1–2 $\mu$m minimum feature sizes. This is in marked contrast to both III-V HEMTs, where 0.1 $\mu$m gate lengths are typical, and Si/SiGe HBTs, where emitter widths are 0.1 $\mu$m [1] and emitter current densities are as high at $10^6$ A/cm$^2$.

## 2. HBT scaling: requirements, approaches, remaining difficulties

For a $\gamma$:1 improvement in all HBT transit times and $RC$ delays, hence a $\gamma$:1 improvement in $f_\tau$, $f_{max}$, and a $\gamma$:1 speed improvement in an arbitrary circuit using the device, device parameters must scale as in table 1 [5].

Insofar as these scaling laws can be followed, HBT bandwidth can be arbitrarily increased. While breakdown voltage decreases as the collector is thinned, with InP

**Table 1.** Required proportional change in key HBT parameters in order to obtain a $\gamma$:1 increase in bandwidth in an arbitrary circuit. Additionally, for mesa HBTs, but not transferred-substrate or undercut-mesa devices, the base contact resistivity $\rho_v$ must also scale as $\gamma^{-2}$

| parameter | symbol | scaling law |
|---|---|---|
| collector depletion thickness | $T_c$ | $\gamma^{-1}$ |
| base thickness | $T_b$ | $\gamma^{-1/2}$ |
| emitter-base junction width | $W_e$ | $\gamma^{-2}$ |
| collector-base junction width | $W_c$ | $\gamma^{-2}$ |
| emitter depletion thickness | $T_{eb}$ | $\gamma^{-1/2}$ |
| emitter parasitic resistivity | $\rho_e$ | $\gamma^{-2}$ |
| emitter junction area | $A_e$ | $\gamma^{-2}$ |
| emitter current | $I_e$ | $\gamma^0$ |
| emitter current density | $J_e$ | $\gamma^2$ |
| bias and signal voltages | $V_{CE}$, $v_{ce}$ | $\gamma^0$ |
| device power density | – | $\gamma^2$ |

collectors, devices with even 300 GHz $f_\tau$ have breakdown far in excess of than required for logic ICs. Emitter contact resistivity must improve rapidly with increases in HBT bandwidth. Emitter current density must increase in proportion to the square of circuit bandwidth. While fast III-V HBT ICs operate at $\sim 10^5$ A/cm$^2$, Si/SiGe HBTs operate at $10^6$ A/cm$^2$. To attain such high current densities in III-V HBTs, heatsinking, emitter resistivity, and reliability must be addressed.

One limit to HBT scaling is the required rapid reduction in emitter and collector junction widths. In a mesa HBT, the collector-base junction lies under both the emitter junction and the base Ohmic contacts. Narrowing the collector junction requires narrowing the base Ohmic contacts; unless the base Ohmic contact resistivity is rapidly improved, this will increase the base resistance. Consequently, the base Ohmic contact resistivity must be improved rapidly (scaling as $\gamma^{-2}$) as the device is scaled. Narrow collector junction dimensions can be obtained simultaneously with wide base Ohmic contacts using either substrate transfer [5] or lateral-etch-undercut [6] processes. Collector junctions can also be aggressively scaled in mesa HBTs if the base contract resistivity is greatly reduced [7].

While the collector current density must increase as $\gamma^2$, III-V HBTs presently operate at relatively low emitter current densities, $\sim 10^5$ A/cm$^2$. Thermal design, passivation, and current-induced and thermally-driven failure mechanisms are key concerns. HBT scaling laws require that the emitter resistivity decrease as $\gamma^{-2}$. Yet, III-V HBTs have emitter resistivity (normalized to a unit emitter junction area) some 5:1 larger than is typical of Si/SiGe HBTs.

These factors are critical for high speed logic circuits. Presently, Si/SiGe and InP HBTs show comparable ECL clock frequencies, despite a ~2:1 ratio in $f_\tau$ and $f_{max}$ between the two technologies. Results of a hand analysis of the delay (ignoring interconnects) of an ECL master-slave latch are shown in table 2 [8]. Examining the delay components in terms of device ($r_{bb}$, $r_{ex}$) and load ($r_l = \Delta V_L/J$) resistances through

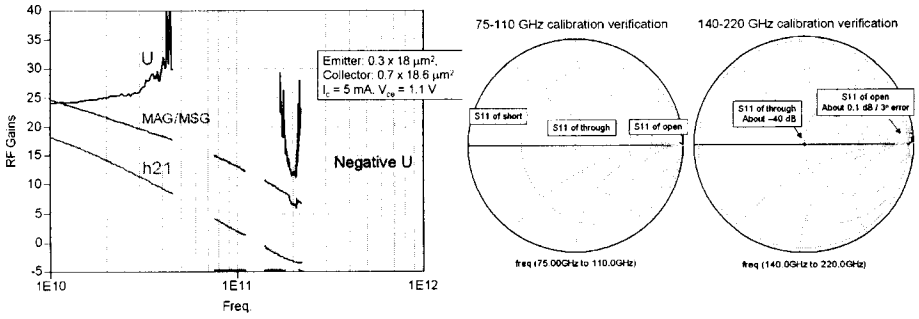
**Table 2.** (a) Approximate delay coefficients $a_{ij}$, for an ECL master-slave latch. Gate delay is of the form $T_{gate} = 1/2f_{clock} = \Sigma a_{ij} r_i c_j$. (b) *Approximate* delay components, derived by a set of circuit simulations, for the HBT of fig. 2, operating at $2 \cdot 10^5$ A/cm$^3$, with $\Delta V_L = 200$ mV

| .. | $c_{je}$ | $c_{cbx}$ | $c_{cbi}$ | $c_{\text{diff}} = \frac{\tau_f J}{\Delta V_L}$ |
|---|---|---|---|---|
| $\Delta V_L/J$ | 1 | 6 | 6 | 1 |
| $kT/qJ$ | 0.5 | 1 | 1 | 0.5 |
| $\rho_e$ | -0.25 | 0.5 | 0.5 | 0.5 |
| $r_{bb}$ | 0.5 | 0 | 1 | 0.5 |

(a)

| .. | $C_{je}$ | $C_{cbx}$ | $C_{cbi}$ | $C_{\text{diff}} = \frac{\tau_f I}{\Delta V_L}$ | total |
|---|---|---|---|---|---|
| $\Delta V_L/I$ | 33.5% | 6.7% | 27.8% | | 68.4% |
| $\Delta V_L/I$ | | | | 12.3% | 12.3% |
| $kT/qI$ | 1.4% | 0.1% | 0.4% | 0.5% | 2.5% |
| $R_{ex}$ | -1.3% | 0.1% | 0.3% | 0.9% | 0.1% |
| $R_{bb}$ | 10.2% | | 2.8% | 3.7% | 16.7% |
| total | 43.8% | 6.8% | 31.3% | 17.5% | 100% |

(b)




(a) (b)

**Figure 1.** (a) Measured gains in the 6-45, 75-110, and 140-220 GHz bands, of a submicron transferred-substrate HBT. In the indicated bands, Mason's gain $U$ is unbounded. (b) Calibration verification in the 75-110, and 140-220 GHz bands. In the 75-110 GHz band, the accuracy is such that the short, open, and through standards appear as barely-visible dots in the correct locations on the Smith chart.

which capacitances are charged, 80% of the delay is associated with $\Delta V_L/J$ . Thus, high current density $J$ and low logic voltage swing $\Delta V_L$ are critical for high-speed logic. *Because the logic swing $\Delta V_L$ must be at least $6(kT/q + J\rho_e)$ for adequate noise margin, low emitter resistivity $\rho_e$ is also essential.* Examining the delay components in terms of charging depletion ($c_{je}$, $c_{cb}$) and diffusion ($\tau_f J/\Delta V_L$) capacitances, 82% of the delay is associated with charging depletion capacitances and only 18% associated with the base+collector transit time $\tau_f$. In present InP HBTs, carrier transit times have been greatly reduced without a corresponding effort to reduce depletion-layer capacitance charging times through excess $C_{cb}$ reduction, increased current density, and reduced emitter resistivity. Consequently, $f_\tau$ shows negligible correlation with logic speed.

## 3. Transferred-substrate HBTs

Using substrate transfer processes, the extrinsic collector-base junction can be reduced in size or eliminated. This permits either aggressive lithographic scaling *without* epitaxial scaling for greatly increased $f_{max}$ at constant $f_\tau$. Alternatively, if high values of both $f_\tau$ and $f_{max}$ are sought, simultaneous lithographic and epitaxial scaling is required; with the extrinsic $C_{cb}$ eliminated, operation at high current density and reduction of the emitter resistance are the key requirements for further scaling.

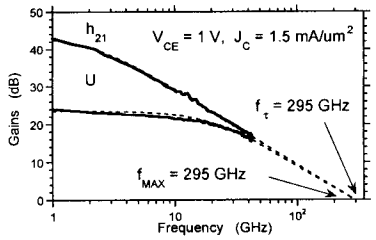



**Figure 2.** Measured RF gains for an HBT with a 300 Å base with 52 meV grading and a 2000 Å collector.

Figure 1,a [9] shows measured current and power gains of a submicron HBT. The device was characterized in the 6-45, 75-110, and 140-220 GHz bands. Above 45 GHz, the device unilateral power gain increases to infinity, and then becomes negative, a condition under which the addition of an appropriate small resistive attenuation results in infinite $U$. The unilateral gain is negative over a bandwidth of approximately 45–170 GHz, and results from a *very* small device negative output conductance $G_{22}$ of approximately -1 mS. The effect does not appear to be a measurement artifact; the calibration, particularly in the 75-110 GHz band is quite precise (fig. 1,b). Figure 2 shows RF gains for an HBT with 0.6 $\mu$m × 8 $\mu$m emitter and 2$\mu$m × 12 $\mu$m collector junctions, a 300 Å thick base with 52 meV bandgap grading, and a 2000 Å thick collector [3]. The devices above are single-heterojunction transistors with low breakdown voltage. Figure 3 shows DC and RF data for a transferred-substrate DHBT [10].

Figure 4 shows a single-HBT tuned amplifier with 6.2 dB gain at 175 GHz. This the highest operating frequency reported for an HBT amplifier. Master-slave latches, configured as 2:1 static frequency dividers, were fabricated using HBTs with 0.6 $\mu$m emitter and 1.4 $\mu$m collector junctions widths (fig. 5). In testing, the IC functions correctly over 5-75 GHz range [4].

## 4. Conclusions

Wideband HBTs are produce by a simultaneous reduction in lithographic and epitaxial dimensions. Major impediments to such scaling are the required reductions to the resisivities of the emitter and base Ohmic contacts, and the required increases in current densities. Scaling difficulties related to the base Ohmic contact can be addressed through either increased base doping or decoupling of base and collector junction dimensions

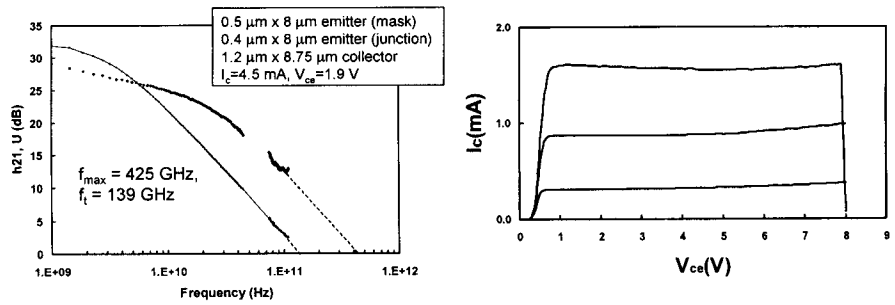



**Figure 3.** Measured power gains and DC characteristics for an InP/InGaAs/InP transferred-substrate HBT. BVCEO is 8 V at $5\times10^4$ A/cm$^2$.

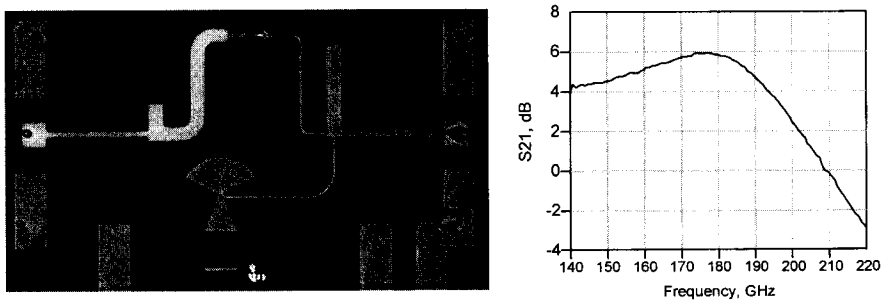



**Figure 4.** 175 GHz single-HBT tuned amplifier.

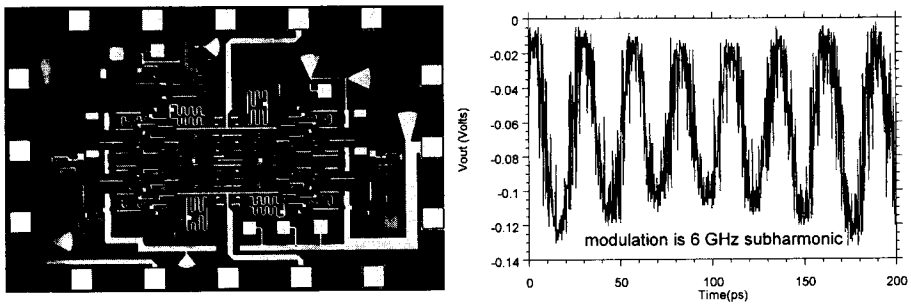



**Figure 5.** 75 GHz master-slave latch. The IC contains 70 HBTs.

through advanced processes. Emitter resistivity and reliable high-current-density operation are more fundamental difficulties. In InP HBTs used in digital and mixed-signal ICs, reduced emitter resistivity and increased current density are critical to increased circuit bandwidth. High yields have not yet been proven for IC processes using submicron InP HBTs. As emitter dimensions are reduced to below 0.5 $\mu$m, present emitter-base fabrication processes will have unacceptably low yield. We see the requirement for innovations in LSI-compatible fabrication processes for submicron InP HBTs.

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