75 GHz ECL static frequency divider using InAlAs/InGaAs HBTs

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A 75 GHz static frequency divider in InAlAs/InGaAs transferred-substrate heterojunction bipolar transistor (HBT) technology is reported. This is the highest reported frequency of operation for a static frequency divider. The circuit has 60 transistors and dissipates 800 mW. The divider was operated at a clock frequency of 5.0 to 75 GHz.

Introduction: Heterojunction bipolar transistors are finding increased applications in radio frequency (RF)/microwave circuits, high-speed analogue-to-digital converters, and fibre-optic ICs. Two important figures of merit in any high-speed technology are the transistor cutoff frequencies (f_t and f_{max}) and logic speed. The device cutoff frequencies have a direct bearing on the analogue circuit performance. The maximum clock frequency of a static frequency divider provides a measure of the logic speed. Static frequency dividers clocking in excess of 60 GHz have been realised in SiGe [1] and InAlAs/InGaAs [2, 3] HBT technology. Transferred substrate HBT technology has exhibited excellent microwave and digital performance [3, 4]. Here we report static frequency dividers operating up to a record 75 GHz clock input.

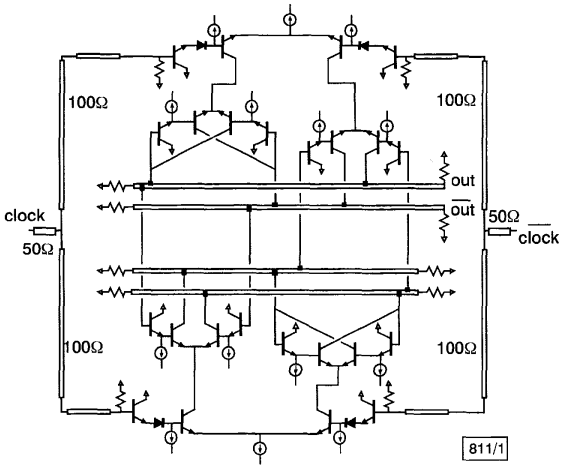

Fig. 1 *Circuit diagram of static frequency divider*

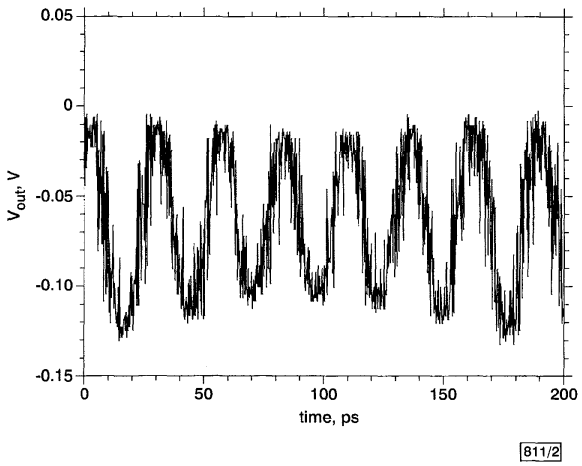

Fig. 2 *Output waveform of divider circuit for 75 GHz clock input*

Technology: The dividers were fabricated using the transferred substrate HBT process [4]. The key feature of this process is the reduced base-collector capacitance (C_{bc}). The presence of a continuous ground plane provides a microstrip wiring environment. The epitaxial layer structure is similar to [3]. The base is 400 Å thick InGaAs, with 52 meV bandgap grading and doped at 4.0×10^{19} cm^{-3}. The collector is 2 kÅ thick and doped at 1.0×10^{16} cm^{-3}. RF measurements on a 6.0×1.0 μm^2 emitter and 7.0×2.0 μm^2 collector device, biased at a $V_{ce} = 1.0$ V and $J_e = 1.0$ mA/μm^2, had an f_t and f_{max} of 165 GHz and 220 GHz, respectively.

Circuit design: The circuit (Fig. 1) is similar to the 66 GHz static divider reported by Lee *et al.* [3]. Modifications to the earlier circuit [3] include reduction in device and IC layout parasitics, and layout modifications to enable access to clock input using microwave wafer probes having waveguide rather than co-axial input connectors. The HBTs used in the divider have a 12.0×0.7 μm^2 emitter geometry (mask dimensions) and a 13.0×1.5 μm^2 collector geometry, and are operated at a peak current density of 1.8 mA/μm^2.

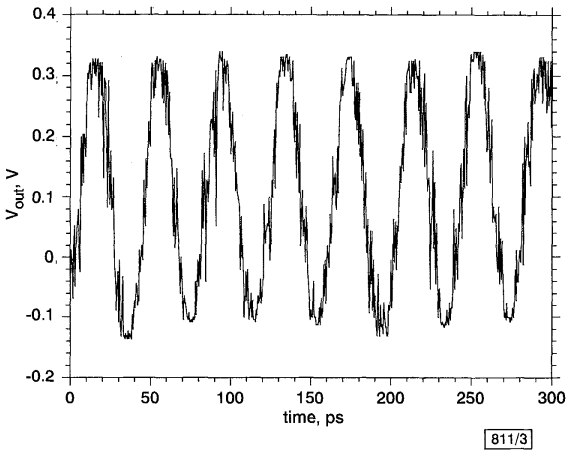

Fig. 3 *Frequency synthesiser output at 25 GHz*
Note 6 GHz sub-harmonic modulation

Measurements and results: Divider measurements were performed at clock frequencies ranging from 5 to 75 GHz. At low frequencies a 2–26 GHz frequency synthesiser output was directly used to drive the clock input. The dividers were tested over the 26–40 GHz frequency range by using the 2–26 GHz frequency synthesiser to drive a 2:1 frequency doubler, producing a 26–40 GHz output. For 50–75 GHz measurements, the 2–26 GHz synthesiser directly drives a 3:1 frequency tripler with output delivered on-wafer with a V-band waveguide-coupled micro-coaxial probe. Here the available signal power is +2.0 to +6.0 dBm over the band. The output waveform for a 75 GHz clock input is shown in Fig. 2. The static divide-by-two output at 37.5 GHz shows a 6.0 GHz sub-harmonic (Fig. 3) present in the 2.0–26.0 GHz frequency synthesiser output. The IC was also tested in W-band (75–110 GHz) by cascading the 2–26 GHz synthesiser with a frequency doubler and a frequency tripler. Here the available output power (–1.0 to +2.0 dBm, including probe losses) was insufficient for IC operation. The IC operates at all tested frequencies between 5.0 and 75.0 GHz.

Acknowledgments: This work was supported by the Office of Naval Research (ONR) under ONR N00014-01-1-0024.

29 March 2001
Electronics Letters Online No: 20010465
DOI: 10.1049/el:20010465

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Improved voltage tripler structure with symmetrical stacking charge pump

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An improved voltage tripler with a symmetrical stacking charge pump is proposed. In this original voltage tripler, parasitic capacitances are pre-charged to reduce their influence, thus reducing the output voltage loss due to parasitic capacitances by a factor of 2.

Introduction: It is well known that charge pump circuits can be used to generate voltages higher than the circuit supply voltage. Charge pump circuits can be classified into two categories according to their structures: asymmetrical and symmetrical. The advantage of the symmetrical structure is that a low-capacitance output capacitor can be used to generate an output voltage with reasonable undulation for a resistive load. By using a low-capacitance output capacitor, the rise time of the output voltage can be made shorter (several clock cycles) [1, 2]. We have realised a voltage tripler with a symmetrical stacking charge pump, which is shown in Fig. 1. As its structure is symmetrical, we need only study the operation of one half of the device. The other part works in the same way but in opposite clock phase. Its operation consists of two phases, as shown in Fig. 2. As a result, in the ideal case, we obtain $3Vdd$ at the output V_2. As V_2 varies between Vdd and $3Vdd$, the output stage is used to generate a DC voltage output $3Vdd$ [1].

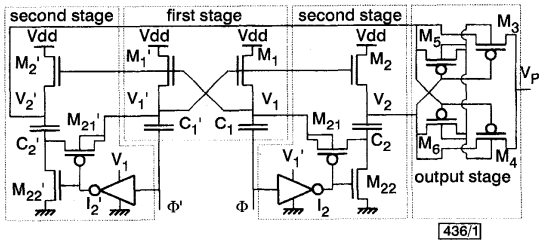

Fig. 1 *Voltage tripler with symmetrical charge pump structure*

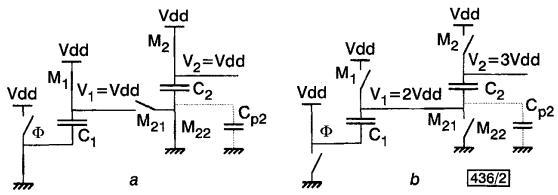

Fig. 2 *Equivalent circuit of one half of charge pump*

a Charging phase
b Stacking phase

However, in practice, parasitic capacitances exist. The dominant capacitances Cp are between the bottom plates (poly1) of the pump capacitors and the substrate. Here Cp_1 represents the parasitic capacitance of C_1 and Cp_2 that of C_2. As Cp_1 is charged directly by the clock signal, its influence is only perceptible in terms of the efficiency. However, Cp_2 influences the maximum output voltage. In fact, during the charging phase when the clock signal Φ is low, C_1 is charged to Vdd and parasitic capacitance Cp_2 is discharged by MOST switch M_{22}. During the stacking phase when Φ is high, parasitic capacitance Cp_2 is in parallel with C_1, which is boosted to $2Vdd$ by the clock signal. There is a redistribution of charges between the two capacitors; some of the charge stored in C_1 during the charging phase will be transferred to Cp_2 during the stacking phase to reach equilibrium potential. Consequently, voltage V_1, which can be obtained from theory, is

$$V_1 = 2Vdd - V_d \tag{1}$$

where V_d is the voltage drop due to parasitic capacitance, which can be calculated by

$$V_d = \frac{2Vdd}{1 + \frac{C_1}{Cp_2}} \tag{2}$$

As V_2 depends on V_1, consequently V_2 can be expressed by

$$V_2 = 3Vdd - V_d \tag{3}$$

As a result, output voltage loss is inevitable.

In this Letter, a new voltage tripler structure based on a symmetrical stacking charge pump is proposed. With this new structure, the influence of parasitic capacitances can be reduced.

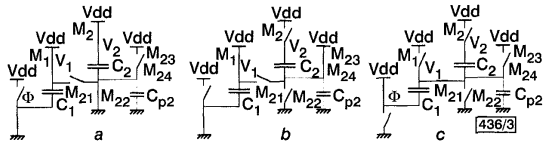

Fig. 3 *Equivalent circuit of one half of optimised charge pump*

a Charging phase
b Pre-charging phase
c Stacking phase

Improved symmetrical charge pump: The output voltage loss is due to charging parasitic capacitances that are completely discharged during the charging phase. To reduce the influence of parasitic capacitance, the parasitic capacitances are pre-charged to Vdd before the stacking phase. As a result, during the stacking phase, the parasitic capacitances will be charged by C_1 from Vdd to $2Vdd$ instead of from 0 to $2Vdd$. In theory, charges transferred and lost to Cp_2 will be reduced by a factor of 2 compared to when the former tripler is used. Thus the output voltage loss, which is expressed by

$$V_d = \frac{Vdd}{1 + \frac{C_1}{Cp_2}} \tag{4}$$

is also reduced by the same amount.

The principle equivalent circuit of one half of the improved symmetrical charge pump is shown in Fig. 3. From the equivalent circuit, we can see that a pre-charging circuit is added to the former circuit. The pre-charging circuit consists of a switch, the realisation of which is discussed in detail in the following Section, and linked to Vdd. The improved charge pump's operation consists of three phases: charging the pump capacitors, pre-charging the parasitic capacitances and stacking the pre-charged pump capacitors.

As with the former charge pump circuit, during the charging phase, by closing M_1, M_2 and M_{22}, only pump capacitors are charged to Vdd. However, unlike in the case of the former structure, a pre-charging phase is carried out before the stacking phase. By closing $M_{23}M_{24}$, parasitic capacitance Cp_2 is charged to Vdd; by opening M_2, M_{21} and M_{22}, charges stored in C_2 remain intact. Finally, when Φ increases, by closing only M_{21}, C_1 and C_2 are stacked. As Cp_2 is already charged to Vdd, fewer charges from C_1 will be transferred and lost to Cp_2 to charge Cp_2 to the same potential as C_1.

Realisation: The improved voltage tripler is shown in Fig. 4, which shows the first stage, the second stage as well as the output stage of the former structure. Note that a pre-charging stage has been added, which consists of MOST switches M_{23} and M_{24} and which is linked to Vdd.