

Thermal Performance of Metamorphic Double Heterojunction Bipolar Transistors with InP and InAlP Buffer Layers

Y. M. Kim, M. Dahlström, M. J. W. Rodwell, A. C. Gossard

Department of Electrical and Computer Engineering, University of California,
Santa Barbara, CA 93106, USA. kymdow@ece.ucsb.edu, 805-893-3543

InP-based double heterojunction bipolar transistors (DHBT) are a key technology for high-speed optical fiber transmission. InP substrates are expensive and are not available in as large sizes as GaAs substrates. Moreover, InP substrates are fragile and are easily broken in fabrication. This motivates development of metamorphic InP DHBT (MDHBT) on GaAs. Thermal performance is of critical importance, as high speed DHBTs must operate at emitter power densities exceeding 250 kW/cm^2 . In the case of MDHBTs, thermal resistance [1] is dominated by the poor thermal conductivity of the thick ($1\text{-}1.5 \mu\text{m}$) metamorphic buffer layer lying immediately below the collector. We have found that AlGaAsSb and InAlAs metamorphic buffer layers have very low thermal conductivity, and have earlier reported MDHBTs with higher thermal conductivity InP buffer layers [2]. Here we compare thermal characteristics of MDHBTs grown on InP and InAlP buffer layers to those of lattice-matched devices. In the case of InP buffer layers and narrow emitter geometries, MDHBT thermal resistance is comparable to that of lattice-matched HBTs. A low $32 \text{ }^\circ\text{C}$ junction-ambient temperature rise is obtained in a device operating at 235 kW/cm^2 .

Most alloy semiconductors have lower thermal conductivities ($\sim 5 \text{ W/k-m}$ for InGaAs and $\sim 10 \text{ W/k-m}$ for InAlAs) than the stoichiometric semiconductors (44 W/k-m for GaAs and 68 W/k-m for InP). Thermal conductivity of metamorphic buffer layers is further reduced by the very high defect density. It is therefore advantageous to select a stoichiometric semiconductor for the metamorphic buffer layer [3]. We compare a lattice matched InP/InGaAs/InP DHBT to MDHBTs on GaAs substrates with similar layer structures but having InP and InAlP metamorphic buffer layers. The InAlP buffer has a compositional grading starting from the lattice constant of GaAs ($\text{In}_{0.49}\text{Al}_{0.51}\text{P}$) to that of InP. HBTs studied had an $8 \mu\text{m}$ emitter stripe length, a $8.5 \mu\text{m}$ base mesa length, emitter contact widths of $0.6, 0.7, 1.0$ and $2.0 \mu\text{m}$, while base contact widths are $0.25, 0.5,$ and $1.0 \mu\text{m}$ on either side of the emitter stripe. The emitter junction width is $\sim 0.3 \mu\text{m}$ smaller than the emitter contact width. Given this large data set, thermal parameters are studied as a function of base mesa area, as thermal resistance is more strongly correlated to base mesa area than to emitter junction area.

Figure 1 shows the measured temperature rise of operating device at power of 7.5 mW , plotted as a function of base mesa area. As base mesa area is increased, the junction temperature is reduced. Metamorphic HBTs with InP buffer layers show junction temperatures only slightly larger than lattice-matched devices, with the reduced thermal conductivity of the metamorphic InP buffer layer almost offset by the use of a thinner (250 \AA vs. 500 \AA) N+ InGaAs Ohmic contact layer within the N+ subcollector. Much higher junction temperatures are observed with InAlP buffer layers. The three-dimensional Laplace heat flow equation was solved assuming the composite subcollector design (250 \AA InGaAs, 1250 \AA InP), the $1.5 \mu\text{m}$ InP or InAlP metamorphic buffer layer, and the GaAs substrate. The thermal conductivity of the buffer layer was treated as a variable parameter. Comparing the results of these calculations (Figure 2) to the observed junction temperature, the thermal conductivities of the InP and InAlP buffer layers are $\sim 35 \text{ W/k-m}$ and $\sim 8 \text{ W/k-m}$.

These data, together with earlier thermal studies of InAlAs and AlGaAsSb buffer layers, strongly suggests the use of InP buffer layers in metamorphic HBTs.

[1] W. Liu, et al, IEEE Trans. Electron Devices, vol.43, (no.3), IEEE, March 1996. p.388-95

[2] Y.M. Kim, et al, "High-Performance InP/In_{0.53}Ga_{0.47}As/InP Double Heterojunction Bipolar Transistors on GaAs Substrates", IEEE EDL, 2002, to be published. Also, IEEE IPRM Conference, May 2002.

[3] Y. M. Kim et al, "InP/In_{0.53}Ga_{0.47}As/InP Double Heterojunction Bipolar Transistors on GaAs Substrates Using InP Metamorphic Buffer Layer", Solid State Electronics, 2002, to be published

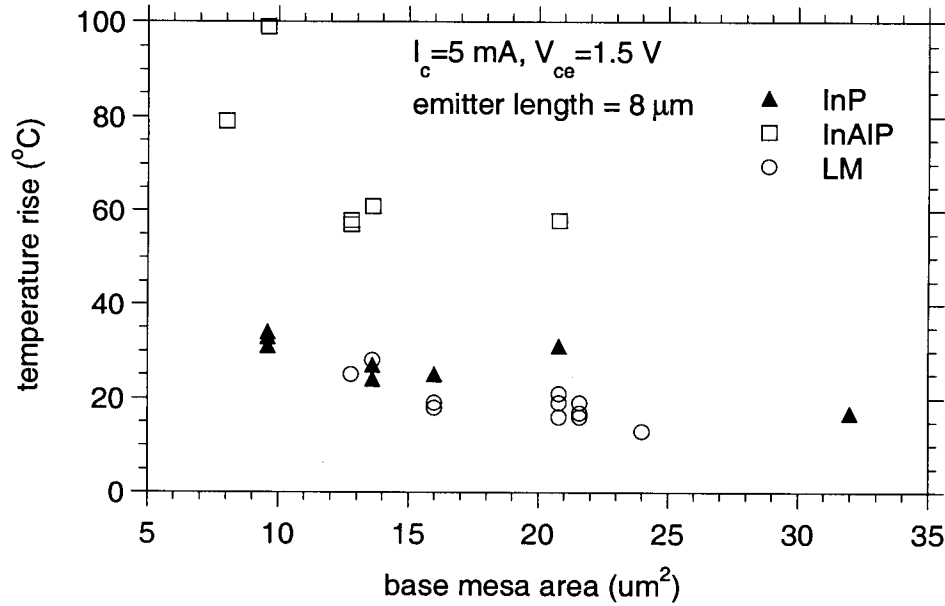


Figure 1. Temperature rise of HBTs biased at 7.5mW dissipation as a function of base mesa area.

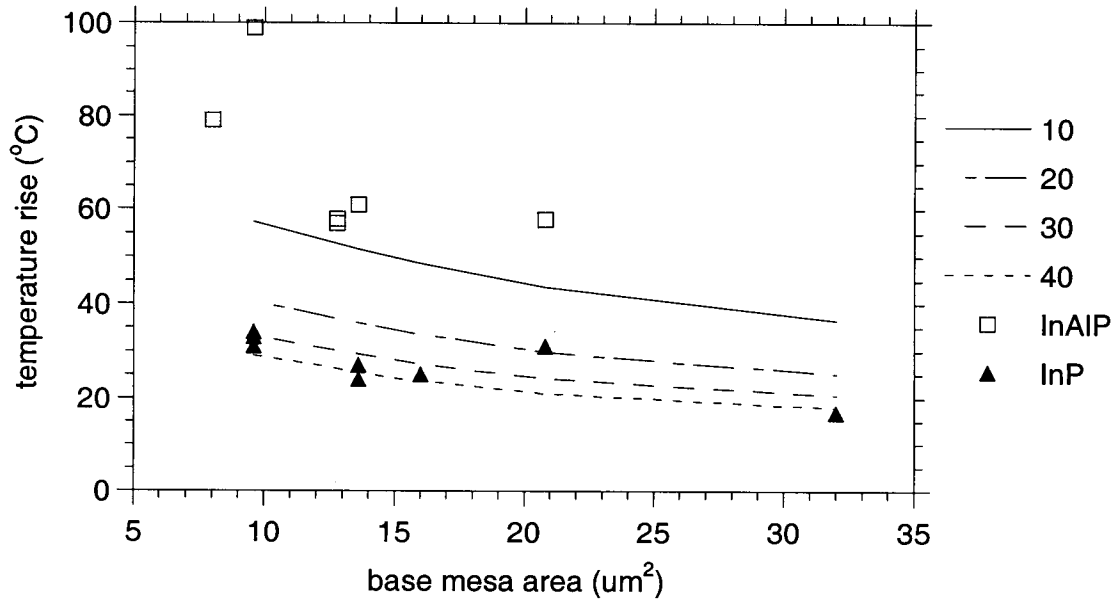


Figure 2. Comparison of measured junction temperatures data with calculation, as a function of metamorphic buffer layer thermal conductivity. The four lines represent calculated temperature rise assuming the thermal conductivities of 10, 20, 30, and 40 W/k-m.