Transistors for Fast Logic Circuits: What We Have Learned from InP-Based HBTs

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III-V's are much better than Silicon (?)

InP: big transport advantages over Silicon
$5x10^7$ vs. $1x10^7$ cm/sec collector electron velocity (measured)
300 Ω/square vs. ~10 kΩ/square base sheet resistance
3x larger breakdown at similar f_τ
shouldn't this lead to ~5 x faster logic ICs ???

This advantage is not being properly exploited

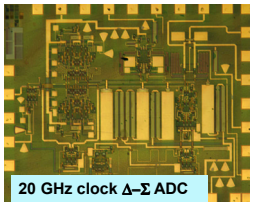
Silicon bipolars:
more aggressively ***SCALED*** (0.18 vs. 1 μm)
more extrinsic ***PARASITIC REDUCTION*** (double poly process)
better designed for ***LOGIC SPEED*** (vs. figures-of-merit)

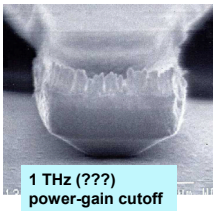
Should inform our efforts to build fast transistors in 6.1 Å system

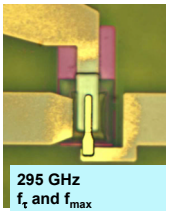
InAlAs/InGaAs/InP materials
advanced processes, scaling
→ extreme parasitic reduction

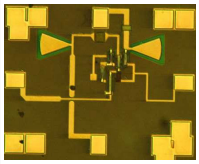
UCSB InP-HBT effort

UCSB
ONR

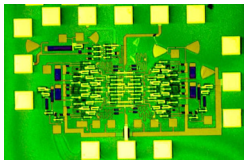

20 GHz clock Δ–Σ ADC


1 THz (???)
power-gain cutoff

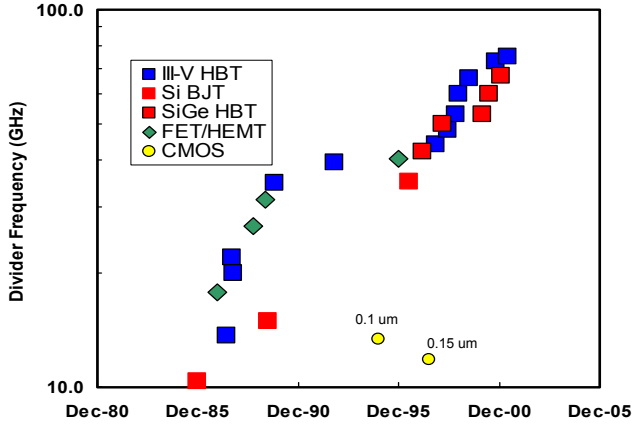

295 GHz
f_τ and f_{max}


DC- 80 GHz Amplifier


6.3 dB, 175 GHz 1-HBT amplifier


75 GHz master-slave latch

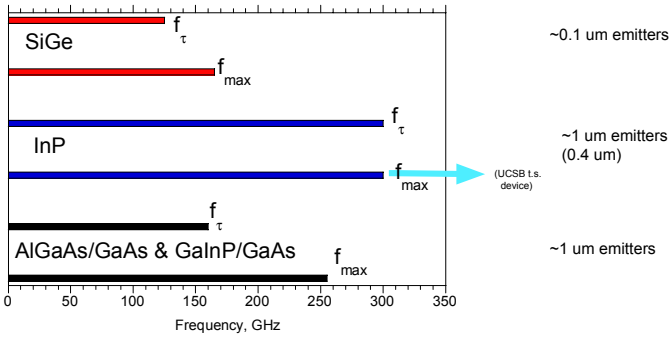
Logic Speed: III-V vs. Silicon



Benchmark: master-slave flip-flop configured as 2:1 **static** frequency divider

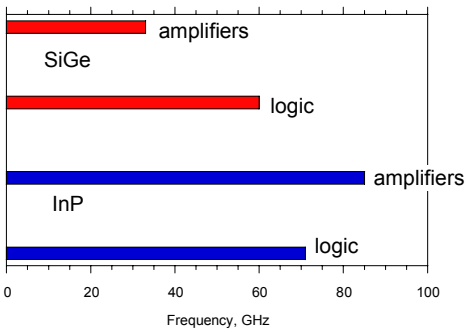
Source: M Sokolich, HRL, Rodwell, UCSB

State-of-art in HBTs, 2000: cutoff frequencies



InP HBTs today 2x faster,
& more scalable: Johnson limit, 2x faster at 5x larger dimensions

State-of-Art in HBTs, 2000: small-scale circuits



Si / SiGe has rough parity in logic with InP despite lower f_τ, f_{max}
due to higher current density, better emitter contacts

Si/SiGe has significantly slower amplifiers

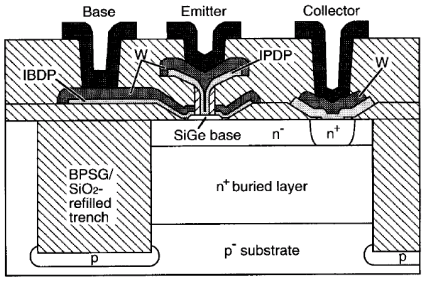
Very strong features of Si-bipolars

Emitter Width:
0.1 um

Emitter Current Density
10 mA/um^2

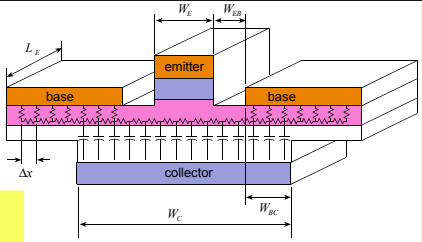
Polysilicon Emitter Contact
metal-semiconductor contact
area >> emitter junction area
→ low Rex

Polysilicon base contact
low sheet resistance in extrinsic base
small extrinsic collector-base junction area



HBT scaling: transit times

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ 's



reduce T_b by √2:1
*→ τ_b **improved** 2:1*

reduce T_c by 2:1
*→ τ_c **improved** 2:1*

*note that Ccb has been **doubled***
..we had wanted it 2:1 smaller

$$\tau_b \cong T_b^2 / 2D_n$$
$$\tau_b \cong T_c / 2v_{sat}$$

$\text{Assume } W_C \sim W_E$

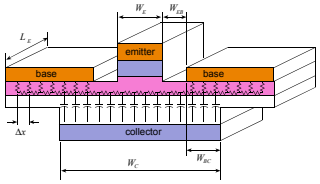
HBT scaling: lithographic dimensions

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ 's

Base Resistance R_{bb} must remain constant
→ L_e must remain ~ constant

$$R_{bb} = R_{gap} + R_{spread} + R_{contact}$$
$$\cong R_{contact}$$
$$= \sqrt{\rho_{sheet}\rho_{c,vertical}} \Big/ 2L_E$$

*Ccb/Area has been **doubled***
..we had wanted it 2:1 smaller
…must make area=L_eW_e 4:1 smaller
→ must make W_e & W_c 4:1 smaller



reduce collector width 4:1
reduce emitter width 4:1
keep emitter length constant

$\text{Assume } W_C \sim W_E$

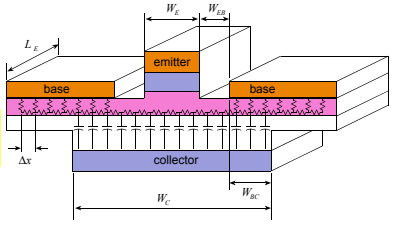
HBT scaling: emitter resistivity, current density

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ 's

Emitter Resistance R_{ex} must remain constant
but emitter area=L_eW_e is 4:1 smaller
resistance per unit area must be 4:1 smaller

$\text{Assume } W_C \sim W_E$

Collector current must remain constant
but emitter area=L_eW_e is 4:1 smaller
and collector area=L_cW_c is 4:1 smaller
current density must be 4:1 larger



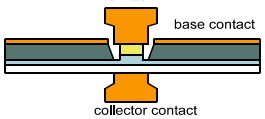
increase current density 4:1
reduce emitter resistivity 4:1

Scaling Laws for fast HBTs

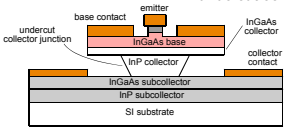
for x 2 improvement of *all* parasitics:
f_t, f_{max}, logic speed…
base √2: 1 thinner
collector 2:1 thinner
emitter, collector junctions 4:1 narrower
current density 4:1 higher
emitter Ohmic 4:1 less resistive

Challenges with Scaling:
Collector
mesa HBT: collector under base Ohmics.
Base Ohmics must be one transfer length
sets minimum size for collector
Emitter Ohmic:
hard to improve…how ?
Current Density:
dissipation, reliability
Loss of breakdown
avalanche Vbr never less than collector Egap
(1.12 V for Si, 1.4 V for InP)
….sufficient for logic, insufficient for power

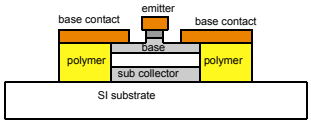
transferred-substrate



undercut-collector

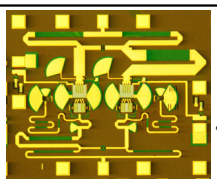


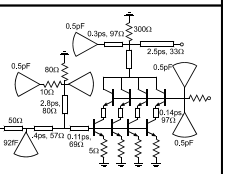
Narrow-mesa with 1E20 carbon-doped base



What HBT parameters determine circuit speed ?

Tuned ICs: MIMICs & RF
f_{max} sets gain
& max frequency, not f_t.

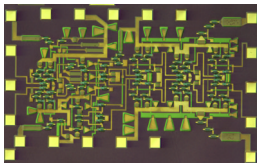


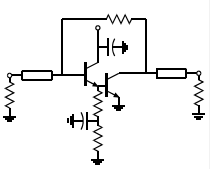


low ft/fmax ratio makes tuning hard (high Q)

Lumped analog circuits

need high & comparable
f_t and f_{max}.





What about digital ?

What do we need for fast logic ?

Gate Delay Determined by :

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C}\right)\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Depletion capacitance charging through the base resistance

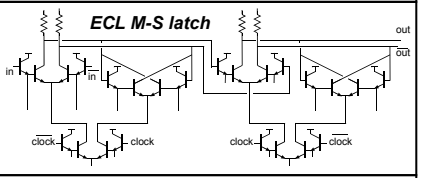
$$R_{bb}\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Supplying base + collector stored charge through the base resistance

$$R_{bb}\left(\tau_b+\tau_c\right)\left(\frac{I_C}{\Delta V_{LOGIC}}\right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 6\left(\frac{kT}{q}+R_{ex}I_c\right)$$



Neither f_τ nor f_{max} predicts digital speed

$C_{cb}\Delta V_{logic}/I_c$ is very important
→ ***collector capacitance reduction is critical***
→ ***increased III-V current density is critical***

R_{ex} must be very low for low ΔV_{logic} at high J_c

InP: R_{bb} , $(\tau_b+\tau_c)$, are already low, must remain so

What HBT parameters determine logic speed ?

	Cje	Ccbx	Ccbi	$(\tau_b+\tau_c)\ (I/\Delta V)$	total
$\Delta V/I$	33.5%	6.7%	27.8%		68.4%
$\Delta V/I$				12.3%	12.3%
(kT/q) I	1.4%	0.1%	0.4%	0.5%	2.5%
Rex	-1.3%	0.1%	0.3%	0.9%	0.1%
Rbb	10.2%		2.8%	3.7%	16.7%
total	43.8%	6.8%	31.3%	17.5%	100.0%
		38%			

Sorting Delays by capacitances :

44% charging C_{je}, 38% charging C_{cb}, only 18% charging C_{diff} (e.g. $\tau_b+\tau_c$)

Sorting Delays by resistances and transit times :

68% from $\Delta V_{\text{logic}}/I_c$, 12% from $(\tau_b+\tau_c)$, 17% from R_{bb}

R_{ex} has very strong indirect effect, as $\Delta V_{\text{logic}} > 6\bullet\left(kT/q + I_C R_{ex}\right)$

Caveats:
assumes a specific UCSB InP HBT (0.7 um emitter, 1.2 um collector 3kÅ thick, 400 Å base, 1.5E5 A/cm^2)
ignores interconnect capacitance and delay, which is very significant

Why isn't base+collector transit time so important ?

Under Small-Signal Operation :

$$\delta Q_{\text{base}} = (\tau_b+\tau_c)\delta I_C = (\tau_b+\tau_c)\frac{dI_C}{dV_{be}}\delta V_{be} = \frac{(\tau_b+\tau_c)I_C}{kT/q}\delta V_{be}$$

Under Large-Signal Operation :

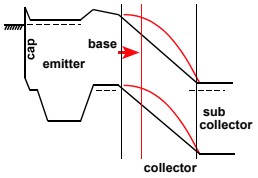
$$\Delta Q_{\text{base}} = (\tau_b+\tau_c)I_C = \frac{(\tau_b+\tau_c)I_{dc}}{\Delta V_{LOGIC}}\Delta V_{LOGIC}$$

Large-signal diffusion capacitance reduced by ratio of

$$\left(\frac{\Delta V_{LOGIC}}{kT/q}\right),\ \text{which is} \sim 10:1$$

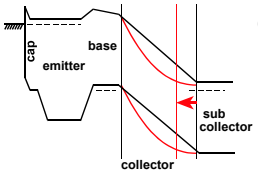
Depletion capacitances see no such reduction

Scaling Laws, Collector Current Density, C_{cb} charging time



Base Push-Out (Kirk Effect)

$$V_{cb}+\phi > +(J/v_{sat} - qN_d)(x_d^2/2\varepsilon)$$



Collector Depletion Layer Collapse

$$V_{cb}+\phi > +(qN_d - J/v_{sat})(x_d^2/2\varepsilon)$$

$$\Rightarrow\ J_{\max} - J_{\min} = 4\varepsilon v_{sat}(V_{cb}+\phi)/x_d^2$$

$$C_{cb}\Delta V_{LOGIC}/I_C = (\varepsilon A_{\text{collector}}/T_c)(\Delta V_{LOGIC}/I_C) = \frac{1}{2}\frac{\Delta V_{LOGIC}}{(V_{CB}+\phi)}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2v_{sat}}\right)$$

Collector capacitance charging time is reduced by ***thinning the collector*** *while increasing current*

High speed logic transistors are miniature power transistors

Devices must operate at very high current densities

… and must therefore withstand high junction temperatures
…and good thermal conductivity is paramount

… high current densities require high collector fields
… and device must be resistant to breakdown

What determines logic-gate power ?

Supply Voltage :

$-V_{ee}$ must be $\sim 2\text{-}3\cdot V_{be}$

Gate Delay :

$T_{gate} = R_L C_{wire} + \text{transistor terms} > R_L C_{wire}$

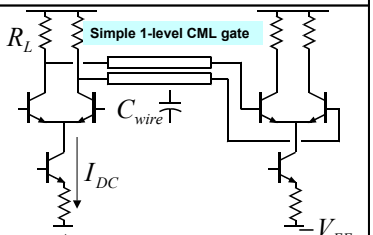
Power :

$P_{gate} = I_{DC}V_{EE} = (\Delta V_{LOGIC}/R_L)\cdot V_{EE}$

Power-Delay Product :

$$P_{gate}T_{gate} = (\Delta V_{LOGIC}/R_L)\cdot V_{EE}\cdot T_{gate} > (\Delta V_{LOGIC}/R_L)\cdot V_{EE}\cdot R_L C_{wire}$$

$$P_{gate}T_{gate} > \Delta V_{LOGIC}\cdot V_{EE}\cdot C_{wire}$$



2:1 reduction in base bandgap
→ 2:1 reduction in power (?)

but, there are difficulties…

If low Vbe = low power, why is SiGe lower-power than InP ?

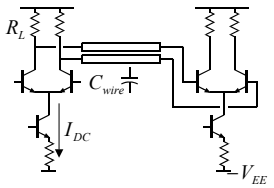
InP: V_{be}=0.7 V
beats SiGe power for highest speeds only
(fastest SiGe uses E²CL, increased V_{ce})

Si/SiGe: V_{be}=0.9 V
lower power at moderate & lower speeds

Why ?

Need small emitter area (0.1-- 0.5 um²).
low power = low current
fast HBT = high current density
→ big HBT = high power or low speed

Need small wiring capacitance
short wires = low capacitance = low power
small device footprint = short wires
many wiring planes = short wires



$$P_{gate}T_{gate} > \Delta V_{LOGIC} \cdot V_{EE} \cdot C_{wire}$$

-or-

3 mA HBT : 300 mV on 100 Ω line.

Specific concerns with some 6.1 Å materials:

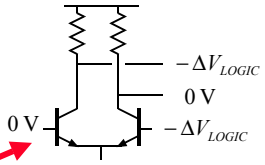
High power density → thermally-aggravated leakage

Low base bandgap + low bias voltage = large Ccb charging time

$$\frac{C_{cb}\Delta V_{LOGIC}}{I_C} \approx \frac{\Delta V_{LOGIC}}{V_{CE}}\left(\frac{A_{\text{coll}}}{A_{\text{emm}}}\right)\left(\frac{T_C}{4v_{sat}}\right)$$

$$V_{CE} = V_{BE} - \Delta V_{LOGIC}$$
$$= 360\text{ mV} - 250\text{ mV}$$
$$= 110\text{ mV}$$

!!!



Low collector bandgap + high bias voltage = breakdown

DARPA ABCS

Circuit design: HBT fast logic families

RSC UCSB

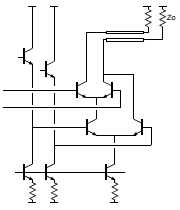
CML Gate:
Fast
emitter followers on lower level only
(level-shifting)
$V_{cc} = 3V_{be}$+300 mV
$I=3I_{switched}=3*\Delta V_{logic}/Z_o$ (approx.)

ECL Gate:
Adds emitter followers on upper level
Somewhat faster
$V_{cc} = 4V_{be}$+300 mV
$I=5I_{switched}=5*\Delta V_{logic}/Z_o$ (approx.)

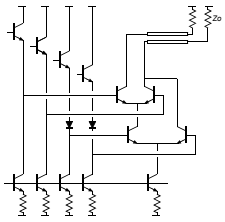
E²CL Gate:
Double emitter followers driving both levels
helps with f/f_τ, higher V_{ce} for high J/C
$V_{cc} = 5V_{be}$+300 mV
$I=7I_{switched}=7*\Delta V_{logic}/Z_o$ (approx.)

Best to use CML for low power
InAs-HBTs may need to be ECL

CML



ECL



Opportunities for the 6.1 Å System

HBTs: very very low contact resistivities
GaSb perfect for P-type
InAs perfect for N-type
emitter resistivity is a major scaling problem
low base contact resistivity → less lateral scaling needed
low voltage operation (if low ΔV_{logic} , high v_{sat})

HEMTs:
high n_s, high μ : very low contact and access resistance
very high velocity
high f_τ, low noise (if leakage fixed).
perhaps low voltage logic