Ultra High f_{max} InP/InGaAs/InP Transferred Substrate DHBTs

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Very wide bandwidth Double Heterojunction Bipolar Transistors (DHBT) will enable high-power amplifiers at 94 and 180 GHz, microwave ADCs , microwave direct digital frequency synthesis, fiber optic transmission at >40 Gb/s and wireless data networks at frequencies above 100 GHz.[1] To realize such ICs, transistors with high breakdown voltage, very high current gain cut off frequency ft and very high power gain cutoff frequency fmax are essential. Transferred substrate single heterojunction bipolar transistors (SHBTs) have demonstrated very high bandwidth and are potential candidates for very high speed integrated circuit applications.[2,3]. The transferred substrate SHBTs, however, have very low breakdown voltage, $BV_{CEO} \sim 1.5$ V. Here we report transferred-substrate DHBTs with emitter junction widths as small as 0.3 μm for the emitter and 1.0 μm for the collector. These exhibit a record 462 GHz f_{max} .

Table. I shows the MBE grown layer structure. As heat flows through the emitter, a thin 300 Å InGaAs emitter contact layer was used for low thermal resistance. We used compositionally graded InGaAs/InAlAs layers at each interface between InP and InGaAs layers. The base layer is 400 Å thick and is Be-doped at $4\times10^{19}/cm^3$. To reduce the base transit time, we designed the base layer with 50 meV band gap grading, introduced by varying the Ga:In ratio. The 0.5, 0.7 and 1.0 μm × 8 μm emitter contact metal was defined by optical projection lithography. The emitter-base mesa was formed by selective wet etching followed by nonselective citric-based wet etching. Undercutting of the emitter metal during emitter etching is ~ 0.1 μm on each side of emitter. Subsequent steps include self aligned base ohmic contact deposition, base mesa isolation, polyimide passivation and planarization and interconnect metal evaporation.[2] Selective wet etching was used for base mesa isolation. The substrate transfer process includes Benzocyclobutene (BCB) coating, etching and plating to form vias and ground planes, binding to a transfer substrate with an In0.8Pb0.15Ag0.05 solder. Fig 1 shows the SEM image of device cross-section after BCB coating and curing. Schottky collector contact was made on a 3000 Å thick InP collector layer after removing the S.I. InP substrate in HCl.

Common emitter DC characteristics are similar to devices published earlier.[4] The offset voltage was 0.2 V and $V_{CE,sat}$ was 1 V, while the DC current gain $\beta \sim 43$. The $BV_{CEO} \sim 8$ V at $J_C \sim 5\times10^4$ A/cm^2. Extrapolating at 20 dB/decade, the power gain cut-off frequency f_{max} values are 343, 395, and 462 GHz for 1/1.5, 0.7/1.0, and 0.5/1.0 μm/μm of Emitter/Collector contact widths, respectively as shown in Fig. 2. Emitter stripe length is 8 μm in all HBTs. The optimum bias condition is V_{CE}=1.8 V and J_C~1.5 mA/μm^2. The current gain cut-off frequency $f_\tau \sim 139$ GHz at $I_c = 5$ mA and $V_{CE} = 1.8$ V for 0.5 μm emitter device. Fig. 3 shows the schematic diagram and the simulation results of small signal hybrid-π equivalent circuit model for the devices with 462 GHz. According to this simulation results, it is clear that an extremely small C_{cbi} ~2.3 fF, which can be achieved in transferred substrate technology, produces ultra high f_{max} ~ 462 GHz.

REFERENCES

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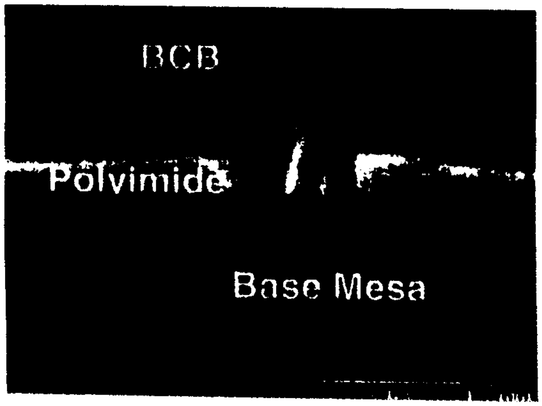
Layer	Material	Doping	Thickness (Å)
Emitter Cap	InGaAs	1×10^{19} : Si	300
Grade	InGaAs/ InAlAs	1×10^{19} : Si	200
N^{++} Emitter	InP	1×10^{19} : Si	900
N^{-} Emitter	InP	8×10^{17} : Si	300
Grade	InGaAs/ InAlAs	8×10^{17} : Si	233
Grade	InGaAs/ InAlAs	8×10^{17} : Be	67
Base	InGaAs	4×10^{19} : Be	400
Grade	InGaAs/ InAlAs	1×10^{16} : Si	480
Delta Doping	InP	1.6×10^{18} : Si	20
Collector	InP	1×10^{16} : Si	2500

Table 1. Layer structure of mbe grown InP/InGaAs/InP DHBT



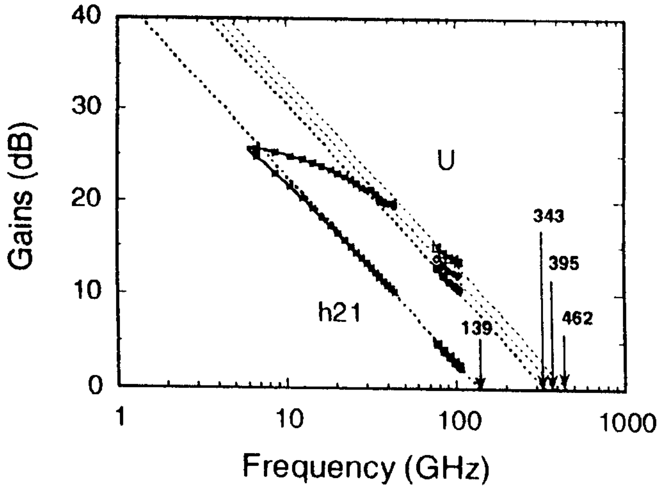


Fig. 1.(left) SEM of device cross-section after BCB coating and curing. Emitter contact metal width is 0.5 μm.
Fig. 2. (right) Small signal current and power gains vs. frequency at $J_C \sim 1.5$ mA/um^2 and $V_{CE} = 1.8$ V for 0.5/1.0(□), 0.7/1.0(◊) and 1.0/1.5(•) um Emitter/Collector contact width devices.

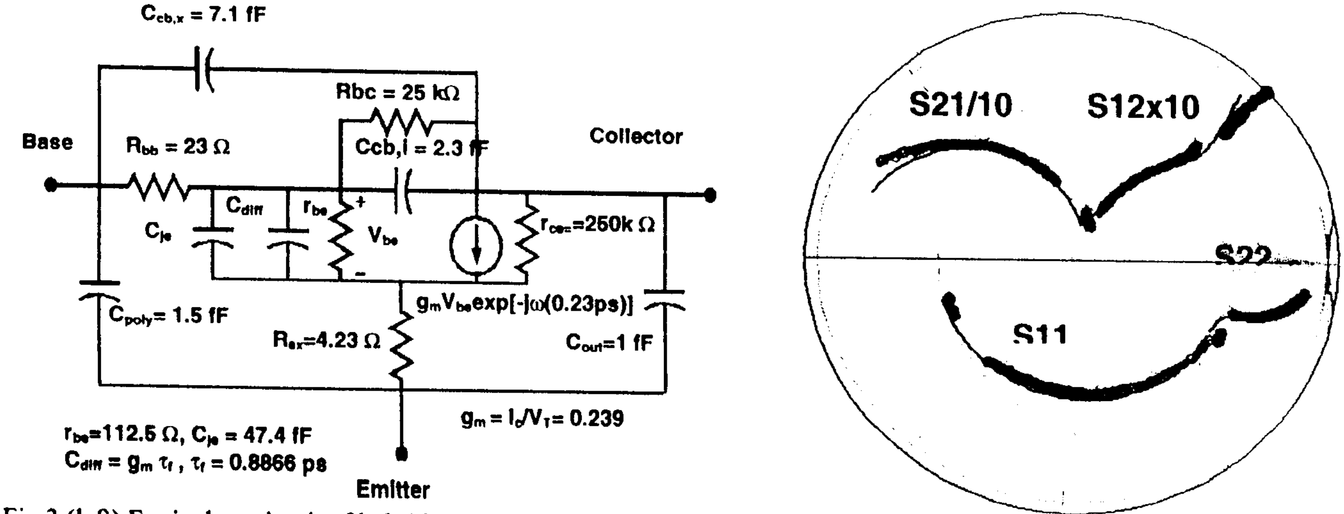


Fig.3 (left) Equivalent circuit of hybrid π model for 0.5/1.0 um Emitter/Collector contact width device. (Right) Comparison of experimental (circle) and simulated (line) S-parameters.