Molecular Beam Deposition of Low-Resistance Polycrystalline InAs

D. Scott, M. Urteaga, N. Parthasarathy, J.H. English and M.J.W. Rodwell
Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106
Tel: (805) 893-8044, Fax: (805) 893-3262, dennis@umail.ucsb.edu

Abstract

We report low-resistance Si-doped polycrystalline InAs (poly-InAs:Si) using molecular beam deposition. We believe this to be the first report of low resistance in poly-InAs. The poly-InAs:Si was deposited using conventional molecular beam epitaxy (MBE) onto SiN_x coated GaAs substrates at various growth temperatures and deposition rates. Poly-InAs samples with thicknesses of 2000Å and 1000Å were grown for Hall and TLM measurements, respectively. We have observed electron concentrations from 8.8×10^{18} to 1.5×10^{19} cm^{-3} and respective mobilities from 886 to 441 cm^2/Vs. This range of values suggests that the poly-InAs:Si has a doping-mobility product, and hence bulk conductivity, that is only 3-4 times lower than that of similarly doped InGaAs lattice-matched to InP. The typical bulk resistivity determined by TLM measurements is approximately 1.4×10^{-3} Ω-cm. Contact resistance to the poly-InAs with a Ti/Pt/Au metal stack less than 1.6×10^{-7} Ω-cm^2. The combined low contact access resistance and low junction capacitance found in poly-InAs:Si may be useful in a variety of III-V device applications.

1. Introduction

Heavily doped polycrystalline silicon (polysilicon) is commonly used in the fabrication of Si- and SiGe-based bipolar junction transistors (BJTs) and heterojunction bipolar transistors (HBTs). Polysilicon is used in the extrinsic base contact of Si-based transistors to obtain reduced base contact resistance and lower base-collector capacitance (C_{bc}). Heavily doped polysilicon is used to form the diffused, self-aligned emitter and an extrinsic emitter contact that is much wider than the active base-emitter junction [1,2]. Low-resistance, p-type polycrystalline GaAs (poly-GaAs) has been reported as an analogous extrinsic base contact material for use in III-V HBTs [3,4]. In this application, low-resistance poly-GaAs might been used with a dielectric buried in the extrinsic base-collector area to reduce C_{bc} while maintaining a low base contact resistance [5], as analogous to established SiGe HBT processes [2]. The poly-GaAs work achieved a lowest resistivity of approximately 5×10^{-3} Ω-cm with a hole concentration of 8.4×10^{20} cm^{-3} [4].

This work is meant to demonstrate a low-resistance polycrystalline material that may be suitable for use as an extrinsic emitter contact that is much wider than the active base-emitter junction. N-type poly-InAs:Si has been found to have resistivities as low as 1.4×10^{-3} Ω-cm and contact resistance to a Ti/Pt/Au metal stack of less than 1.6×10^{-7} Ω-cm^2. We have used the low-resistance poly-InAs in an HBT utilizing non-selective-area regrowth in the

formation of the emitter-base heterojuction [6]. In general, combined low contact access resistance and low junction capacitance may also be useful in a variety of III-V device applications through the formation of a wide, extrinsic n-type contact layer deposited over a narrow semiconductor mesa and planarized by a buried dielectric.

2. Experimental Procedure

Poly-InAs:Si was grown in a modified Varian GenII solid-source MBE system. The poly-InAs was deposited on (100) semi-insulating GaAs substrates coated by PECVD with 3000Å of SiN_x. The deposition temperature of the substrate was determined by pyrometer and was typically maintained at approximately 480°C. The deposition rates varied from 0.21-0.77 µm/h. The SiN_x coated wafers were first raised to a temperature above 550°C in the MBE growth chamber. Hydrogen was allowed to escape from the SiN_x coated wafers until the baseline pressure of the growth chamber was achieved. The wafer temperature was then lowered to the desired growth temperature, and the Si-doped InAs was deposited. For studies of the bulk material, 2000Å of poly-InAs:Si was deposited directly onto the SiN_x coated wafers. For studies of the electrical characteristics, 1000Å of poly-InAs was grown on top of approximately 2000Å of polycrystalline InAlAs. The polycrystalline InAlAs is assumed to be highly resistive and of low mobility similar to that shown in published work on polycrystalline InGaAs [7] and our own experience with polycrystalline ternaries. Electron concentration and mobility were determined by room temperature Hall measurements. Resistance data were determined by TLM measurements using a Ti/Pt/Au metal stack. The grain size of the poly-InAs was examined by scanning electron microscopy (SEM).

3. Results and Discussion

The dependence of electron concentration and mobility of the doped poly-InAs:Si on the doping cell temperature is shown in Fig. 1. The substrate growth temperature was 480°C, and the growth rate was 0.71 µm/h. The Si cell temperature was varied between 965-995°C in these growths. As expected, the electron concentration increases with the doping cell temperature, and the mobility decreases with increased carrier concentration. In this range of increasing doping cell temperature, the electron concentration increases from 8.8×10^{18} to 1.5×10^{19} cm^{-3} and the mobility decreases from 886 to 441 cm^2/Vs. For comparison, InGaAs lattice matched to InP and grown at similar conditions has electron concentrations ranging from 1.2×10^{19} to 4.3×10^{19} cm^{-3} and mobility less than 2500 cm^2/Vs in this range of doping cell temperatures. This comparison suggests that the poly-InAs:Si has a doping-mobility product, and hence bulk conductivity, that is only 3-4 times lower than that of the lattice-matched InGaAs typically used as the capping layer in InP-based HBTs. This demonstrates that poly-InAs:Si may be a suitable material for use as an extrinsic emitter contact.

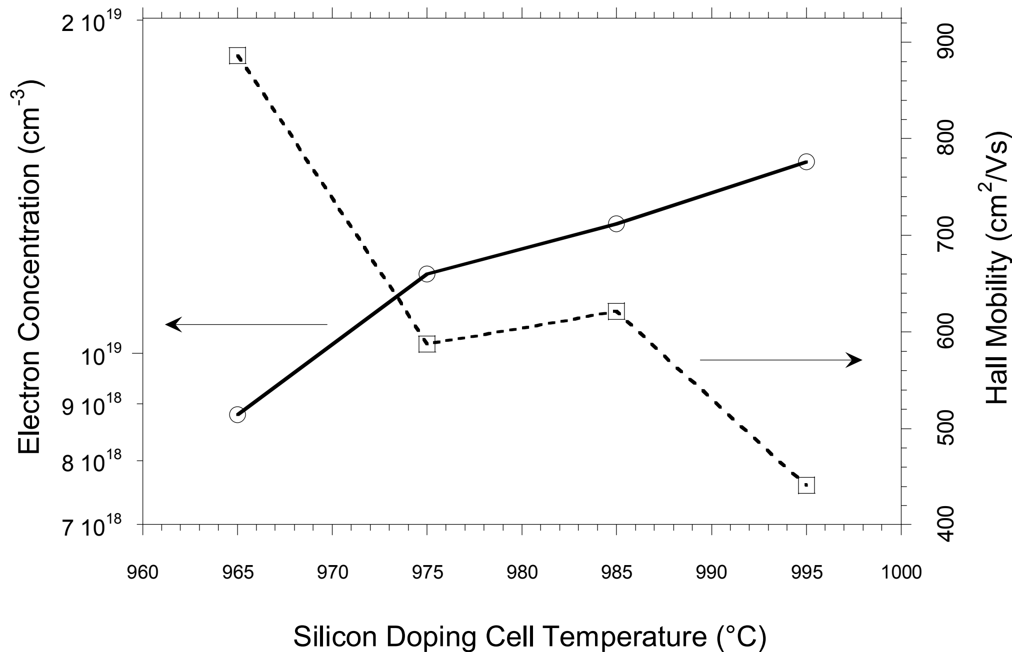


Figure 1. Doping cell temperature dependence of electron concentration and Hall mobility.

The dependence of electron concentration and mobility of the doped poly-InAs:Si on the substrate growth temperature is shown in Fig. 2. The substrate temperature was varied from 400-490°C while the Si doping cell temperature was maintained at 980°C for all of these growths. The growth rate was lowered to 0.21 μm/h for this series of growths to determine the effect of growth rate on the poly-InAs:Si material. As substrate temperature increases from 400-490°C, the doping decreases from 1.8×10^{18} to 8.1×10^{17} cm^{-3} and the mobility increases from 793 to 476 cm^2/Vs. This data suggests that the bulk conductivity is slightly higher for the lower growth temperatures.

Studies in poly-GaAs:Be report observations of increased resistivity with increased polycrystalline grain size [4,8]. The polycrystalline grain size was increased in the poly-GaAs studies by increasing the substrate growth temperature. The observed increase in resistivity was unexpected, as mobility is expected to increase with larger polycrystalline grain size and resistivity is expected to decrease. Although the mobility was found to increase with grain size in these reports, the hole concentration simultaneously decreased and lead to an overall decrease in the resistivity. To date, similar trends have not been observed in our poly-InAs:Si data. Increasing the growth rate from 0.21 to 0.71 μm/h is observed to strongly impact polycrystalline grain size and doping while having a minimal effect on the Hall mobility. The electron concentration shown in Fig. 1 (growth rate of 0.71 μm/h) is an order of magnitude higher than that shown in Fig. 2 (growth rate of 0.21 μm/h) at similar

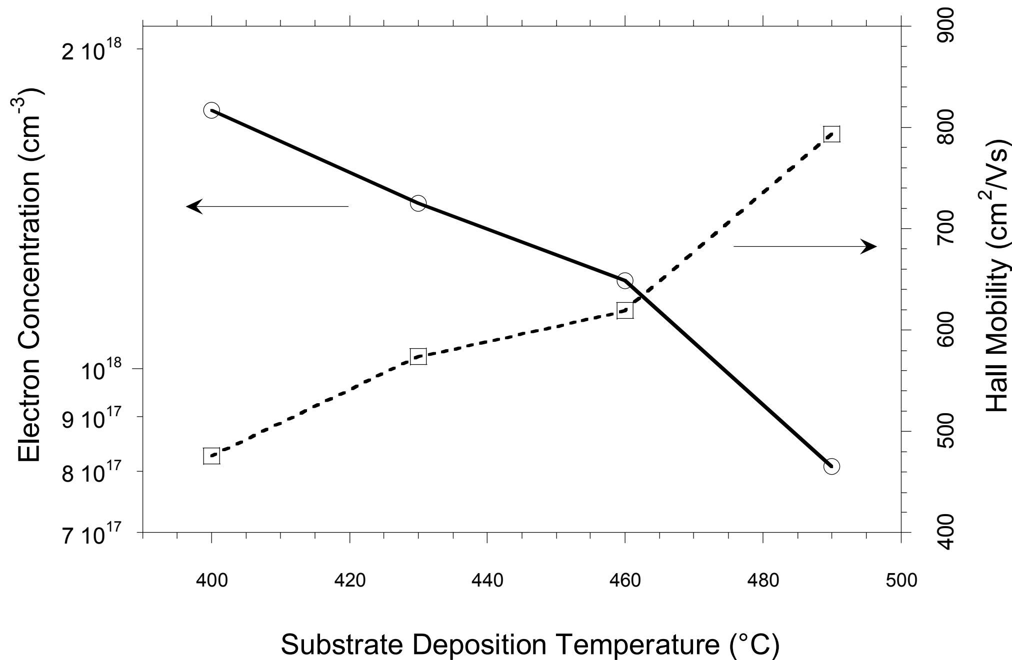
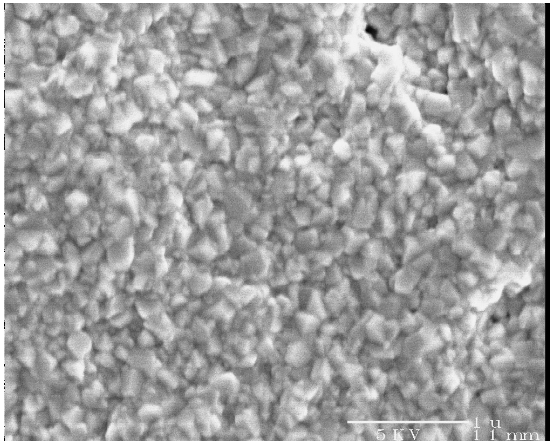


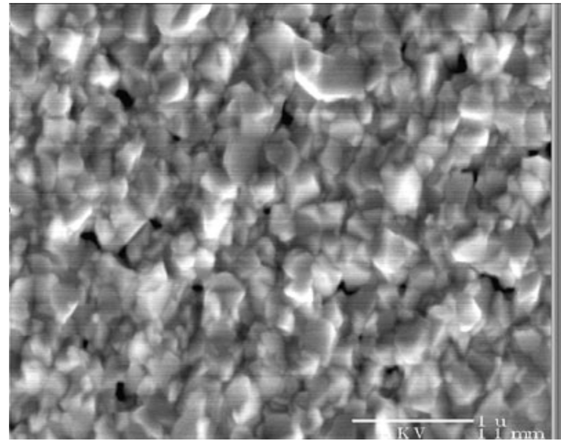
Figure 2. Substrate temperature dependence of electron concentration and Hall mobility.

substrate and dopant cell temperatures. Figure 3 shows the typical surface morphology of the poly-InAs:Si at these growth rates. The SEM images show the material at the same magnification so the difference in the polycrystalline grain size and density may be compared. Figure 3(a) shows poly-InAs:Si deposited at a rate of 0.71 μm/h. The grain sizes in Fig. 3(a) are smaller than those grown at the lower rate, as shown in Fig. 3(b). A grain size of approximately 130 nm is obtained at the higher deposition rate, and the polycrystalline grains for the lower growth rate average about 190 nm in size. The poly-InAs:Si grain size is not observed to vary significantly in our data with variations in growth temperature.

TLM structures have been used to determine the bulk resistivity and contact resistance of the poly-InAs:Si. We have used the poly-InAs:Si as the emitter cap and extrinsic emitter contact in an HBT utilizing non-selective-area regrowth in the formation of the emitter-base heterojuction [6]. The HBT utilizes the poly-InAs as a low-resistivity emitter contact with an area larger than that of the base-emitter junction, allowing for low emitter resistance while shrinking the active base-emitter junction area. A cross-section of the base-emitter junction with the poly-InAs cap and a schematic of the transistor are shown in Fig. 4. The substrate temperature is set to 480°C during the poly-InAs:Si growth of the HBTs, and the growth rate is typically about 0.70 μm/h. The typical bulk resistivity is approximately 1.4×10^{-3} Ω-cm. Contact resistance to the poly-InAs with a Ti/Pt/Au metal stack less than 1.6×10^{-7} Ω-cm^2.

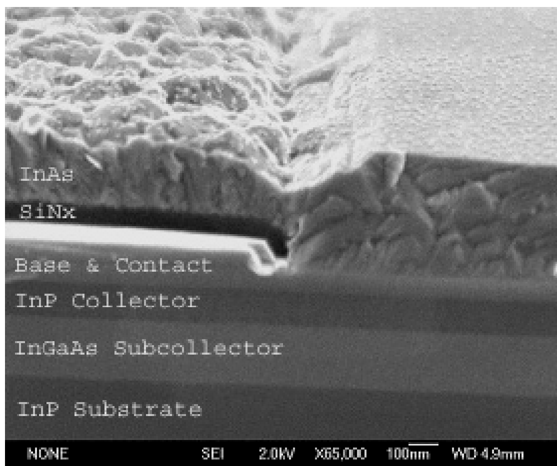


(a)

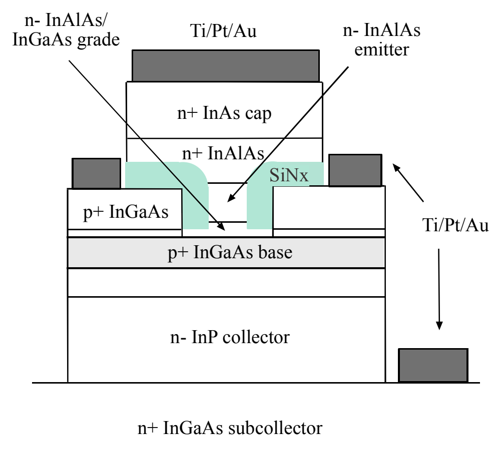


(b)

Figure 3. SEM images of typical poly-InAs morphology when grown at (a) 0.71 μm/h and (b) 0.21 μm/h.



(a)



(b)

Figure 4. (a) SEM cross-section of the regrown emitter HBT showing the polycrystalline regrowth (left) and the regrowth on crystalline material (right). (b) HBT schematic with poly-InAs emitter cap.

4. Conclusion

We report, for the first time, that low-resistance poly-InAs:Si can be achieved. The low-resistance polycrystalline material may be suitable in III-V HBTs for use as an extrinsic emitter contact in the non-selective regrowth of the emitter-base heterojuction. In addition, the material may also be useful in other III-V devices where low contact access resistance and low junction capacitance are desired.

References

[1] K. Washio, “Self-aligned Si BJT/SiGe HBT technology and its application to high-speed circuits”, International Journal of High Speed Electronics and Systems, vol.11, no.1, World Scientific, pp.77-114, March 2001.

[2] S.J. Jeng, B. Jagannathan, J.-S. Rieh, J. Johnson, K.T. Schonenberg, D. Greenberg, A. Stricker, H. Chen, M. Khater, D. Ahlgren, G. Freeman, K. Stein, S. Subbanna, **“**A 210-GHz f/sub T/ SiGe HBT with a non-self-aligned structure”, IEEE Electron Device Letters, vol.22, no.11, pp. 542-4 November 2001

[3] K. Mochizuki, T. Nakamura, “Comparison of Be and C diffusion in heavily doped polycrystalline GaAs”, Applied Physics Letters, vol.65, no.16, pp.2066-8, 17 Oct. 1994.

[4] N.Y. Li, C.W. Tu, “Low-resistance polycrystalline GaAs grown by gas-source molecular beam epitaxy using CBr_4”, Journal of Crystal Growth, vol.188, no.1-4, pp.45-9, June 1998.

[5] T. Oka, K. Hirata, K. Ouchi, H. Uchiyama, K. Mochizuki, T. Nakamura, “Small-scaled InGaP/GaAs HBTs with WSi/Ti base electrode and buried SiO_2”, IEEE Transactions on Electron Devices, vol.45, no.11, pp. 2276-82, Nov. 1998.

[6] D. Scott, H. Xing, S. Krishnan, M. Urteaga, N. Parthasarathy, M. Rodwell, “InAlAs/ InGaAs/InP DHBTs with Polycrystalline InAs Extrinsic Emitter Regrowth”, 2002 Device Research Conference Conference Digest, pp. 171-2.

[7] K. Mochizuki, T. Oka, T. Nakamura, “Molecular beam deposition of n-type polycrystalline $In_{0.6}Ga_{0.4}As$ for high resistances in heterojunction bipolar transistor integrated circuits”, Electronics Letters, vol.33, no.13, p. 1181, 19 June 1997.

[8] K. Mochizuki, T. Nakamura, T. Mishima, H. Masuda, T. Tanoue, T. **“**Molecular beam deposition of low-resistance polycrystalline GaAs”, Journal of Electronic Materials, vol.23, no.6, pp.577-80, June 1994.

Acknowledgements

This work is supported by the Office of Naval Research (Contract No. N0014-99-1-0041)