InP-based HBTs: Devices and GHz mixed-signal ICs

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Applications:

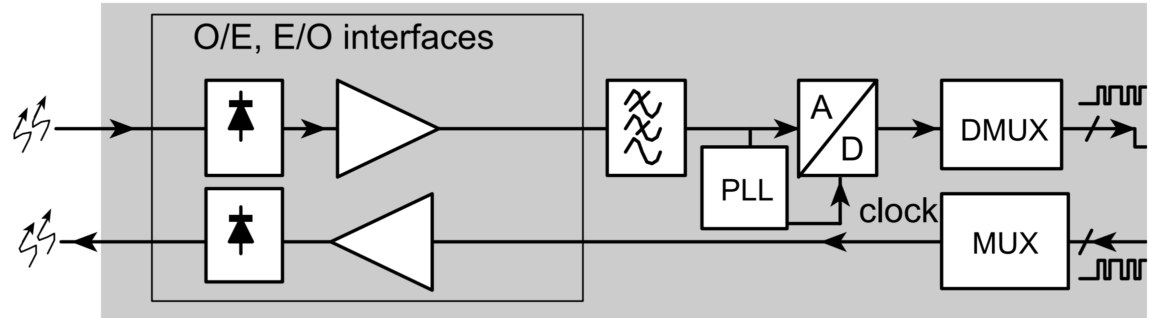
Applications: optical fiber transceivers at 40 Gb/s and higher

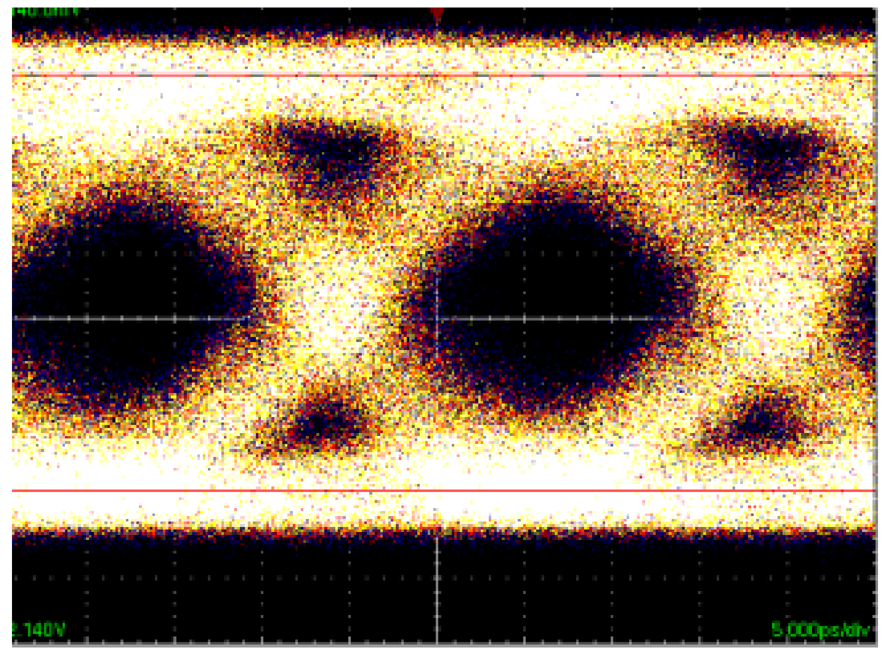
Key advantages for:
TIA, LIA, Modulator driver

Closer competition with SiGe:
MUX/CMU, DMUX/CDR
lower power
problems with integration scale

"40 Gb" is often 44, 48, or 52…
increases InP leverage over SiGe

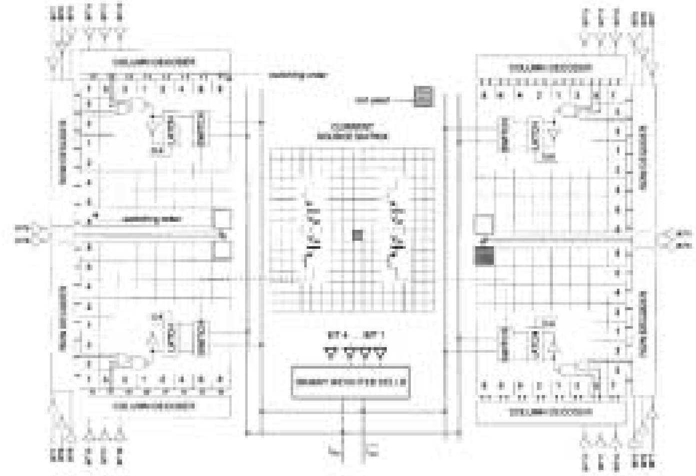
80 & 160 Gb may come in time
world may not need capacity for some time
WDM might be better use of fiber bandwidth





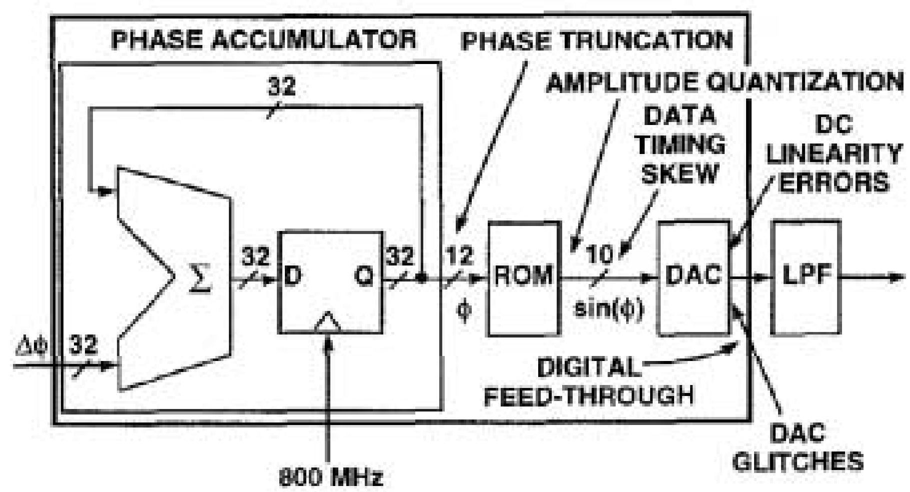
Applications: military mixed-signal ICs

Radar/Comms transmitter electronics
direct digital frequency synthesis
accumulator, sine ROM, DAC



Radar/Comms receiver electronics
high resolution ADC

Technology requirements
3,000 to 30,000 transistors
Few GHz IF (operating) bandwidths
~160 dB/Hz dynamic range



high resolution drives technology
speed far beyond signal bandwidth

50-100 GHz clock rate digital technologies sought

Applications: wireless / RF

Present Wireless/RF ICs
GaAs HBTs at lower frequencies
InGaAs PHEMTs in higher bands

Opportunities for InP
33 GHz LMDS and 60 GHz metropolitan area networks (IEEE 802.16)
cheap GaAs HBT processes → cheap InP HBT processes
200 GHz f_t and f_{max} , 8 V BVCEO
quick migration to 6" wafers enabled by metamorphic growth on GaAs

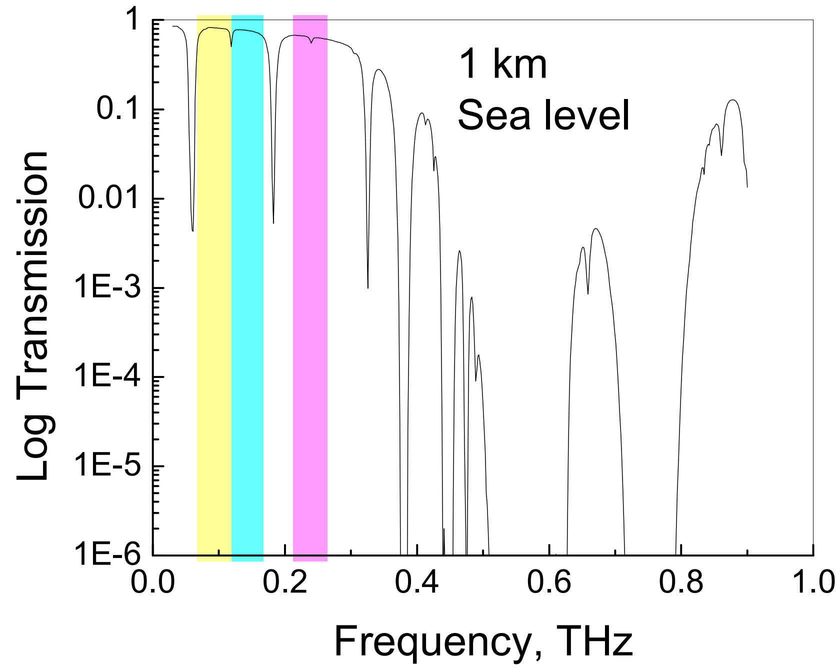
Longer-term opportunities for InP
wider range of RF/wireless applications
…IF SiGe-like integration scales can be reached.

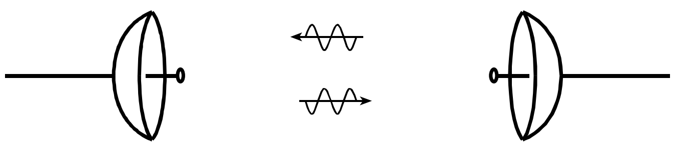
mmWave Transmission

UCSB

Atmospheric attenuation is LOW (~4 dB/km) at bands of interest
60-80 GHz, 120-160 GHz, 220-300 GHz

(Weather permitting)





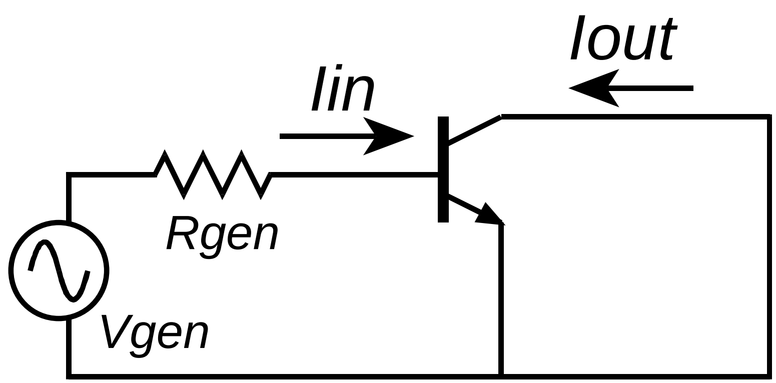
Geometric path losses are LOW due to short wavelengths.

55 mW transmitter power sufficient for 10 Gb/s transmission over 500 meters range.

Bit rate	**1.00E+10**	1/sec	
carrier frequency	**1.50E+11**	Hz	
F	**10**	dB	receiver noise figure
Distance	**5.00E+02**	m	transmission range
atmospheric loss	**4.00E-03**	dB/m	dB loss per unit distance
Dant, trans	**0.1**	m	transmit antenna diameter
Dant, rcvr	**0.1**	m	receive antenna diameter
bits/symbol	1		
kT	-173.83	dBm (1Hz)	
Prec	-48.27	dBm	received power at 10^{-9} B.E.R
Δf	1.00E+10	Hz	RF channel bandwidth required
transmission	-63.68		geometric path loss, dB
atmospheric loss	**2**	dB	total atmospheric loss, dB
Ptransmitter	55.1	mW	required transmitter power

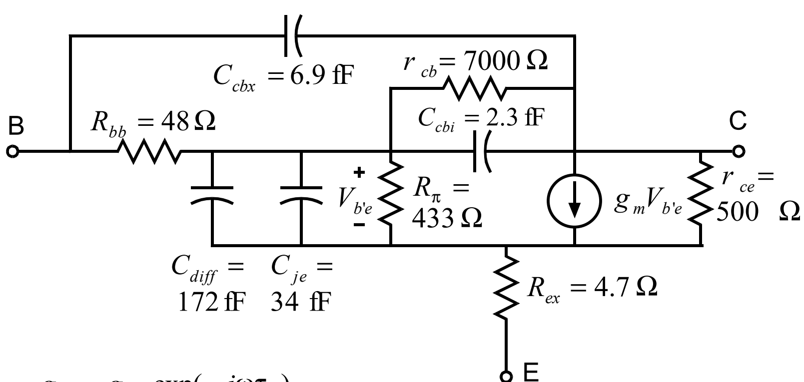
Transistor Figures of Merit

Short-circuit current gain cutoff frequency

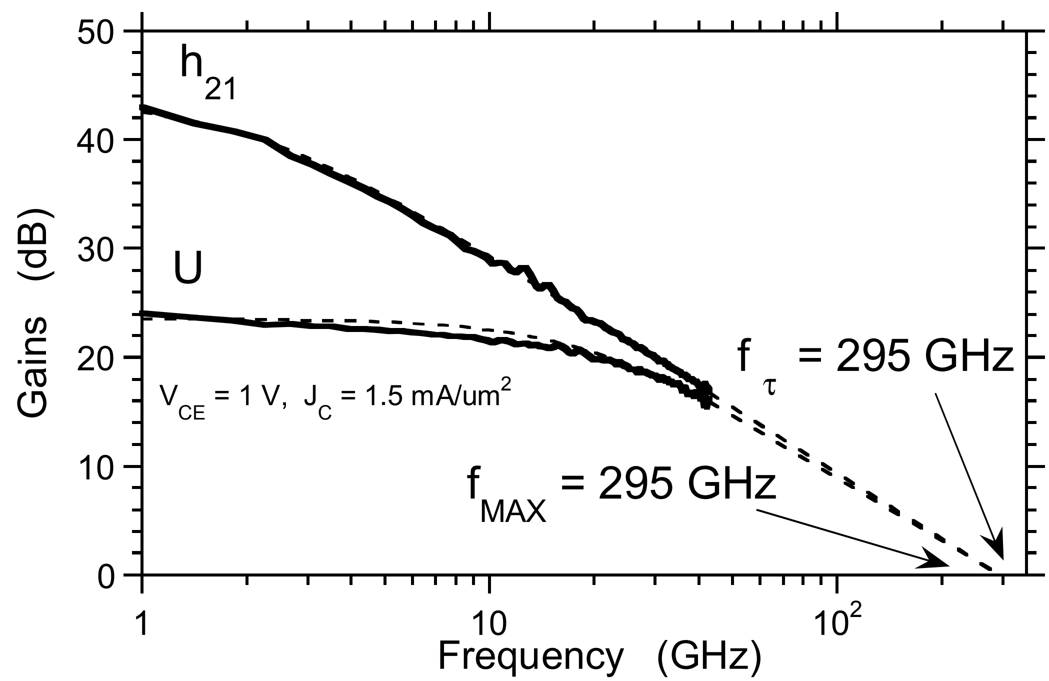


short-circuit current gain:
drive input, short output,
measure $H_{21}=I_{out}/I_{in}$

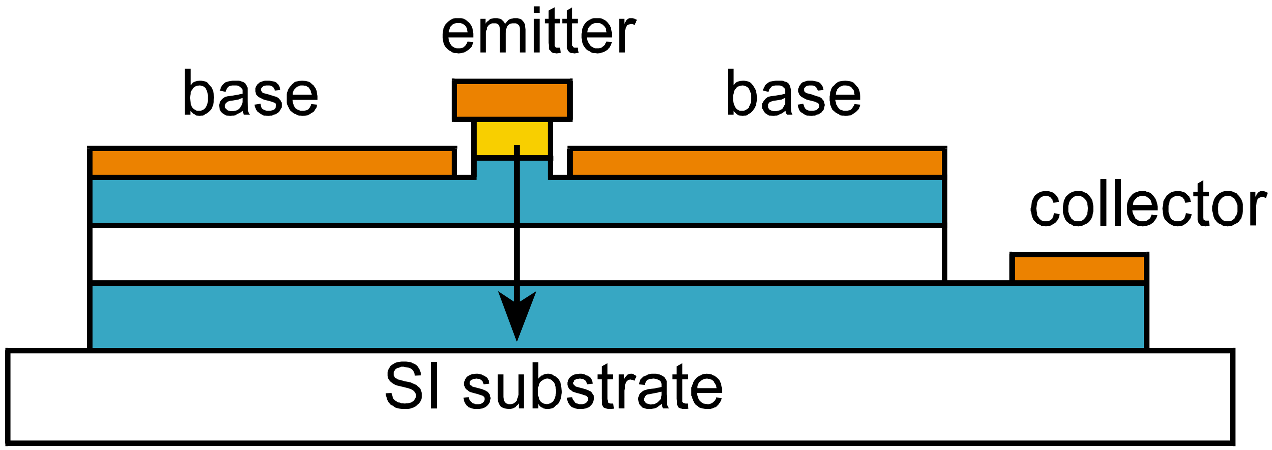
$$H_{21}(f)\approx\frac{1}{(1/\beta)+(jf/f_\tau)}$$



$$g_m = g_{mo}\exp(-j\omega\tau_c)$$
$$C_{diff} = g_{mo}\tau_f$$
$$R_\pi = \beta / g_m$$



Current-gain cutoff frequency in HBTs



$$\frac{1}{2\pi f_\tau} = \tau_{base} + \tau_{collector} + C_{je}\frac{kT}{qI_E} + C_{bc}\left(\frac{kT}{qI_E} + R_{ex} + R_{coll}\right)$$

$$\tau_{base} \approx T_b^2 / 2D_n \qquad \tau_{collector} \approx T_c / 2v_{sat}$$

RC terms are quite important for > 200 GHz f_τ devices
f_τ is a questionable metric for high speed digital logic
…where capacitance charging has proportionally larger role

Miguel Urteaga

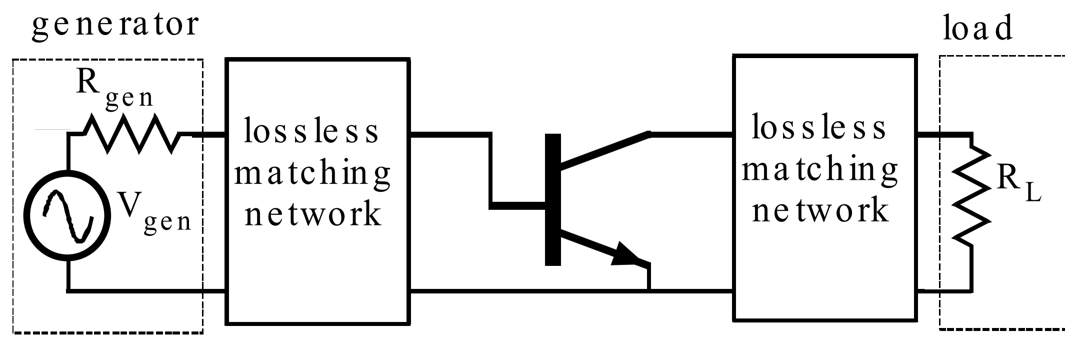
Measurement of power gains and f_{max}

Maximum Available Gain

Simultaneously match input and output of device

$$\mathbf{MAG} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right)$$

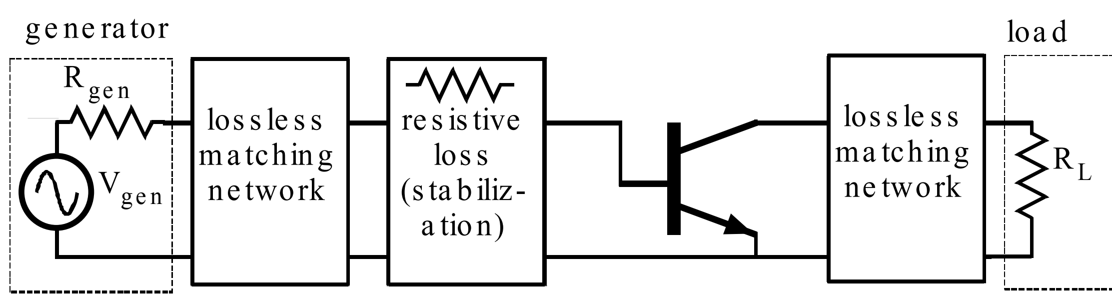
K = Rollet stability factor



Transistor must be unconditionally stable or MAG does not exist

Maximum Stable Gain

Stabilize transistor and simultaneously match input and output of device



$$\mathbf{MSG} = \frac{|S_{21}|}{|S_{12}|} = \frac{|Y_{21}|}{|Y_{12}|} \approx \frac{1}{\omega C_{cb}\left(R_{ex} + kT/qI_c\right)}$$

Approximate value for hybrid-π model

To first order MSG does not depend on f_τ or R_{bb}

For Hybrid- π model, MSG rolls off at 10 dB/decade, MAG has no fixed slope. So, NEITHER can be used to accurately extrapolate f_{max}

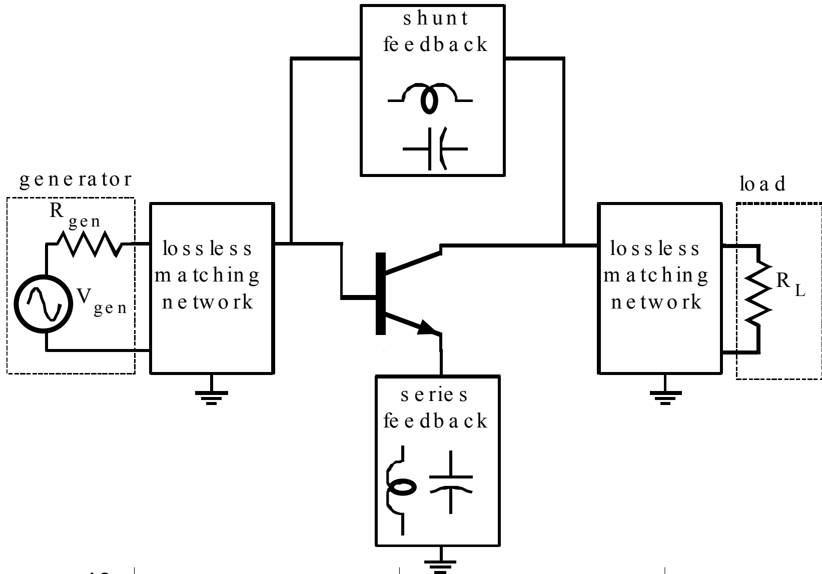
MSG/MAG is however of direct relevance in tuned RF amplifier design

Miguel Urteaga

Unilateral Power Gain

Mason's Unilateral Power Gain

Use lossless reactive feedback to cancel device feedback and stabilize the device, then match input/output.

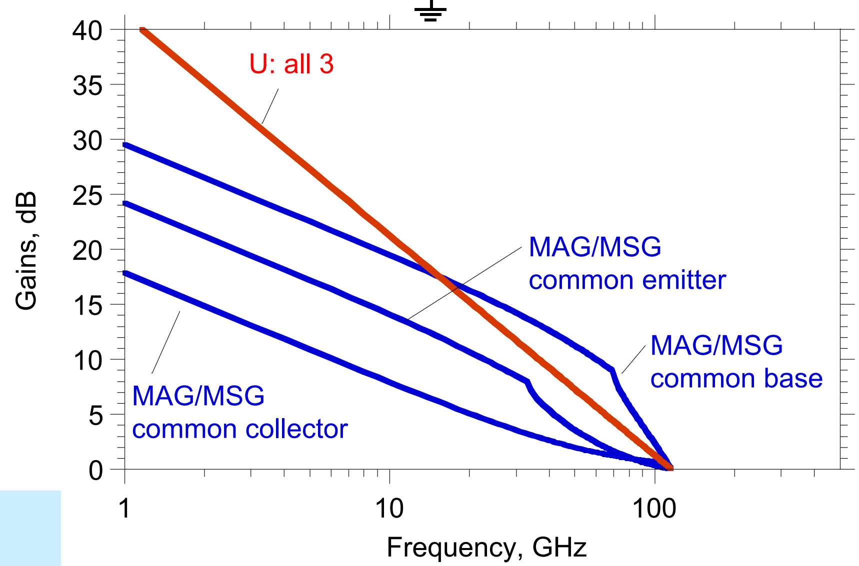


$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})}$$

U is not changed by pad reactances

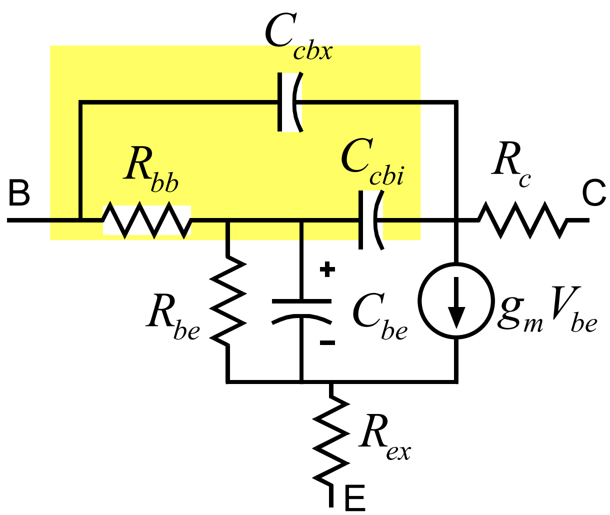
For Hybrid- π model,
U rolls off at 20 dB/decade

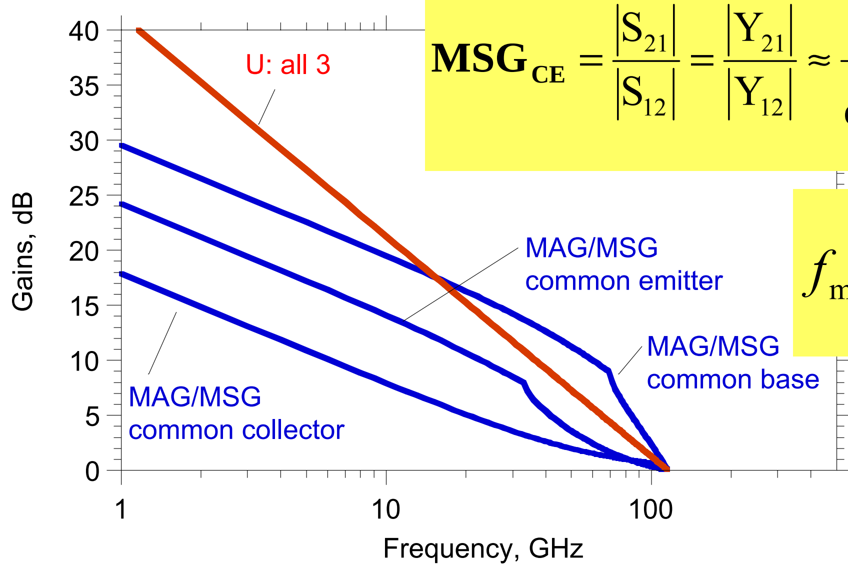
ALL Power Gains must be unity at f_{max}



Monolithic amplifiers not easily made unilateral, so U of only historical relevance to IC design.
U is *usually* valuable for f_{max} extrapolation

Excess Collector Capacitance, Fmax, and Device Utility





$$\mathbf{MSG}_{\mathbf{CE}} = \frac{|S_{21}|}{|S_{12}|} = \frac{|Y_{21}|}{|Y_{12}|} \approx \frac{1}{\omega C_{cb}\left(R_{ex} + kT/qI_c\right)}$$

$$f_{max} \cong \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cbi}}}$$

The partitioning between C_{cbi} and C_{cbx} will be discussed later.

C_{cbx} has no effect upon $f_{\max}$ or U.

C_{cbx} has a large impact upon common-emitter MSG,

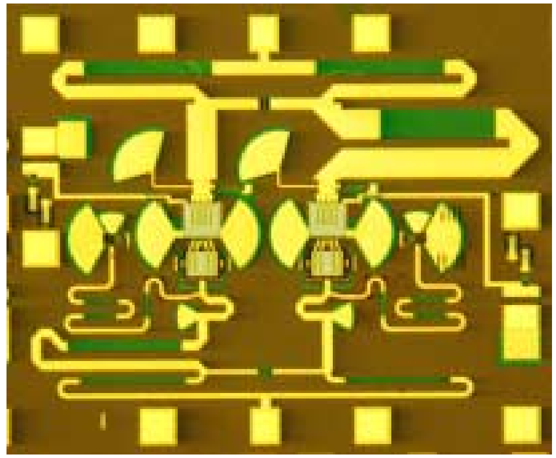
hence has large impact on usable gain in mm-wave circuits.

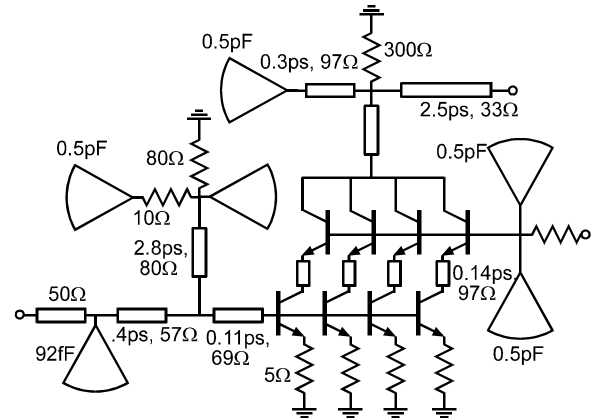
C_{cbx} has a large impact upon digital logic speed.

high f_{max} does not mean low C_{cb} or fast logic

What do we need: f_τ , f_{max} , or … ?

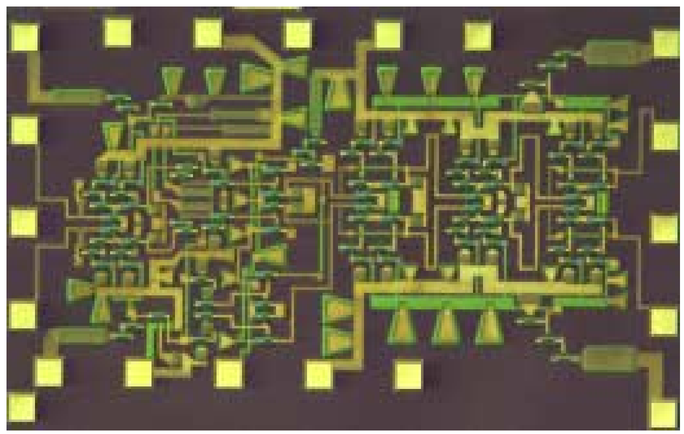
Tuned ICs (MIMICs, RF):
fmax sets gain,
& max frequency, not ft.
…low ft/fmax ratio makes tuning design hard (high Q)
high C_{cbx} reduces MSG

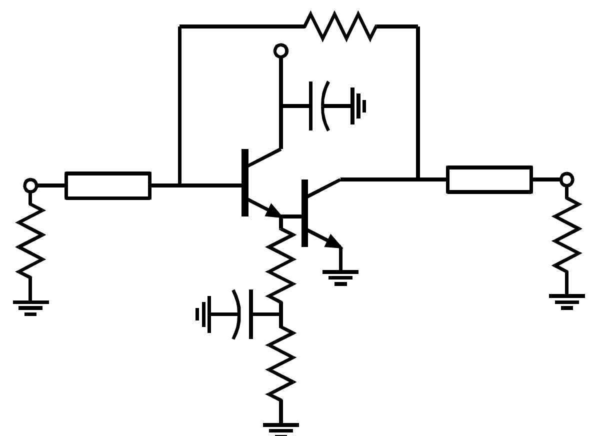




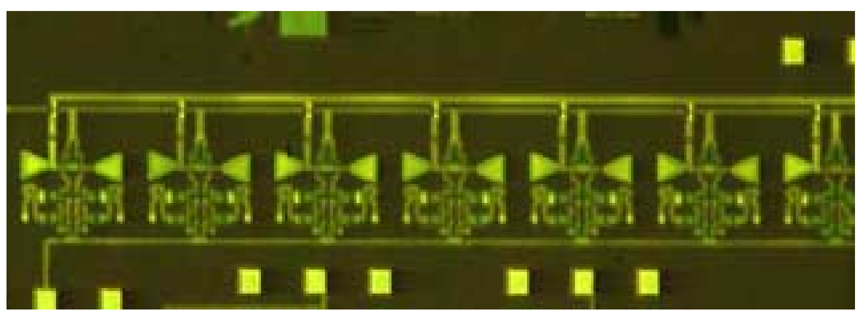
Lumped analog circuits
need high & comparable ft and fmax.

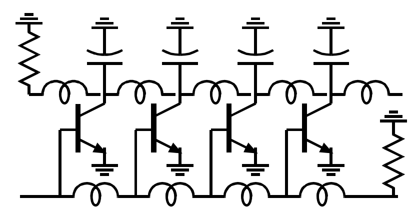
C_{cb}/I_c has major impact upon bandwidth





Distributed Amplifiers
in principle, fmax-limited,
ft not relevant….
(low ft makes design hard)



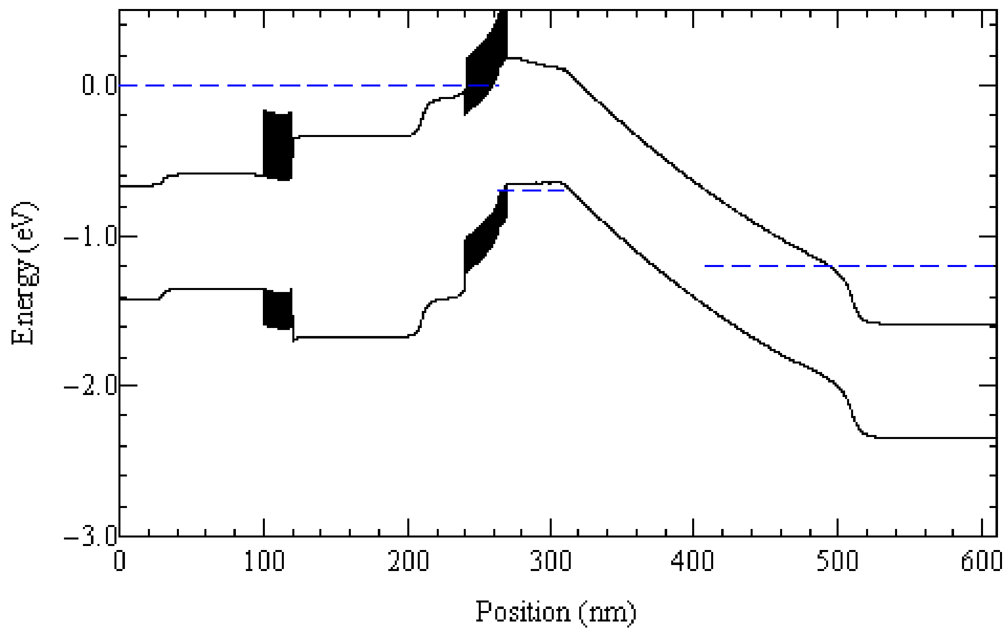


digital ICs will be discussed in detail later

transistor layer structures

SHBT layer structure

Layer	Material	Doping	Thickness (Å)
Emitter cap	$In_{0.53}Ga_{0.47}As$	2×10^{19} cm^{-3}: Si	300
N^+ emitter	InP	2×10^{19} cm^{-3}: Si	700
N^- emitter	InP	8×10^{17} cm^{-3}: Si	500
Emitter-base grade	$In_{0.53}Ga_{0.26}Al_{0.21}As$ to $In_{0.455}Ga_{0.545}As$	P: 4×10^{17} cm^{-3}: Si N: 8×10^{17} cm^{-3}: C	233 47
Base	$In_{0.53}Ga_{0.47}As$	N: 4×10^{19} cm^{-3}: C	400
Collector	$In_{0.53}Ga_{0.47}As$	N: 2×10^{16} cm^{-3}: Si	2000
Subcollector	InP	N: 1×10^{19} cm^{-3}: Si	~1000 Å



very low breakdown:
scaling beyond ~75 GHz
digital clock rate very difficult

high collector-base leakage
particularly at elevated temperatures.
Serious difficulties in real applications

very high thermal resistance
InGaAs collector and subcollector

DHBT Layer structure

PK Sundararajan

B-C grade design is critical

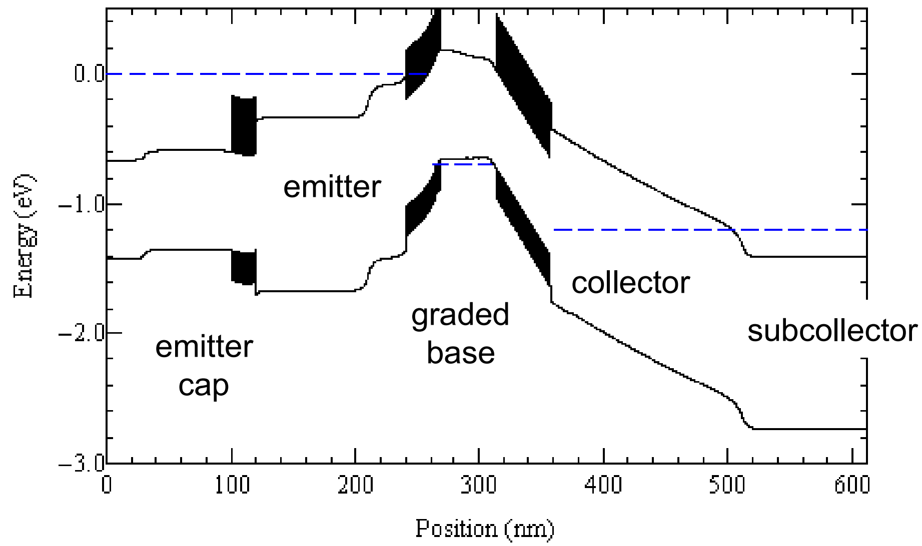
InGaAs or GaAsSb bases
GaAsSb more easily passivated
otherwise comparable

high breakdown
important for microwave power
important for logic

low thermal resistance
essential for high power density
important for microwave power
important for logic

Performance
ft and fmax good or better than SHBTs

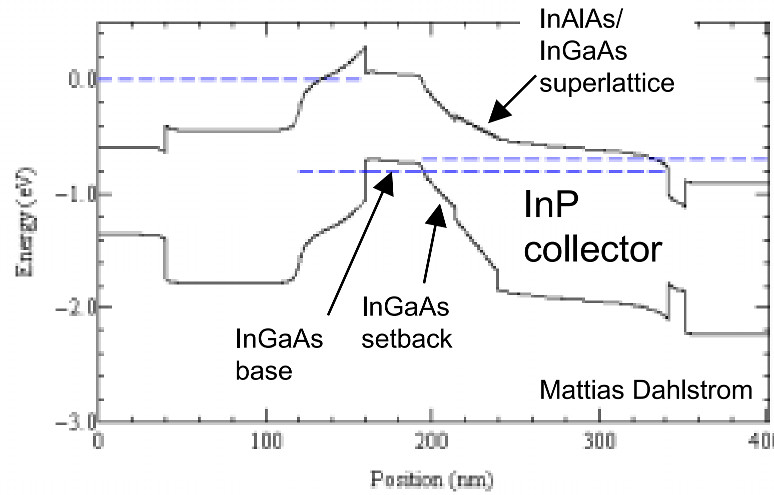
Layer	Material	Doping	Thickness (Å)
Emitter cap	$In_{0.53}Ga_{0.47}As$	2×10^{19} cm^{-3}: Si	300
N^+ emitter	InP	2×10^{19} cm^{-3}: Si	700
N^- emitter	InP	8×10^{17} cm^{-3}: Si	500
Emitter-base grade	$In_{0.53}Ga_{0.26}Al_{0.21}As$ to $In_{0.455}Ga_{0.545}As$	P: 4×10^{17} cm^{-3}: Si N: 8×10^{17} cm^{-3}: C	233 47
Base	$In_{0.53}Ga_{0.47}As$	N: 4×10^{19} cm^{-3}: C	400
Base-collector grade	$In_{0.53}Ga_{0.47}As$ to $In_{0.53}Ga_{0.26}Al_{0.21}As$	N: 2×10^{16} cm^{-3}: Si	240
Pulse doping	InP	5.6×10^{18} cm^{-3}: Si	30
Collector	InP	N: 2×10^{16} cm^{-3}: Si	1,630
Subcollector	InP	N: 1×10^{19} cm^{-3}: Si	~1000 Å



Alternative InP DHBT base-collector junction designs

Several layer alternatives exist for DHBTs with:
high ft
high current density
negligible current blocking
low base sheet and contact resistivity

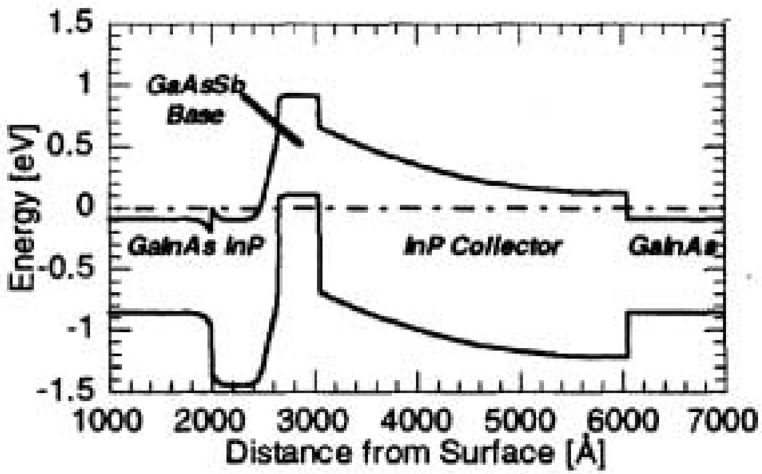
UCSB: InGaAs base, MBE



11th International Conference on Indium Phosphide and Related Materials
16-20 May 1999 Davos, Switzerland
TuA1-3

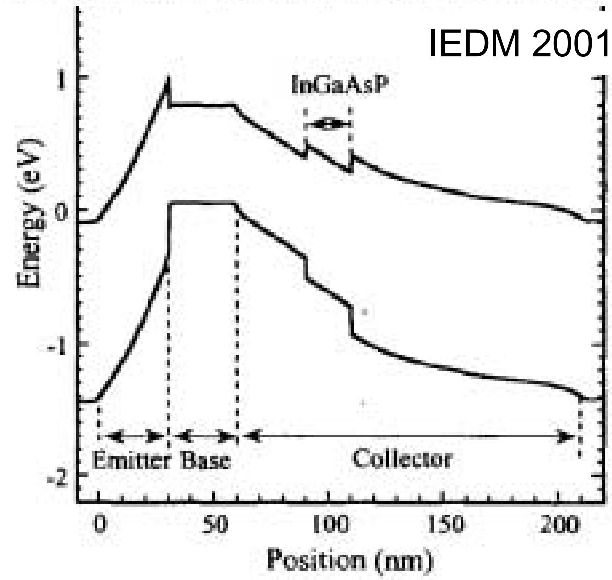
InP/GaAsSb/InP DOUBLE HETEROJUNCTION BIPOLAR TRANSISTORS WITH HIGH CUT-OFF FREQUENCIES AND BREAKDOWN VOLTAGES

N. Matine, M. W. Dvorak, X. G. Xu, S. P. Watkins, and C. R. Bolognesi



InP/InGaAs DHBTs with 341-GHz f_T at high current density of over 800 kA/cm^2

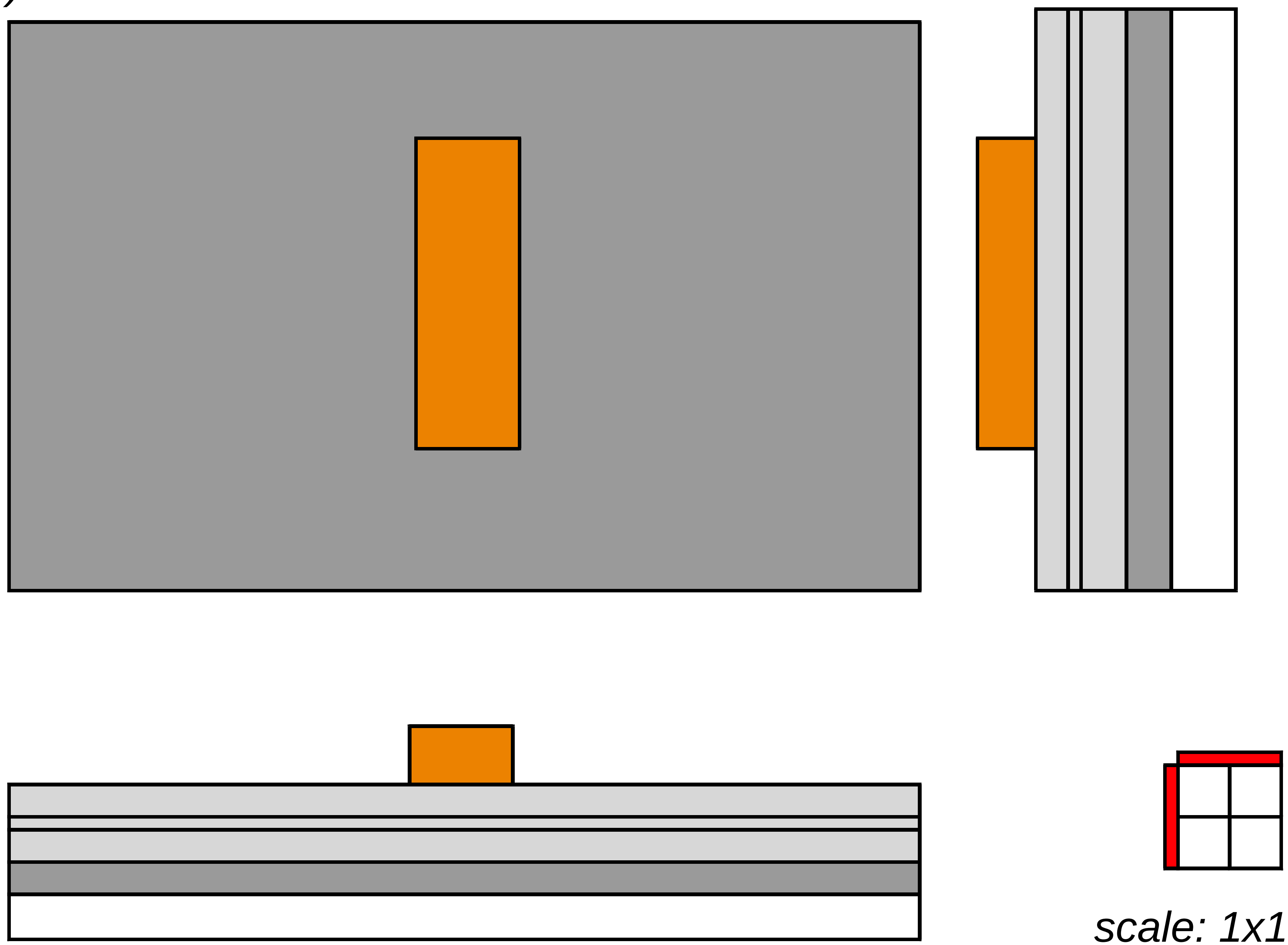
Minoru Ida, Kenji Kurishima, Noriyuki Watanabe, and Takatomo Enoki



transistor process flow

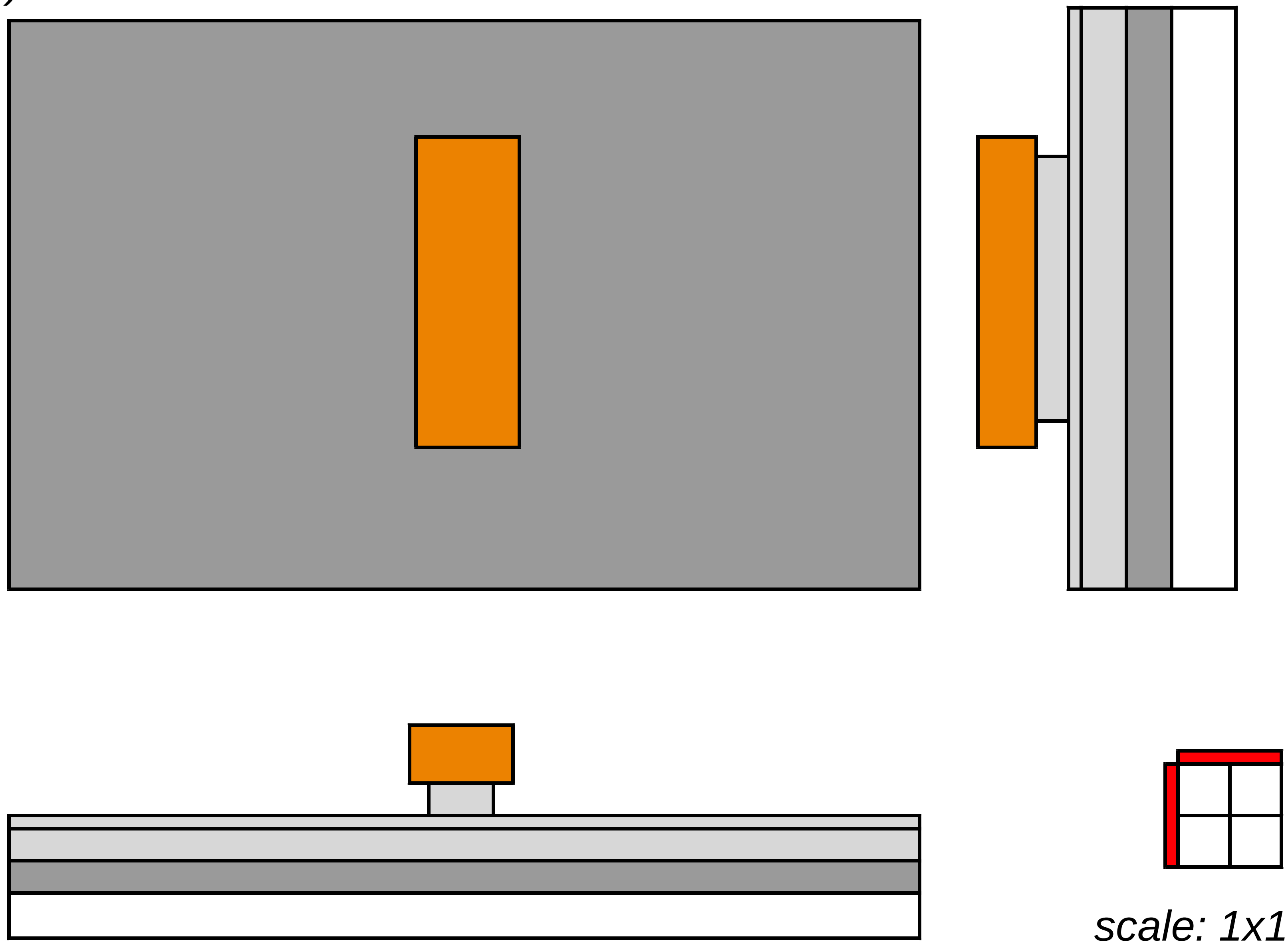
(research-lab-like)

1) emitter metal liftoff



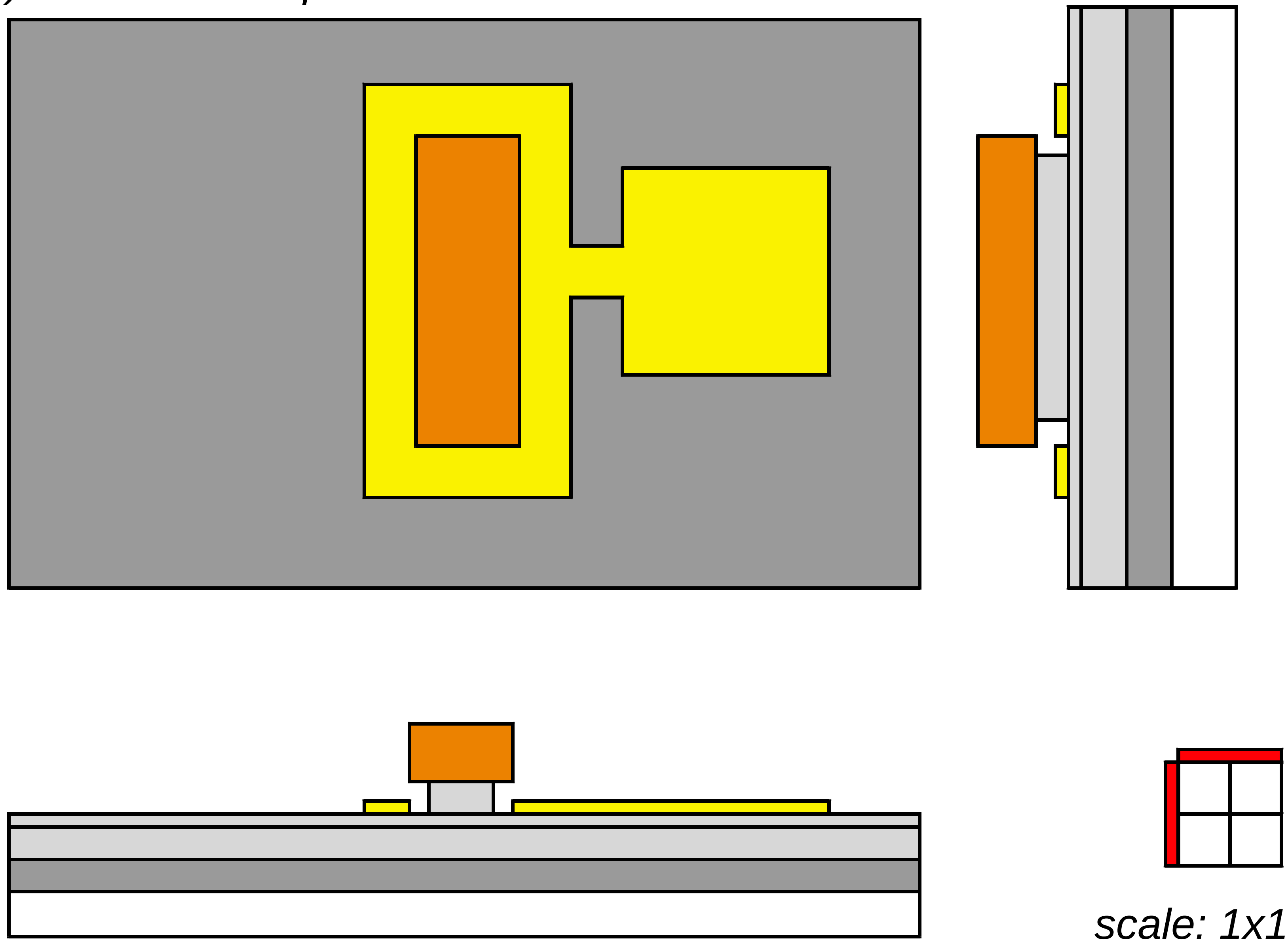
scale: 1x1 um

2) base recess etch



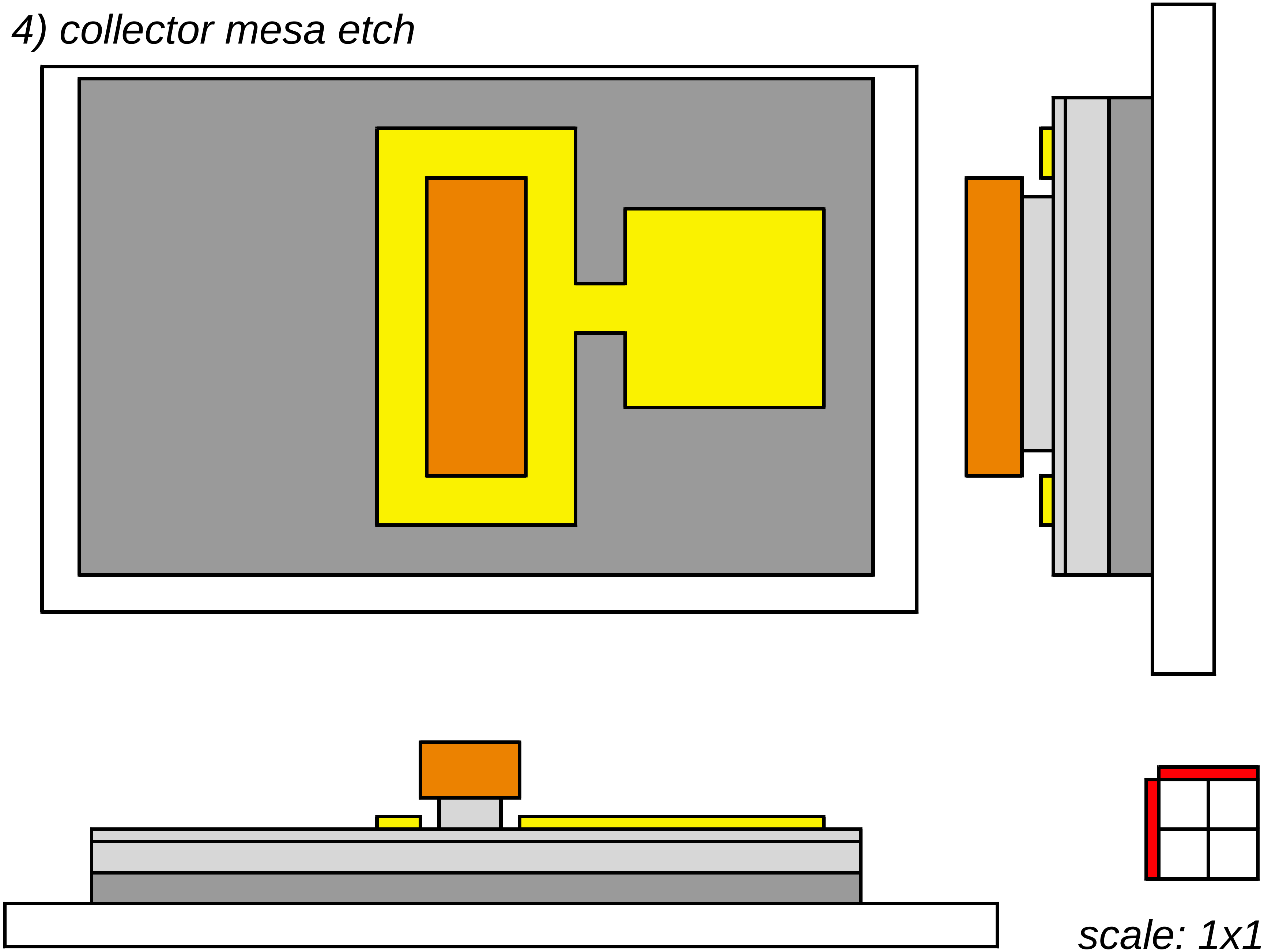
scale: 1x1 um

3) base metal deposition



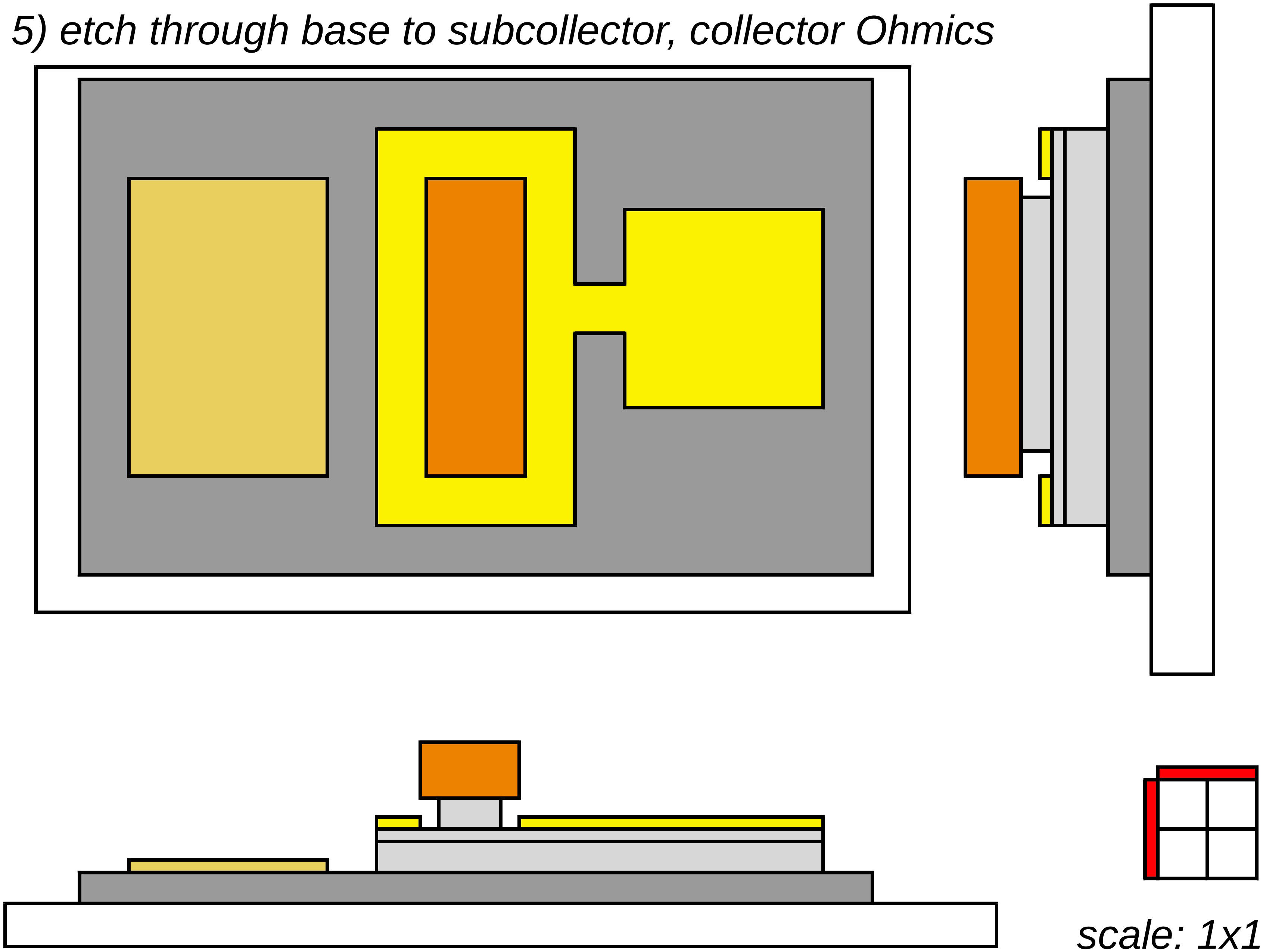
scale: 1x1 um

4) collector mesa etch



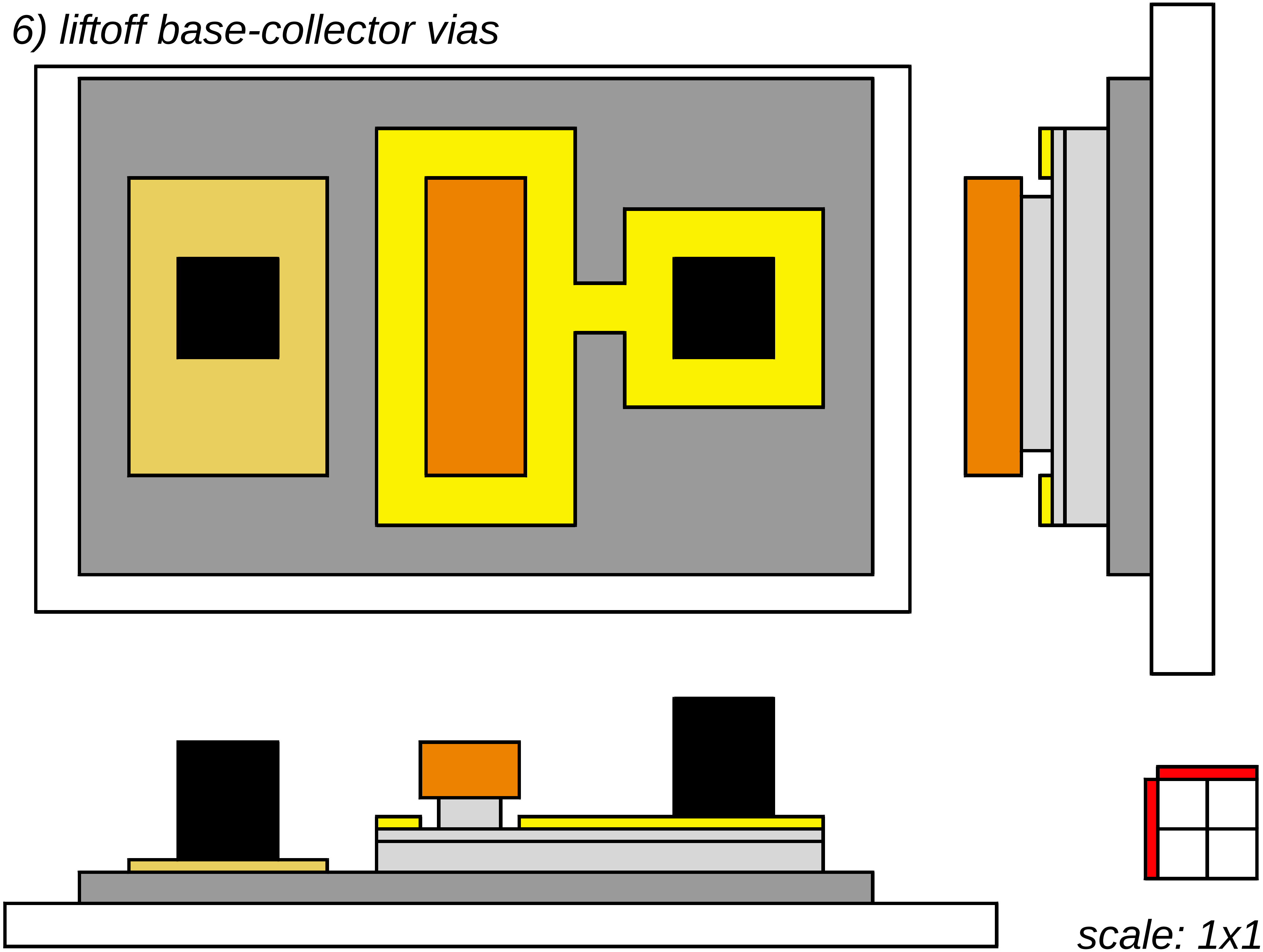
scale: 1x1 um

5) etch through base to subcollector, collector Ohmics



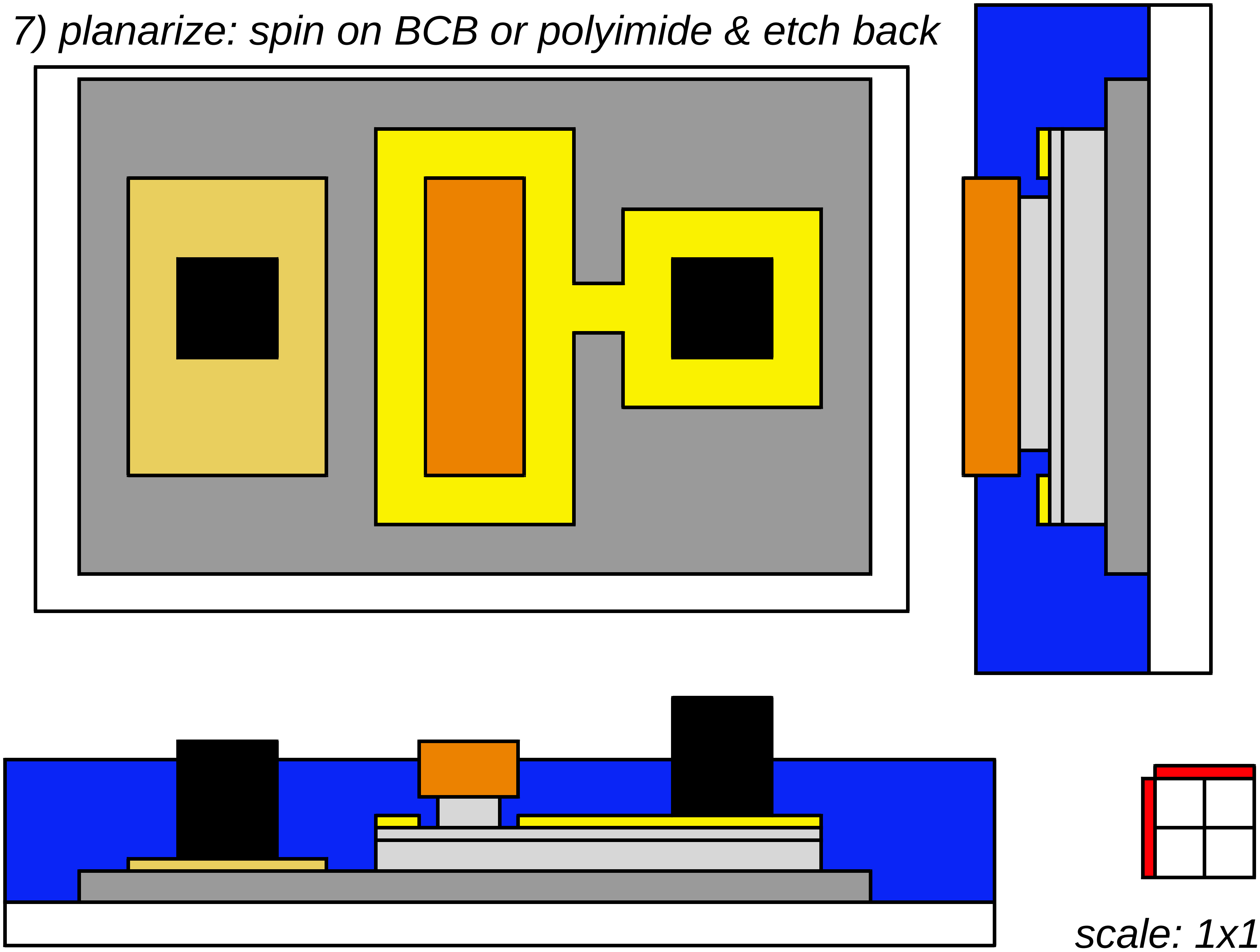
scale: 1x1 um

6) liftoff base-collector vias



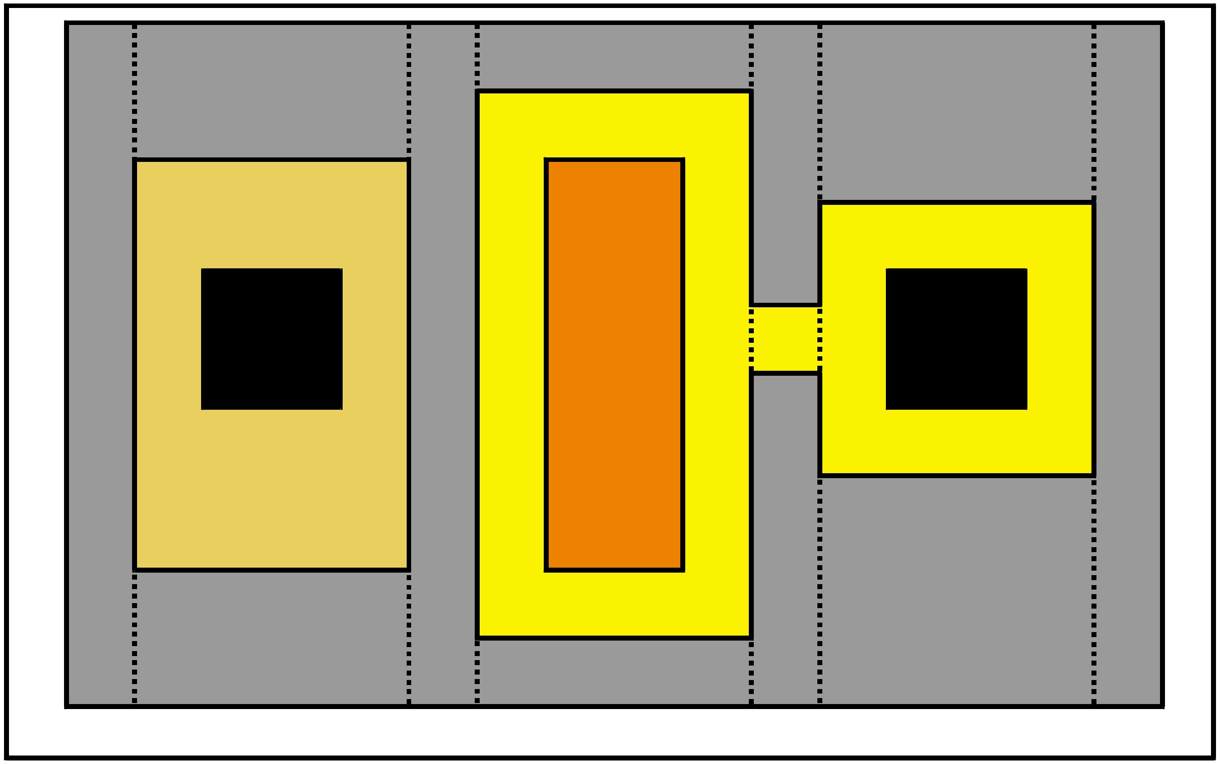
scale: 1x1 um

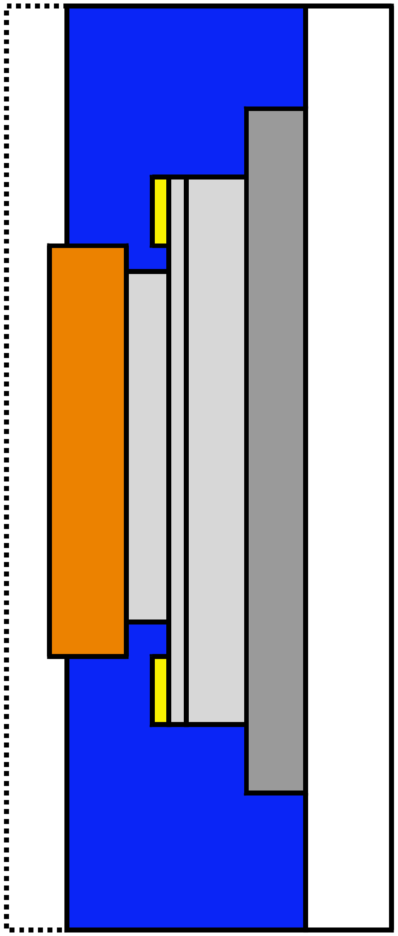
7) planarize: spin on BCB or polyimide & etch back

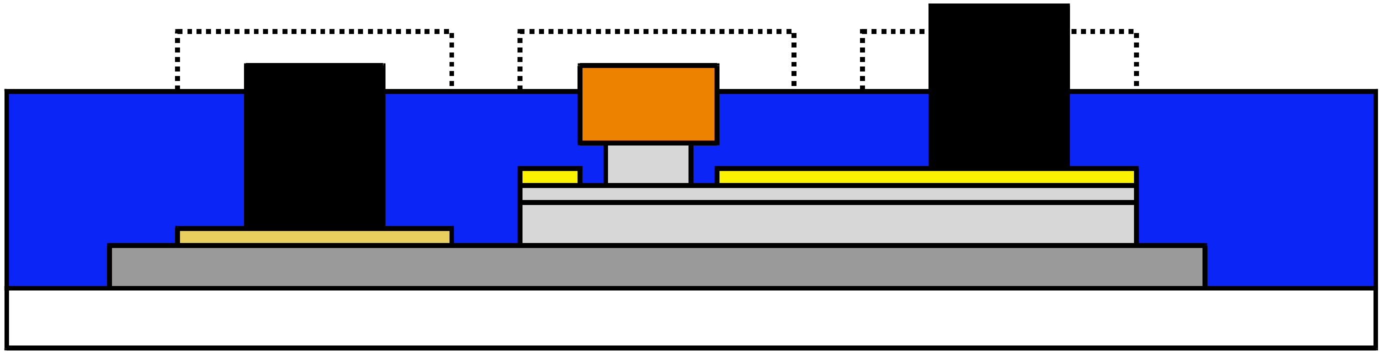


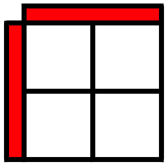
scale: 1x1 um

8) deposit interconnect metal









scale: 1x1 um

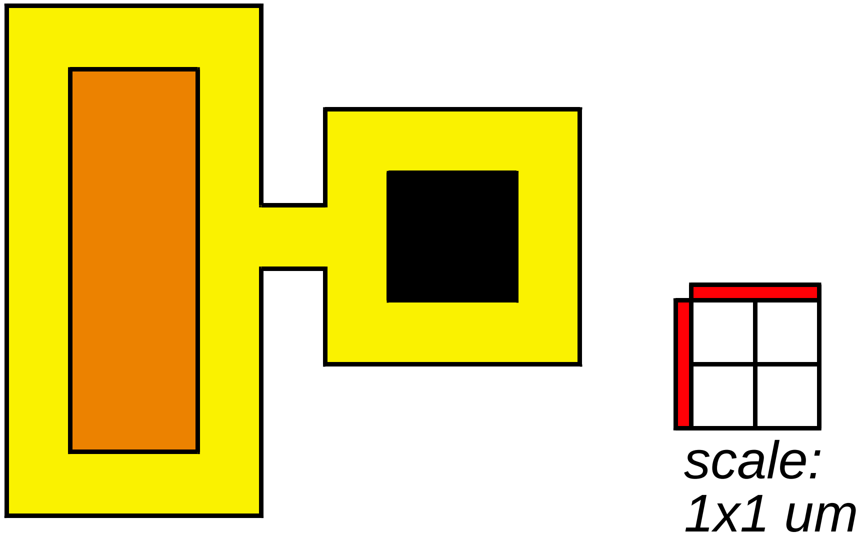
Problems with mesa process flow

Large Parasitic Collector Junction, Large Excess Ccb
resembles Si bipolar processes of 1960's !
parasitic collector junction lies under base contacts
base contacts must be nonzero size: nonzero resistivity
base contacts must be nonzero size: lithographic impact on yield

Self-aligned emitter-base process flow
base-emitter short-circuits
problems with wet-etch undercut control
problems with dry-etch reproducibility

Nonplanar process
loss of yield in back-end process

Problems with mesa process flow



emitter-base junction is 3 um^2
collector-base junction is 12 um^2

collector/emitter area ratio
even worse
in non-self-aligned processes...

While research-lab processes have moderate Ccb, processes aimed at high yield at >3000 HBTs have very large collector junctions

Ccb then the dominant circuit parasitic, regardless of impact on f_τ & f_{max}.

transistor key parasitics and model

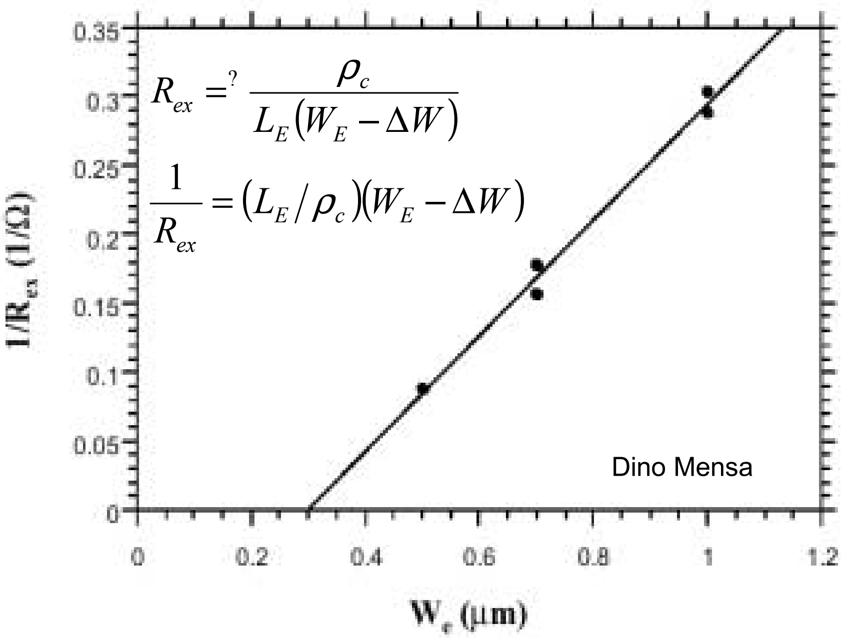
Emitter Resistance

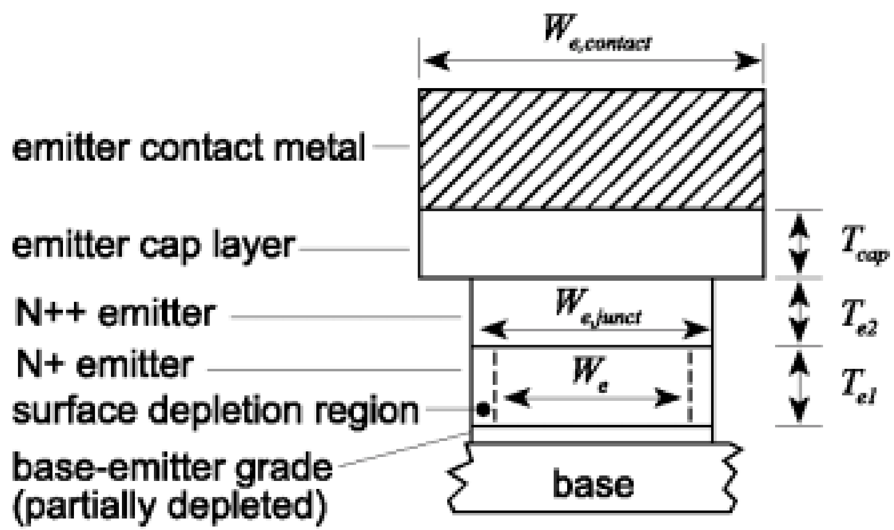
$$\text{Emitter resistance : one limiting factor in scaling for speed}$$

$$\text{high speed devices : high } J \rightarrow \text{low } \left(C_{cb}/I_c\right)$$

$$\text{but high } J \rightarrow \text{excessive } \left(I_E R_{ex}\right) \text{ voltage drop}$$

evidence of edge depletion or damage

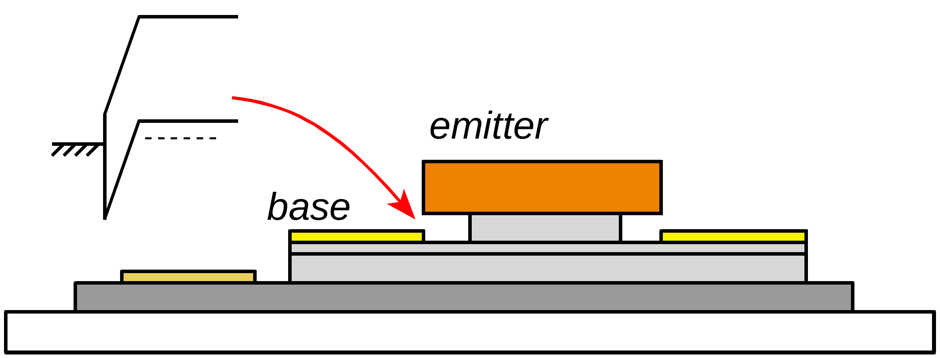




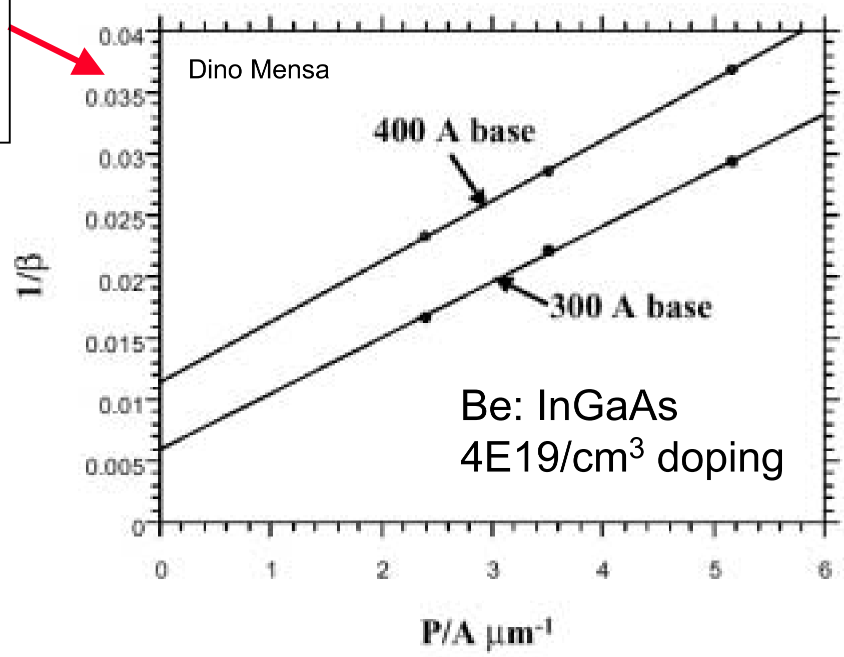
Current Gain: surface leakage

Surface Conduction:
InGaAs has low surface recombination velocity.
InGaAs has surface pinning near conduction band.
→ weak surface inversion layer on base, surface conduction to base contact
Problem aggravated by InP emitter, as this also pins near conduction band

$$\frac{1}{\beta}=\frac{I_b}{I_c}=\frac{I_{surface}}{I_c}+\frac{I_{bulk}}{I_c}$$
$$=\frac{P_E(k_1 q n_{po})}{A_E(q n_{po} D_n / W_b)}+\frac{1}{\beta_{bulk}}$$



evidence of surface conduction



Current Gain: Auger recombination

Carbon base doping : above 10^{20} / cm^2 feasible

Bulk recombination dominated by Auger

$$\tau_{\mathrm{Auger}} \propto 1/N_A^2$$

Since $\tau_{\mathrm{base}} \propto 1/T_B^2$ ..

$$\beta \propto 1/(N_A T_B)^2 \propto 1/\rho_{sheet}^2$$

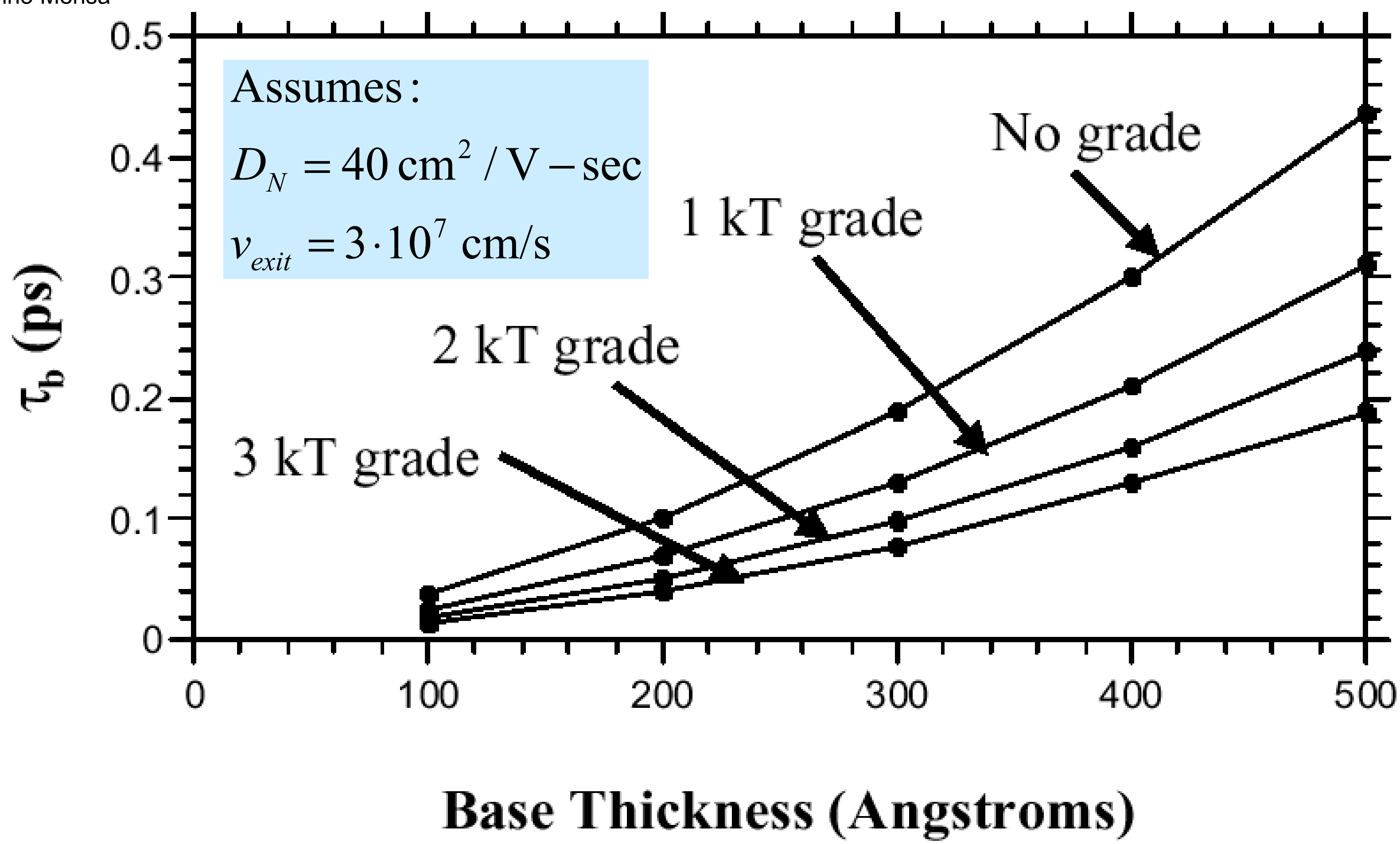
This constrains ρ_{sheet} reduction through high base doping

But, high base doping + thin base

$\Rightarrow$ low base contact resistivity, low transit time

Base Transit Time

Dino Mensa



$$\tau_b = W_b L_g / D_n - \left(L_g^2 / D_n - L_g / v_{sat}\right)\left(1 - e^{-W_b/L_g}\right)$$

where L_g is the grading length:

$$L_g = W_b \left(kT / \Delta E_g\right)$$

Drift-diffusion model correct if

$\tau_b >> \tau_m \approx D_n m^* / kT \approx 35$ fs

Base Bandgap vs. Doping Grading

Objective : introduce a 52 meV potential drop across base.

Case 1 : base bandgap grading.

Vary In : Ga ratio : $In_{0.455}Ga_{0.545}As \leftrightarrow In_{0.53}Ga_{0.47}As$ (strained)

Case 2 : base doping grading, non - degenerate base

Base doping near emitter side constrained by growth / reliability

Reduce doping at collector side of base by $e^{-2} : 1 = 0.12 : 1$

$\Rightarrow$ greatly increased base sheet resistance

$\Rightarrow$ Contact resistance increased : contacts land somewhere in middle of base

Case 3 : base doping grading, degenerate base

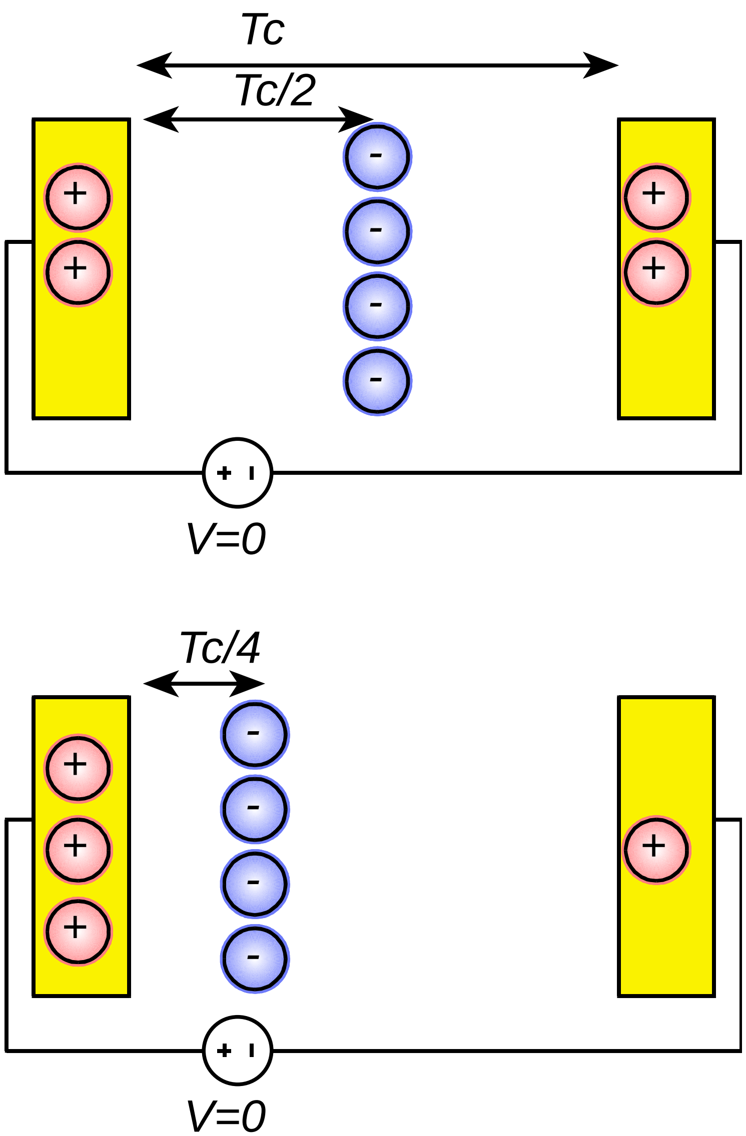
Degenerate doping statistics : small doping change induces big field

With heavy doping, Auger - induced β collapse sets maximum $\int_0^{T_b} p(x)dx$

Can introduce built - in field without degrading sheet resistance.

Collector Transit Time

T. Ishibashi

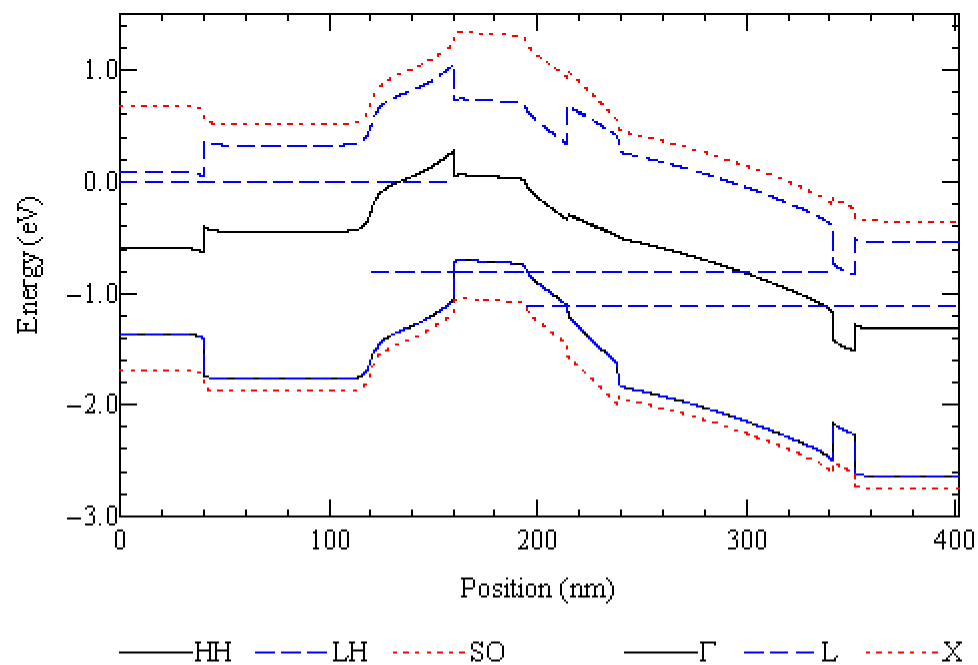


From elementary electrostatics (refer to sketch)

$$\tau_c = \int_0^{T_C} \frac{(1 - x/T_c)}{v(x)} dx \equiv \frac{T_c}{2v_{eff}}$$

τ_c is more sensitive to velocity near base.

Fortuitous, as initial velocity is high,
then decreases due to Γ - L scattering.



Collector Transit Time

...from best fit to RF data

Velocities in InGaAs collectors

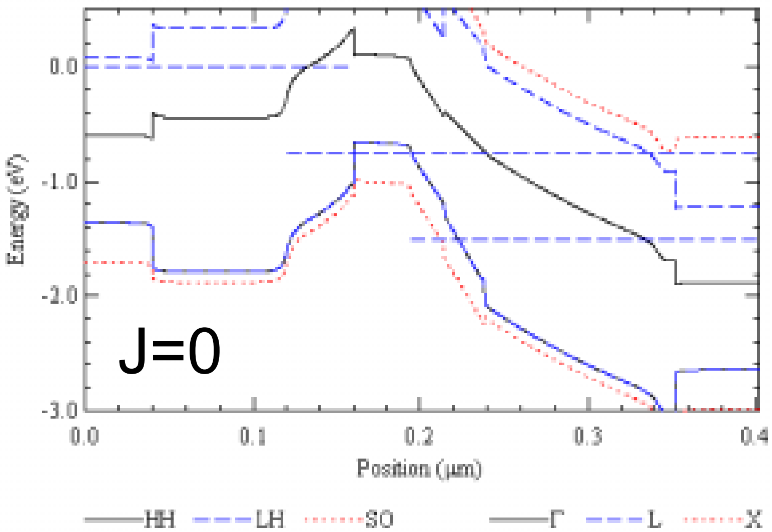
$3\text{-}5 \cdot 10^7$ cm/s for ~ 2000 Å layers

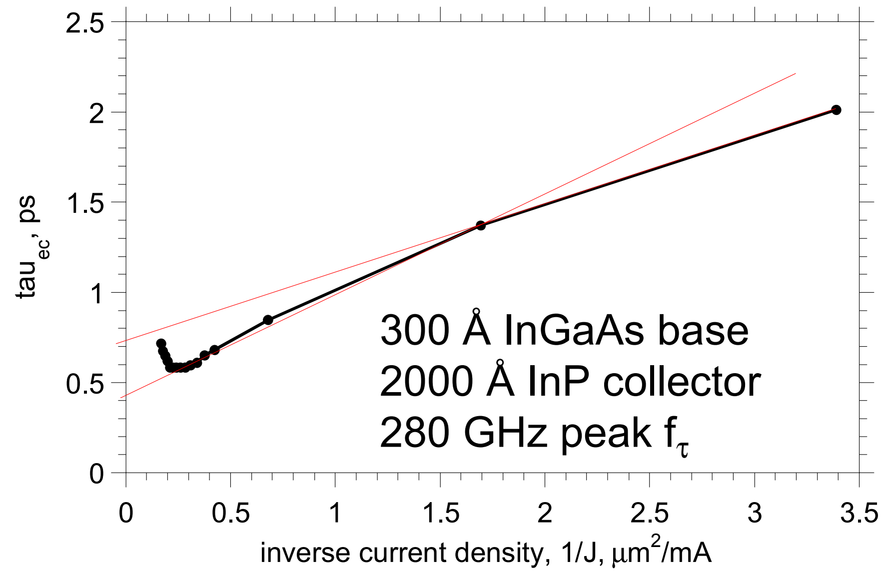
Velocities in InP collectors

also $3\text{-}5 \cdot 10^7$ cm/s for ~ 2000 Å layers

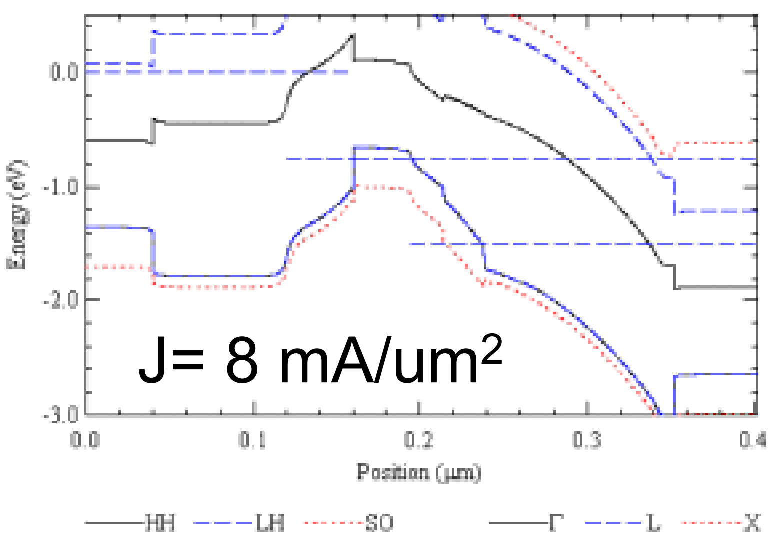
Current-induced Collector Velocity Overshoot (?)

Mattias Dahlstrom





Effect predicted by Ishibashi

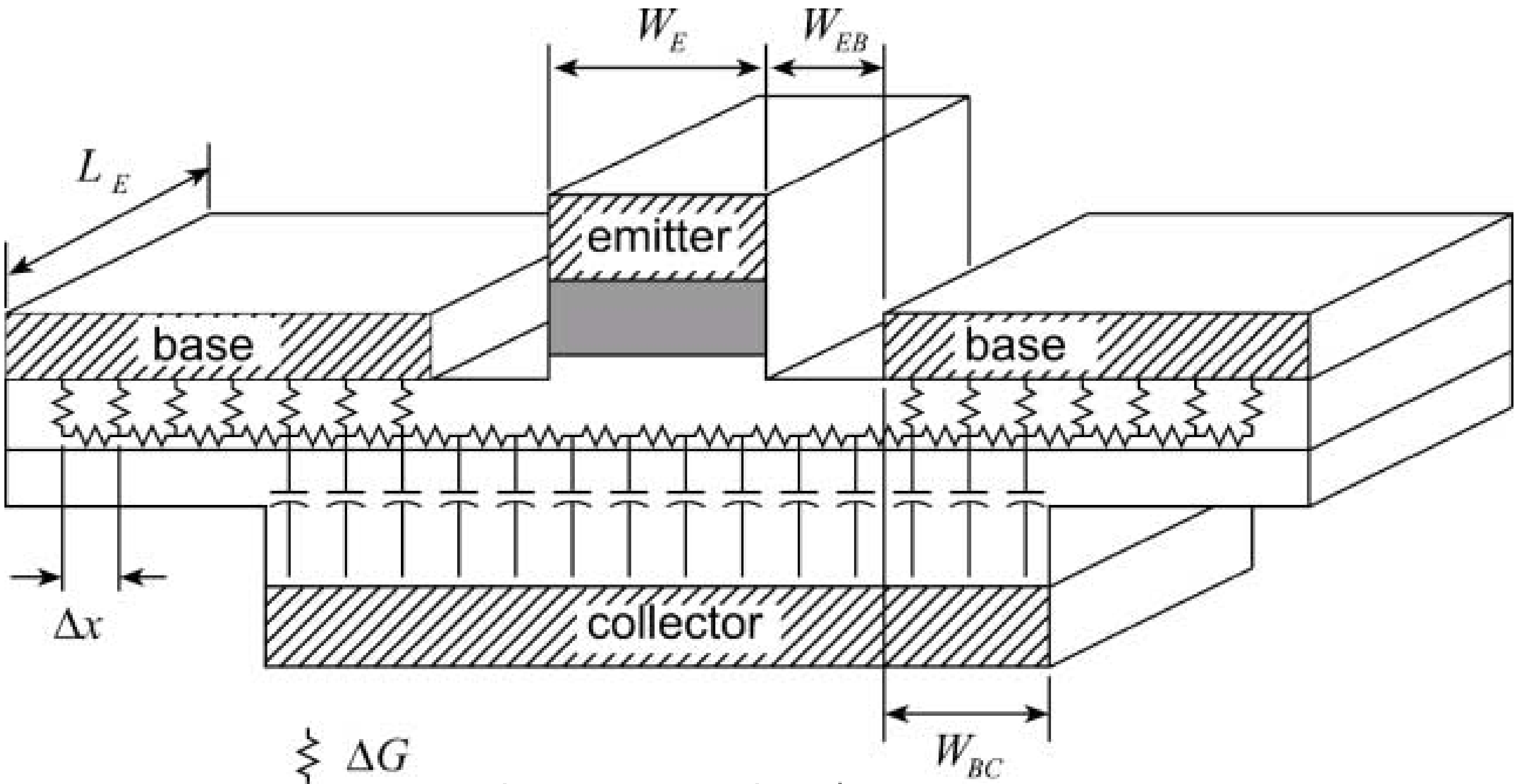


τ_{ec} data *does* show predicted trend.

BUT : τ_{ec} variation may also be due to modulation in emitter ideality factor with bias current ($1/g_m$ often does not vary as $R_{ex} + kT/qI_E$).

C_{je} also varies with bias.

Base-Collector Distributed Model: exact



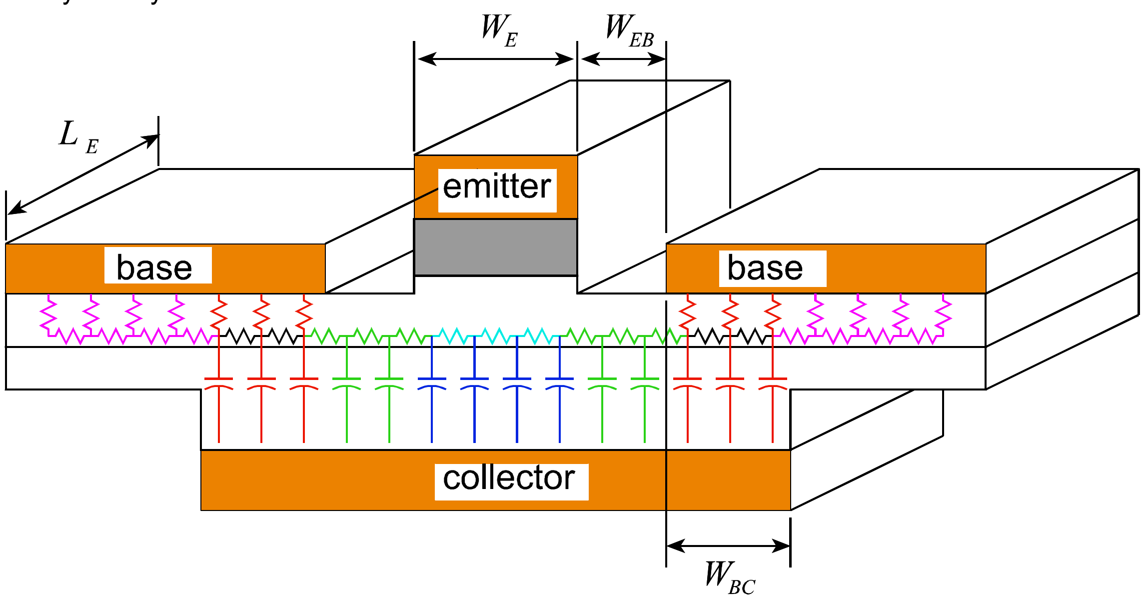
$$\Delta G = L_e \Delta x / \rho_c; \quad \Delta C = \epsilon L_e \Delta x / T_c$$

$$\Delta R = \rho_s \Delta x / L_e$$

This "mesh model" can be entered into a microwave circuit simulator (e.g. Agilent ADS) to predict f_{max} , etc.

Components of Rbb and Ccb

Pulfrey / Vaidyanathan



$$R_{horiz} = \rho_s W_{bc} / 2L_E$$

$$R_{cont} = \sqrt{\rho_s \rho_v} / 2L_e$$

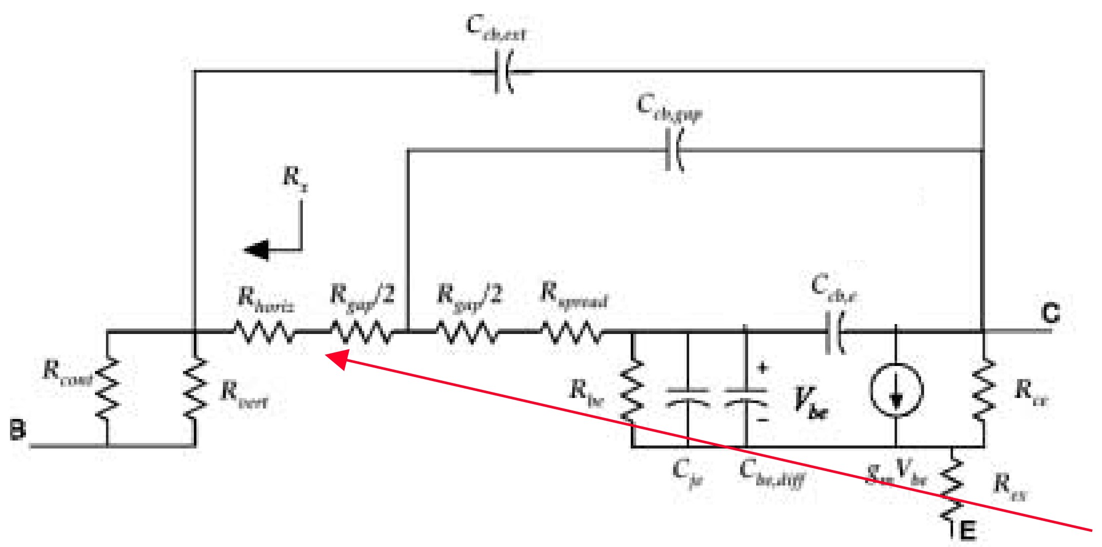
$$R_{gap} = \rho_s W_{eb} / 2L_e$$

$$R_{spread} = \rho_s W_e / 12 L_e.$$

$$C_{cb,ext} = 2\epsilon L_e W_{cb} / T_c$$

$$C_{cb,gap} = 2\epsilon L_e W_{eb} / T_c$$

$$C_{cb,e} = \varepsilon L_e W_e / T_c$$



$$R_x = R_{horiz} + R_{vert} \| R_{cont} = R_{cont}!$$

Miguel Urteaga

Components of base ~~spreading~~ resistance

$$R_{bb} = R_{cont} + R_{gap} + R_{spread}$$

$$R_{cont} = \sqrt{\rho_s \rho_v}/2L_e$$

$$R_{gap} = \rho_s W_{eb}/2L_e$$

$$R_{spread} = \rho_s W_e/12L_e.$$

With submicron emitters

(or with ~ 1E20 base doping)

R_{bb} is dominated by $R_{contact}$ and R_{gap}.

Given that emitter area

$A_E = L_E W_E$ is fixed:

decreased emitter width W_E

results in increased emitter length L_E.

$\Rightarrow$ Low R_{bb} is obtained with narrow

emitters, even with negligible R_{spread}.

Typical base parameters

$4\cdot 10^{19}\,/\mathrm{cm}^3$ Be - doped InGaAs base, 52 meV grading, 400 A thickness

$\rho_\mathrm{s} = 750$ Ohms/square , $\rho_\mathrm{c} = 100$ Ohm - $\mu\mathrm{m}^2$, $\tau_b \approx 170$ fs, $D_n \approx 40\ \mathrm{cm}^2/\mathrm{s}$

$7\cdot 10^{19}\,/\mathrm{cm}^3$ C - doped InGaAs base, 52 meV (doping) grading, 300 A thickness

$\rho_\mathrm{s} = 700$ Ohms/square , $\rho_\mathrm{c} < 10$ Ohm - $\mu\mathrm{m}^2$, $\tau_b \approx 100$ fs, $D_n \approx 40\ \mathrm{cm}^2/\mathrm{s}$

$8\cdot 10^{19}\,/\mathrm{cm}^3$ C - doped GaAsSb base, ?? meV grading, 250 A thickness

$\rho_\mathrm{s} = 1000$ Ohms/square , $\rho_\mathrm{c} \approx 20$ Ohm - $\mu\mathrm{m}^2$, $\tau_b \approx 150-200$ fs, $D_n \approx 20\ \mathrm{cm}^2/\mathrm{s}$

(Dvorak)

Pulfrey / Vaidyanathan fmax model

Pulfrey / Vaidyanathan

$$f_{max} = \sqrt{\frac{f'_\tau}{8\pi\tau_{cb}}},$$

$$\frac{1}{2\pi f'_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}\,(C_{je} + C_{cb}),$$

$$\begin{aligned}\tau_{cb} &= C_{cb,e}\,(R_{cont} + R_{gap} + R_{spread}) \\ &+ C_{cb,gap}\,(R_{cont} + R_{gap}/2) \\ &+ (R_{cont} \| R_{vert})\, C_{cb,ext}\end{aligned}$$

Note that the external capacitance $C_{cb,ext}$ is charged through a relatively low resistance, less than R_{vert}.

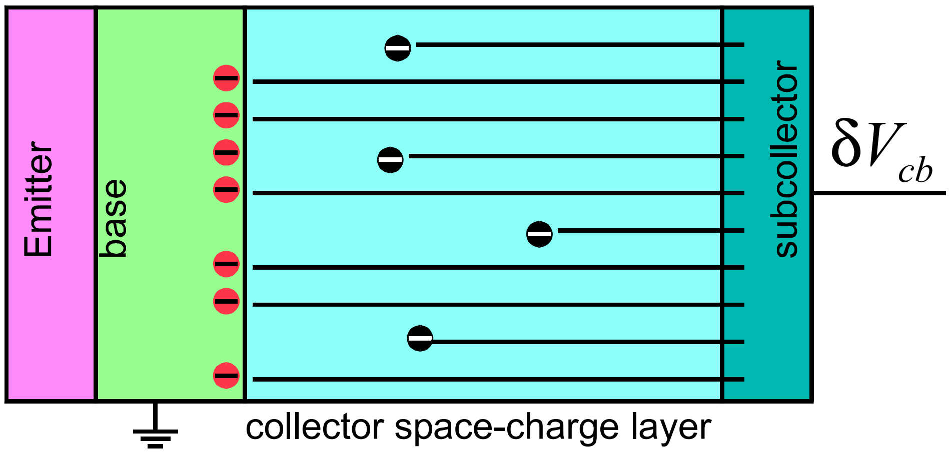
$$C_{cb,ext}\left(R_{cont} \| R_{vert}\right) < C_{cb,ext} R_{vert} = \frac{\varepsilon}{T_c}\frac{1}{\rho_{contact}}$$

...the associated charging time is relatively small

$C_{cb,ext}$ has moderate effect upon $f_{\max}$, but big impact upon digital and analog speed

C_{cb} Cancellation by Collector Space-Charge

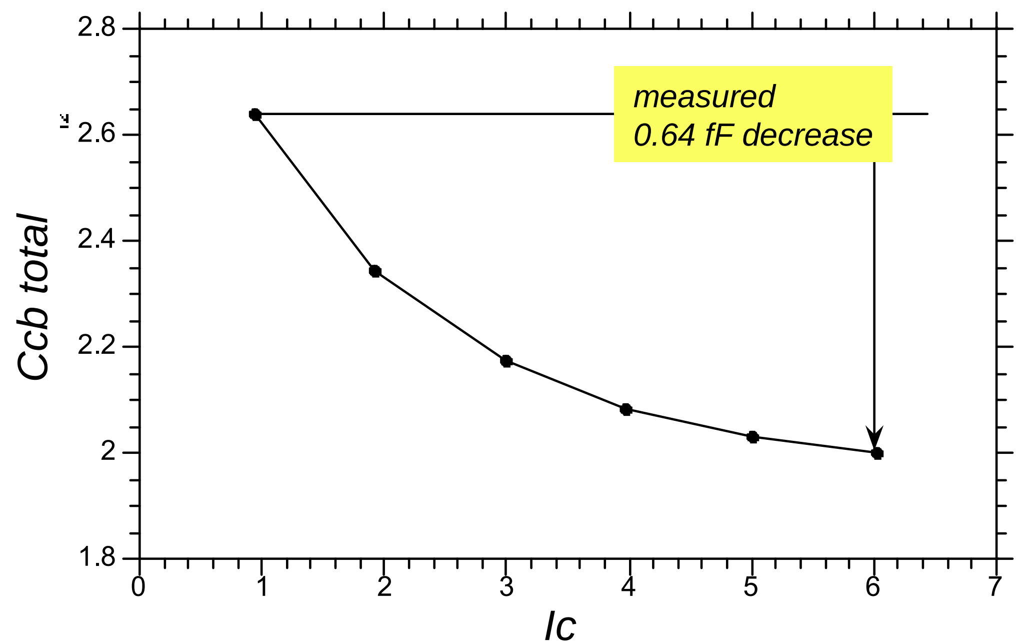
Moll & Camnitz, Betser and Ritter



$$\frac{\partial Q_{base}}{\partial V_{cb}} = \frac{\varepsilon A}{T_c} - \frac{\partial}{\partial V_{cb}}\left(\frac{I_c T_c}{2 v_{sat}}\right)$$

$$\Rightarrow C_{cb} = \frac{\varepsilon A}{T_c} - I_c \frac{\partial \tau_c}{\partial V_{cb}}$$

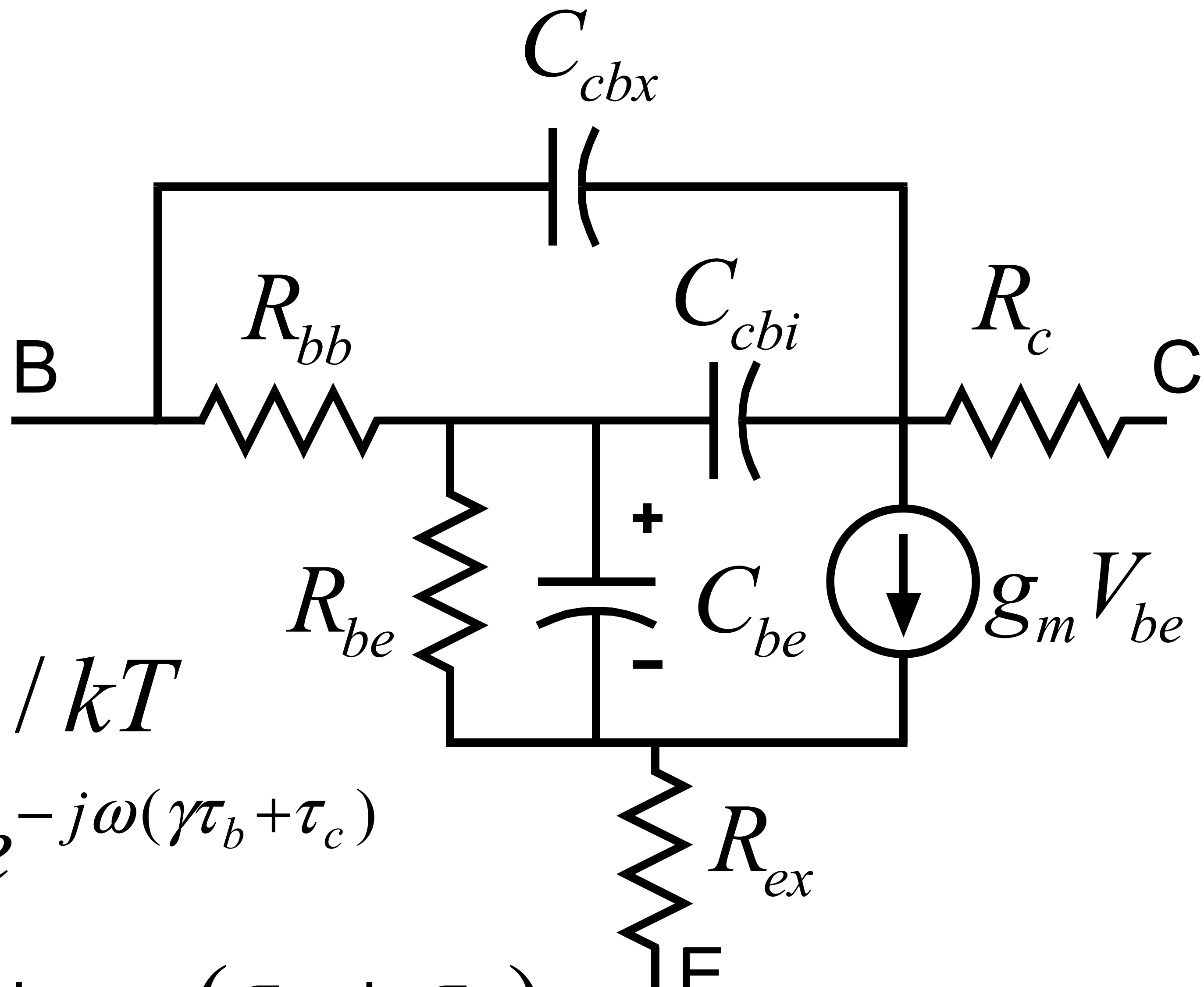
Collector space charge screens field,
Increasing voltage decreases velocity,
→ modulates collector space-charge
→ offsets modulation of base charge
→ Ccb is reduced



Even if you don't care about fmax, the effect can confuse HBT model extraction

equivalent circuit model

Transistor Hybrid-Pi equivalent circuit model



$$g_{m0} = qI_E / kT$$

$$g_m = g_{m0} e^{-j\omega(\gamma\tau_b + \tau_c)}$$

$$C_{be} = C_{je} + g_m(\tau_b + \tau_c)$$

Comments regarding the Hybrid-Pi model

The common - base (T) model directly models frequency - dependent transport

The hybrid - pi model results from a fit to the T to first order in ω.

The capacitance $C_{be,diff}$ models the effect of $(\tau_b + \tau_c)$ on input impedance

The g_m generator nevertheless also requires an associated $\sim (0.2 \cdot \tau_b + \tau_c)$ delay (important in fast IC design)

$R_{bb} C_{cbi}$ and C_{cbx} represent fits to the distributed RC base - collector network

Collector field-screening (Kirk Effect)

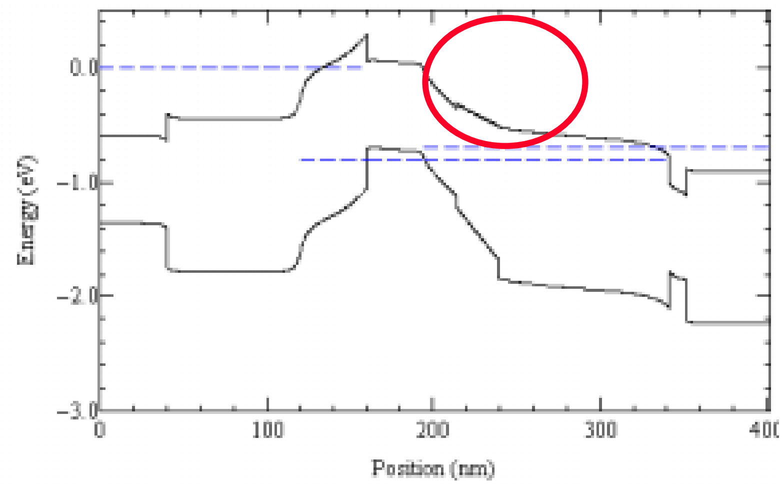
Kirk effect in DHBTs: not base pushout, but current-blocking

$$\frac{d^2\phi}{dx^2} = \frac{\rho}{\varepsilon} = \frac{qN_d - J/v}{\varepsilon}$$

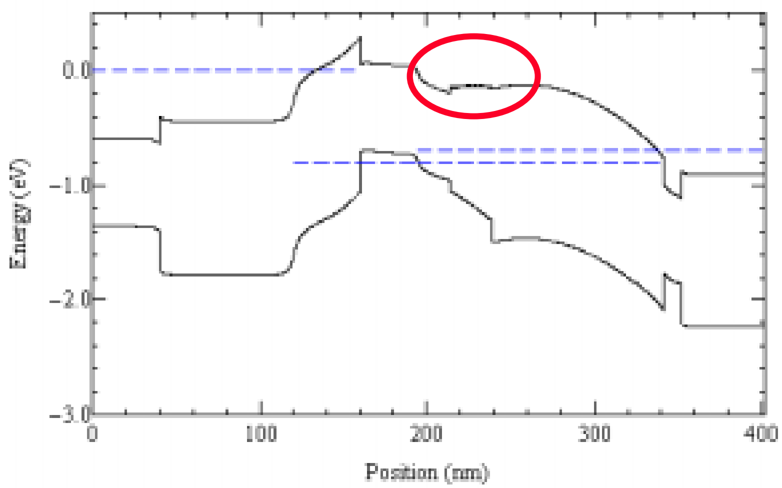
Bandbending under high J and low V_{ce} results in current blocking

$\Rightarrow$ decrease in β and f_τ

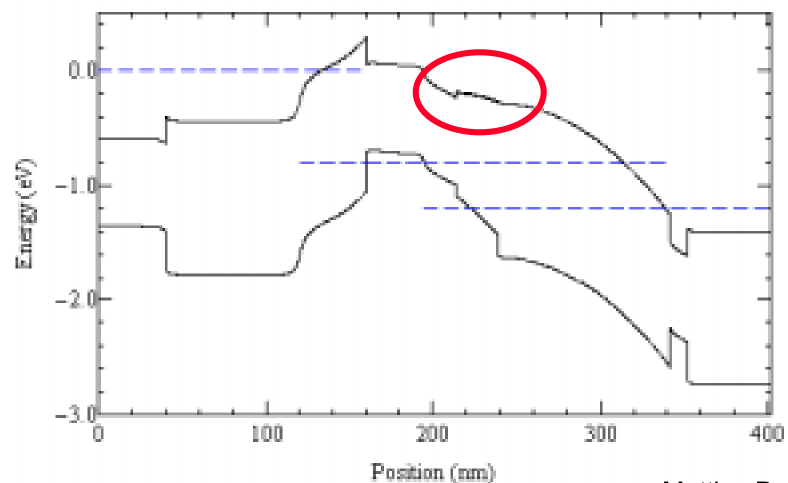
$V_{ce} = 0.7\text{ V}, J_e = 0\text{ kA/cm}^2, v_{sat,eff} = 4\cdot 10^7\text{ cm/s}$



$V_{ce} = 0.7\text{ V}, J_e = 1000\text{ kA/cm}^2, v_{sat,eff} = 4\cdot 10^7\text{ cm/s}$



$V_{ce} = 1.2\text{ V}, J_e = 1000\text{ kA/cm}^2, v_{sat,eff} = 4\cdot 10^7\text{ cm/s}$



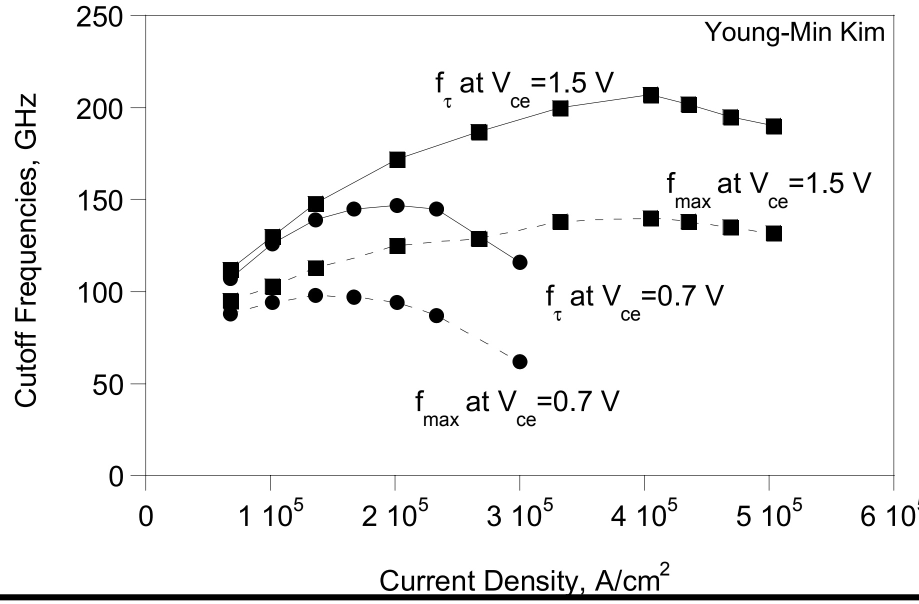
Mattias Dahlstrom

Kirk effect in DHBTs

Decrease in f_τ and $f_{\max}$ at lower J

Kirk-effect threshold increases with increased V_{ce}

$$J_{\max} = 2\varepsilon v_{sat}(V_{cb} + V_{cb,\min} + 2\phi)/T_c^2$$
$$\cong 2\varepsilon v_{sat}(V_{ce} + V_{ce,\min})/T_c^2$$

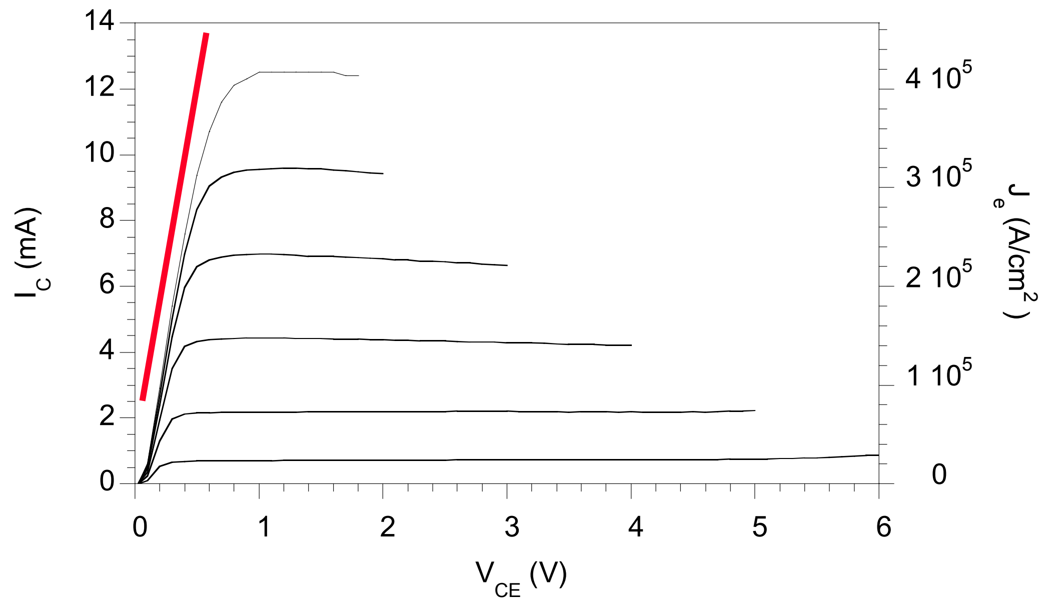


Increase in $V_{ce,sat}$ with increased J

$$\frac{dV_{ce}}{dI_c} = R_{\text{space-charge}} = \frac{T_c^2}{2\varepsilon v_{sat} A_{effective}}$$

where the effective collector current flux area is

$$A_{effective} \approx L_E (W_E + 2T_C)$$



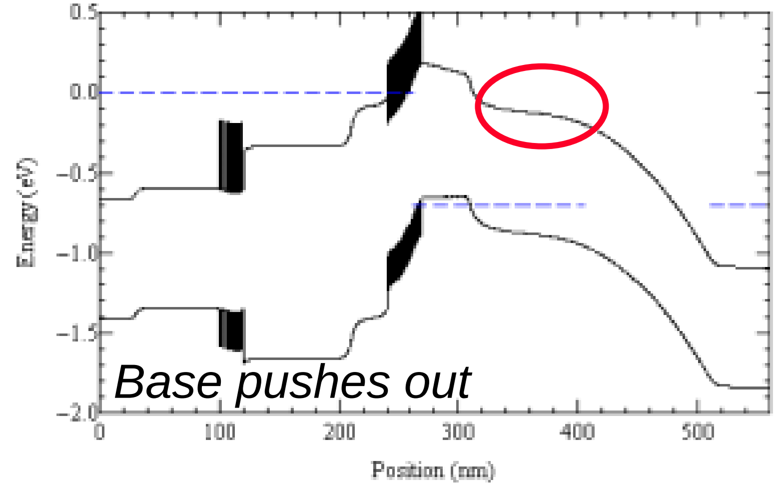
Kirk effect in SHBTs: base pushout, increased Ccb

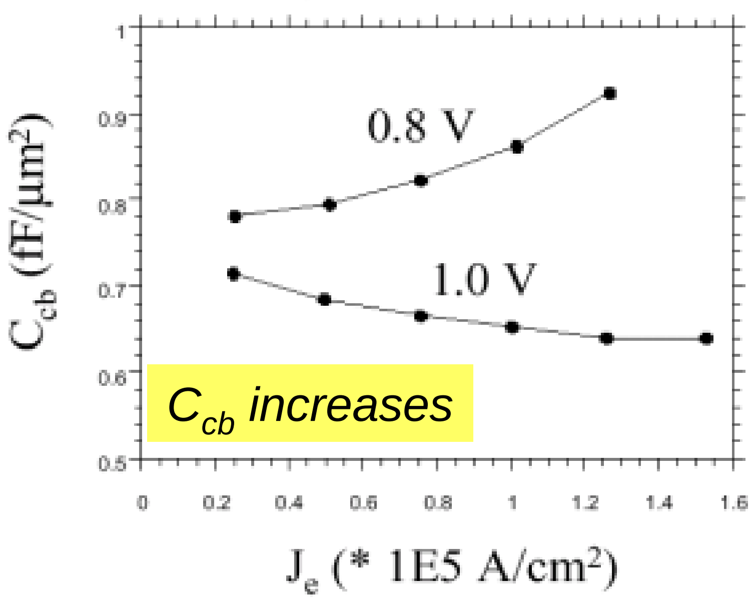
Base pushes out.

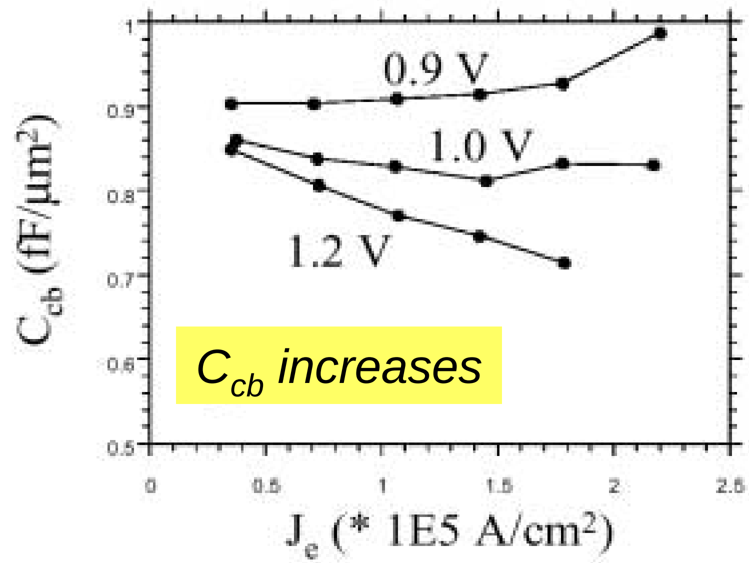
Holes compensate electrons

C_{cb} increases.

$V_{ce} = 0.7$ V, $J_e = 500$ kA/cm^2, $v_{sat,eff} = 3 \cdot 10^7$ cm/s







Kirk effect with Nonuniform Collector Electron Velocity

From transit time analysis,

$$\tau_c = \int_0^{T_C} \frac{(1 - x/T_c)}{v(x)} dx \equiv \frac{T_c}{2v_{eff}}$$

τ_c and v_{eff} are more sensitive to velocity near base.

Kirk effect with uniform collector velocity:

$$J_{max} = 2\varepsilon v_{sat}(V_{cb} + V_{cb,min} + 2\phi)/T_c^2$$

$$\cong 2\varepsilon v_{sat}(V_{ce} + V_{ce,min})/T_c^2$$

Kirk effect with NONuniform collector velocity:

$$J_{max} = 2\varepsilon v_{eff}(V_{cb} + V_{cb,min} + 2\phi)/T_c^2$$

$$\cong 2\varepsilon v_{eff}(V_{ce} + V_{ce,min})/T_c^2$$

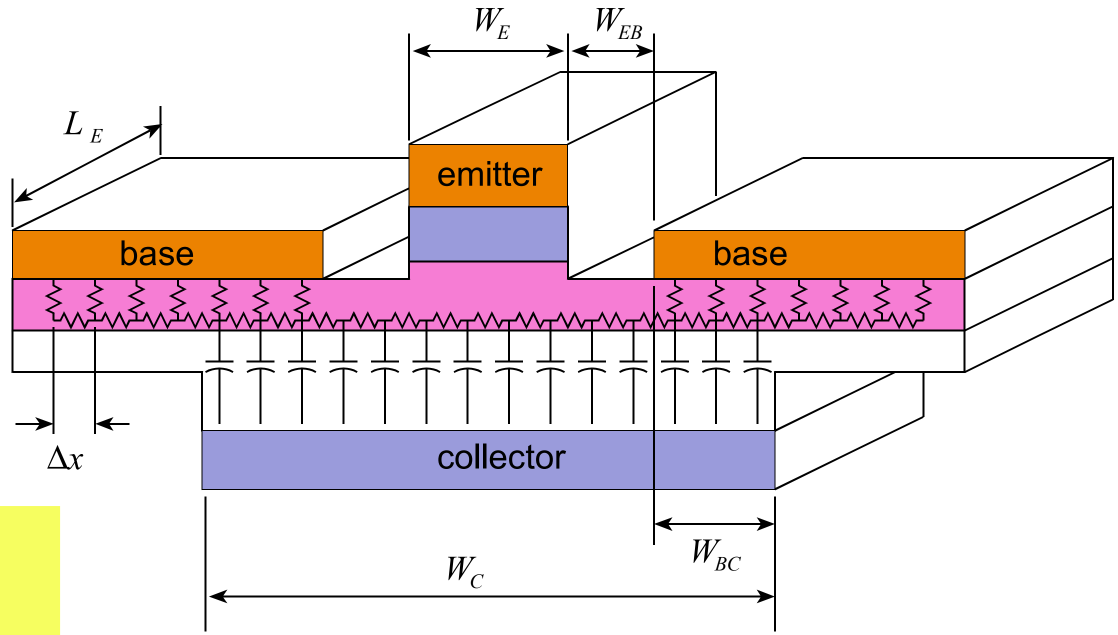
Nonuniform collector electron velocity doesn't profoundly change Kirk effect…

transistor scaling theory

Rodwell

HBT scaling: layer thicknesses

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ's



reduce T_b by $\sqrt{2}$:1
*$\rightarrow \tau_b$ **improved** 2:1*

reduce T_c by 2:1
*$\rightarrow \tau_c$ **improved** 2:1*

*note that Ccb has been **doubled***
..we had wanted it 2:1 smaller

$$\tau_b \cong T_b^2 / 2D_n$$

$$\tau_b \cong T_c \;/ 2v_{sat}$$

$$\text{Assume } W_C \sim W_E$$

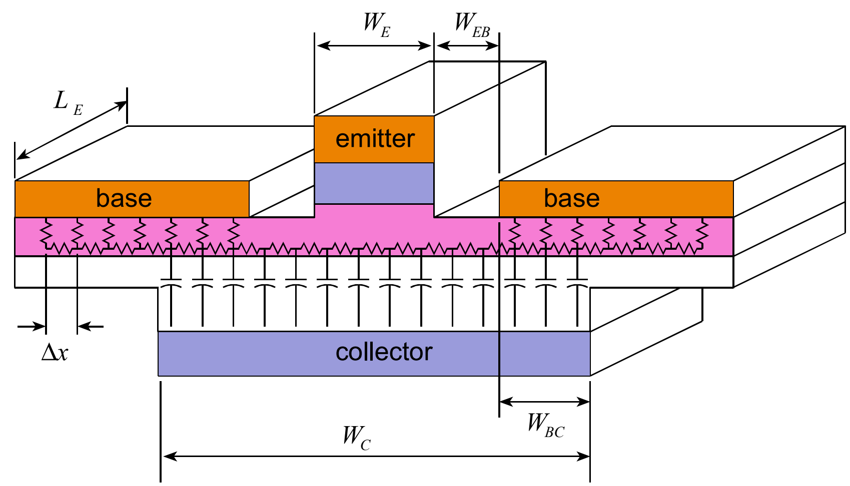
HBT scaling: lithographic dimensions

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ's

Base Resistance R_{bb} must remain constant
$\rightarrow L_e$ must remain ~ constant

$$R_{bb} = R_{gap} + R_{spread} + R_{contact}$$
$$\cong R_{contact}$$
$$= \sqrt{\rho_{sheet}\rho_{c,vertical}} / 2L_E$$

*Ccb/Area has been **doubled***
..we had wanted it 2:1 smaller
…must make area=L_eW_e 4:1 smaller
$\rightarrow$ must make W_e & W_c 4:1 smaller



reduce collector width 4:1
reduce emitter width 4:1
keep emitter length constant

$$\text{Assume } W_C \sim W_E$$

HBT scaling: emitter resistivity, current density

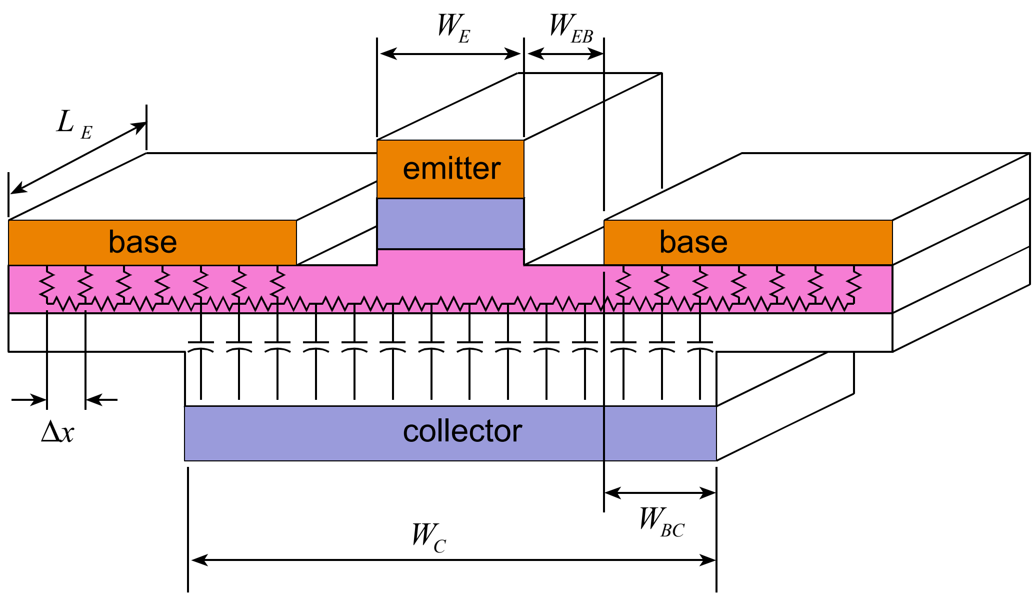
2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ's

Rodwell

Emitter Resistance R_{ex} must remain constant
but emitter area=$L_e W_e$ is 4:1 smaller
resistance per unit area must be 4:1 smaller

Assume $W_C \sim W_E$

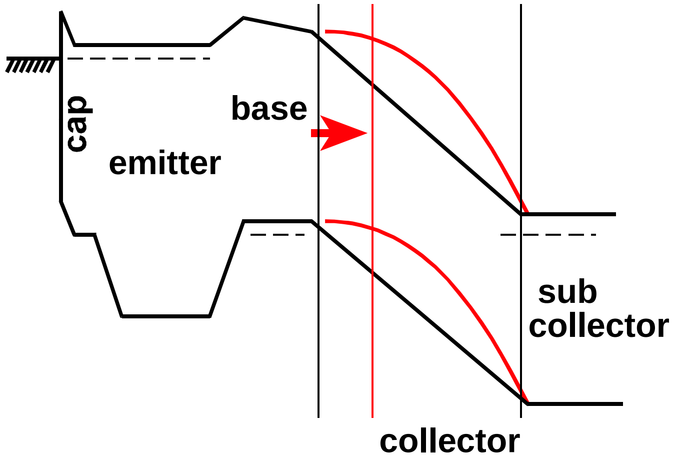
Collector current must remain constant
but emitter area=$L_e W_e$ is 4:1 smaller
and collector area=$L_c W_c$ is 4:1 smaller
current density must be 4:1 larger



increase current density 4:1
reduce emitter resistivity 4:1

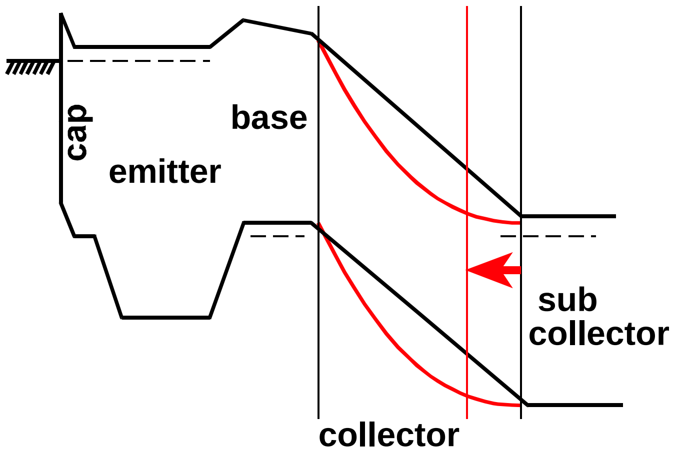
Rodwell

Scaling Laws, Collector Current Density, C_{cb} charging time



Collector Field Collapse (Kirk Effect)

$$V_{cb} + \phi > +(J / v_{sat} - qN_d)(T_c^2 / 2\varepsilon)$$



Collector Depletion Layer Collapse

$$V_{cb,\min} + \phi > +(qN_d)(T_c^2 / 2\varepsilon)$$

$$\Rightarrow \quad J_{\max} = 2\varepsilon v_{sat}(V_{cb} + V_{cb,\min} + 2\phi) / T_c^2$$

Note that $V_{be} \cong \phi$, hence $(V_{cb} + \phi) \cong V_{ce}$

$$C_{cb}\Delta V_{LOGIC} / I_C = (\varepsilon A_{\text{collector}} / T_c)(\Delta V_{LOGIC} / I_C) = \frac{\Delta V_{LOGIC}}{(V_{CE} + V_{CE,\min})}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2v_{sat}}\right)$$

Collector capacitance charging time is reduced by ***thinning the collector*** *while increasing current*

Scaling Laws for fast HBTs

for x 2 improvement of *all* parasitics:
f_t, f_{max}, logic speed…
base $\sqrt{2}$: 1 thinner
collector 2:1 thinner
emitter, collector junctions 4:1 narrower
current density 4:1 higher
emitter Ohmic 4:1 less resistive

Challenges with Scaling:

Collector
mesa HBT: collector under base Ohmics.
Base Ohmics must be one transfer length
sets minimum size for collector

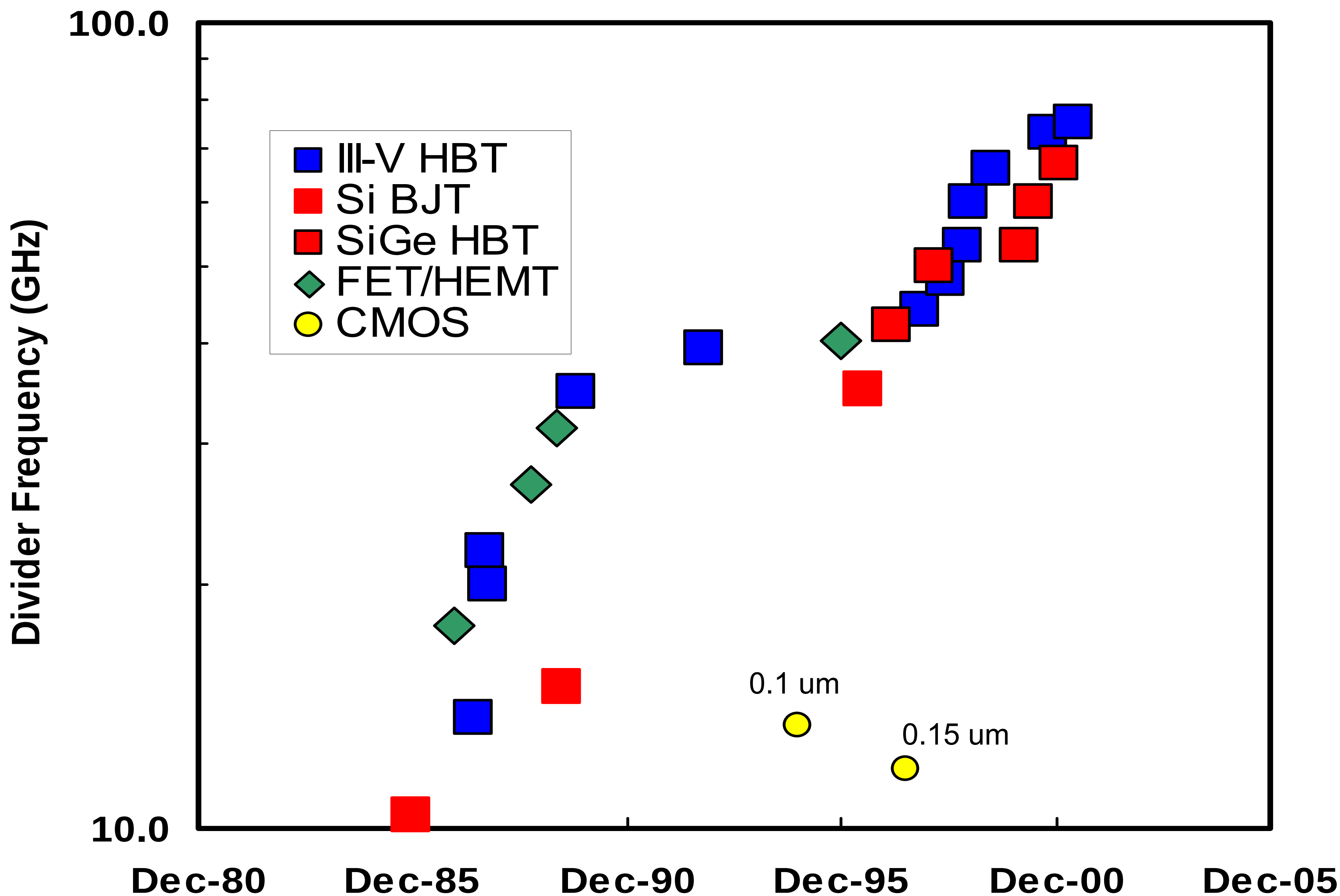
Emitter Ohmic:
hard to improve…how ?

Current Density:
dissipation, reliability

Loss of breakdown
avalanche Vbr never less than collector Egap
(1.12 V for Si, 1.4 V for InP)
….sufficient for logic, insufficient for power

digital circuit speed

Logic Speed: III-V vs. Silicon



Benchmark: master-slave flip-flop configured as 2:1 **static** frequency divider

Source: M Sokolich, HRL, Rodwell, UCSB

75 GHz HBT master-slave latch connected as ***Static*** frequency divider

UCSB

Thomas Mathew
Michelle Lee
Hwe-Jong Kim

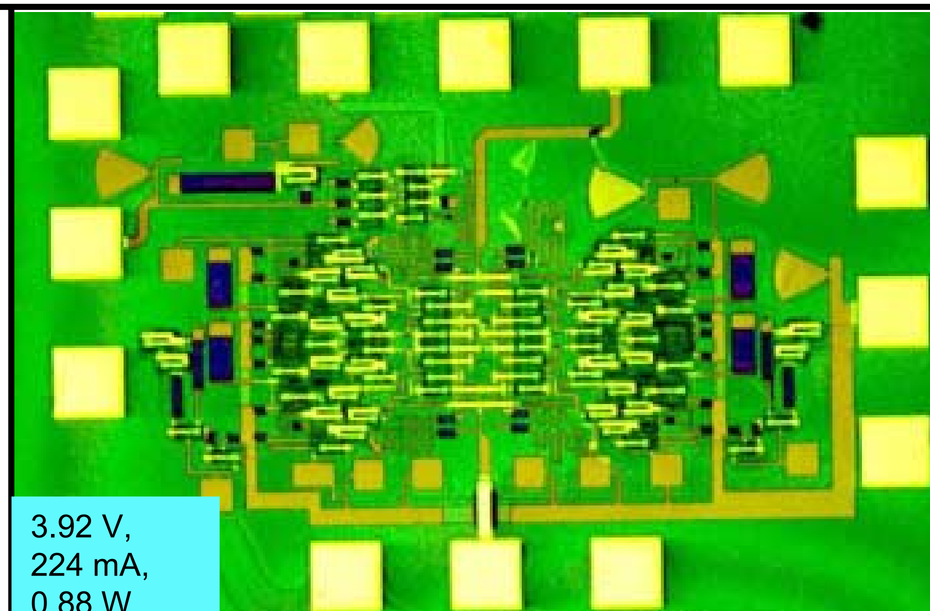
technology:

400 Å base, 2000 Å collector HBT
0.7 um mask (0.6 um junction) x 12 um emitters
1.5 um mask (1.4 um junction) x 14 um collectors

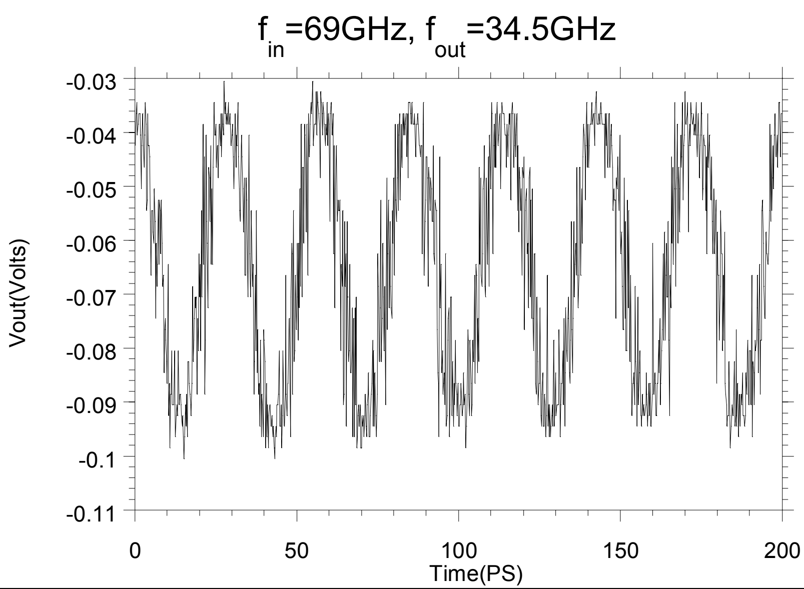
transistor performance:

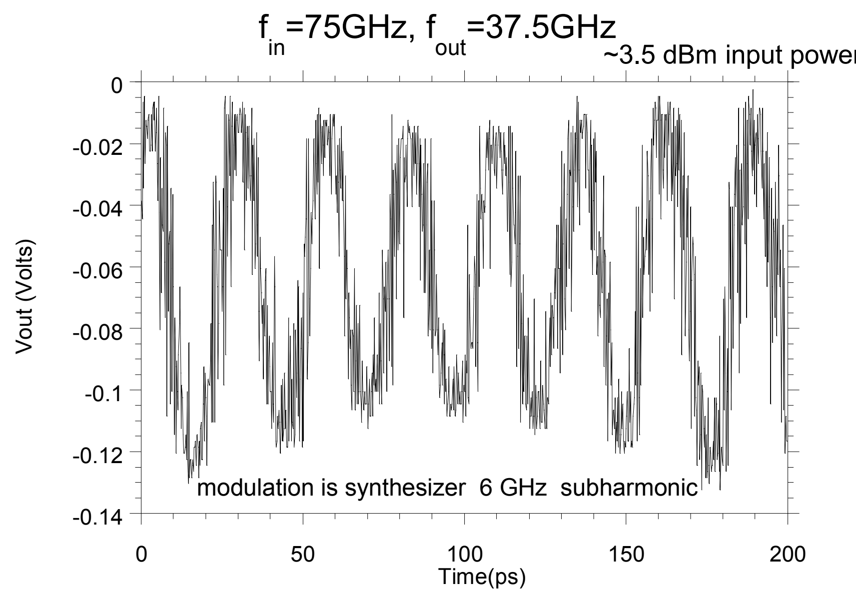
1.8×10^5 A/cm^2 operation, 180 GHz ft, 260 GHz fmax
collector/ emitter junction area ratio: 2.7:1 (low)
Ccb/Ic: 0.9 ps/V
Rex*I=54 mV

simulations: 95 GHz clock rate in SPICE



3.92 V,
224 mA,
0.88 W





What do we need for fast logic ?

Gate Delay Determined by:

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C}\right)\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Depletion capacitance charging through the base resistance

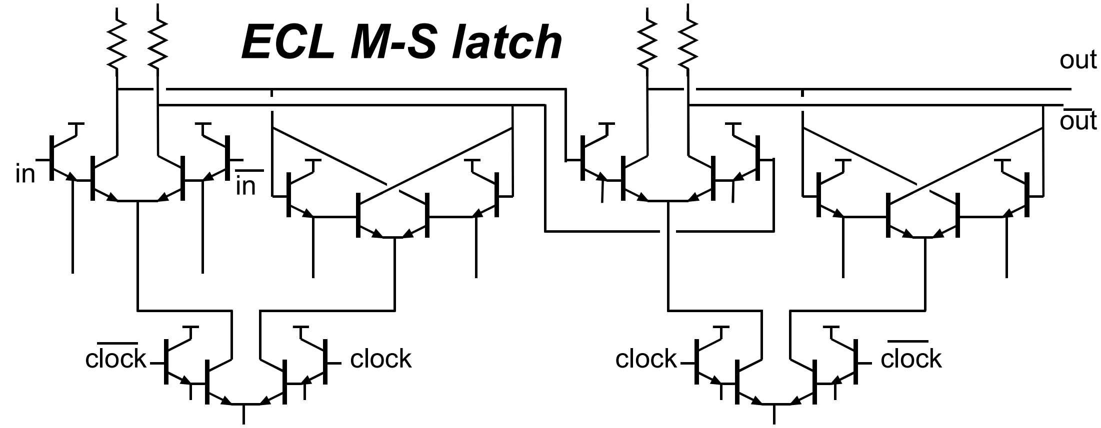
$$R_{\text{bb}}\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Supplying base + collector stored charge through the base resistance

$$R_{\text{bb}}\left(\tau_b+\tau_c\right)\left(\frac{I_C}{\Delta V_{LOGIC}}\right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 6\left(\frac{kT}{q}+R_{ex}I_c\right)$$



Neither f_τ nor f_{max} predicts digital speed

$C_{cb}\Delta V_{logic}/I_c$ is very important

→ ***collector capacitance reduction is critical***

→ ***increased III-V current density is critical***

R_{ex} must be very low for low ΔV_{logic} at high J_c

InP: R_{bb}, $(\tau_b+\tau_c)$, are already low, must remain so

Yoram Betser, Raja Pullela

What HBT parameters determine logic speed ?

	Cje	Ccbx	Ccbi	$(\tau_b+\tau_c)$ (I/ΔV)	total
ΔV/ I	33.5%	6.7%	27.8%		68.4%
ΔV/ I				12.3%	12.3%
(kT/q) I	1.4%	0.1%	0.4%	0.5%	2.5%
Rex	-1.3%	0.1%	0.3%	0.9%	0.1%
Rbb	10.2%		2.8%	3.7%	16.7%
total	43.8%	6.8%	31.3%	17.5%	100.0%
		38%			

Sorting Delays by capacitances :

44% charging C_{je}, 38% charging C_{cb}, only 18% charging C_{diff} (e.g. $\tau_b + \tau_c$)

Sorting Delays by resistances and transit times :

68% from $\Delta V_{\text{logic}} / I_c$, 12% from $(\tau_b + \tau_c)$, 17% from R_{bb}

R_{ex} has very strong indirect effect, as $\Delta V_{logic} > 6 \bullet \left(kT/q + I_C R_{ex}\right)$

Caveats:
assumes a specific UCSB InP HBT (0.7 um emitter, 1.2 um collector 2kÅ thick, 400 Å base, 1.5E5 A/cm^2)
ignores interconnect capacitance and delay, which is very significant

Yoram Betser, Raja Pullela

Logic Speed

..	c_{je}	c_{cbx}	c_{cbi}	$\tau_f J/\Delta V_L$
$\Delta V_L/J$	1	6	6	1
kT/qJ	0.5	1	1	0.5
ρ_e	-0.25	0.5	0.5	0.5
r_{bb}	0.5	0	1	0.5

Approximate delay coefficients a_{ij} for an ECL master-slave flip-flop, found by hand analysis. Gate delay is of the form $T_{gate} = 1/2 f_{clock,\max} = \Sigma a_{ij} r_i c_j$, where f_{clock} is the maximum clock frequency. The minimum logic voltage swing is $\Delta V_{LOGIC} > 6(kT/q + J\rho_{ex})$

Caveat: ignores interconnect capacitance and delay, which is very significant

Yoram Betser
Raja Pullela

Logic Speed: definition of terms

c_{je} : emitter base depletion capacitance per unit emitter area

c_{cbi} : intrinsic collector base capacitance per unit emitter area

c_{cbx} : extrinsic collector base capacitance per unit emitter area

τ_f : sum of base and collector transit times

J : emitter current per unit emitter area

ΔV_{LOGIC} : logic voltage swing

r_{bb} : base resistance times emitter area (e.g. "per-area" R_{bb})

ρ_{ex} : emitter resistance times emitter area (e.g. "per-area" R_{ex})

Why isn't base+collector transit time so important ?

Under Small-Signal Operation :

$$\delta Q_{\text{base}} = (\tau_b + \tau_c)\delta I_C = (\tau_b + \tau_c)\frac{dI_C}{dV_{be}}\delta V_{be} = \frac{(\tau_b + \tau_c)I_C}{kT/q}\delta V_{be}$$

Under Large-Signal Operation :

$$\Delta Q_{\text{base}} = (\tau_b + \tau_c)I_C = \frac{(\tau_b + \tau_c)I_{dc}}{\Delta V_{LOGIC}}\Delta V_{LOGIC}$$

Large-signal diffusion capacitance reduced by ratio of

$$\left(\frac{\Delta V_{LOGIC}}{kT/q}\right), \text{ which is} \sim 10:1$$

Depletion capacitances see no such reduction

roadmap

Technology Roadmaps for 40 / 80 / 160 Gb/s

Parameter	Transferred-Substrate HBT	Mesa HBT Generation 1	Mesa HBT Generation 2	Mesa HBT Generation 3
Predicted MS-DFF speed (no interconnects)	93 GHz	62 GHz	125 GHz	237 GHz
Observed speed	75 GHz			
Emitter Junction Width	0.6 µm	1 µm	0.8 µm	0.2 µm
Parasitic Resistivity	30 Ω-μm^2	50 Ω-μm^2	20 Ω-μm^2	5 Ω-μm^2
Base Thickness	400 Å	400Å	300Å	250Å
Doping	4 10^{19} /cm^2	5 10^{19} /cm^2	5 10^{19} /cm^2	5 10^{19} /cm^2
Sheet resistance	750 Ω	750 Ω	700 Ω	700 Ω
Contact resistance	150 Ω-μm^2	150 Ω-μm^2	20 Ω-μm^2	10 Ω-μm^2
Collector Width	1.5 µm	3 µm	1.6 µm	0.4 µm
Collector Thickness	2000 Å	3000 Å	2000 Å	1000 Å
Current Density	1.8 mA/μm^2	1 mA/μm^2	2.3 mA/μm^2	9.3 mA/μm^2
$A_{collector}/A_{emitter}$	2.5	4.55	2.6	2.6
f_τ	180	170	260	500
f_{max}	220	170	440	1000
C_{cb} / I_c	0.8 ps/V	1.7 ps/V	0.63 ps/V	0.31 ps/V
$C_{cb}\Delta V_{logic} / I_c$	0.24 ps	0.5 ps	0.19 ps	0.093 ps
$R_{bb} /(\Delta V_{logic} / I_c)$	0.9	0.8	0.65	0.52
$C_{je} (\Delta V_{logic} / I_C)$	0.9 ps	1.7 ps	0.72 ps	0.18 ps
$R_{ex} /(\Delta V_{logic} / I_c)$	0.12	0.1	0.15	0.15

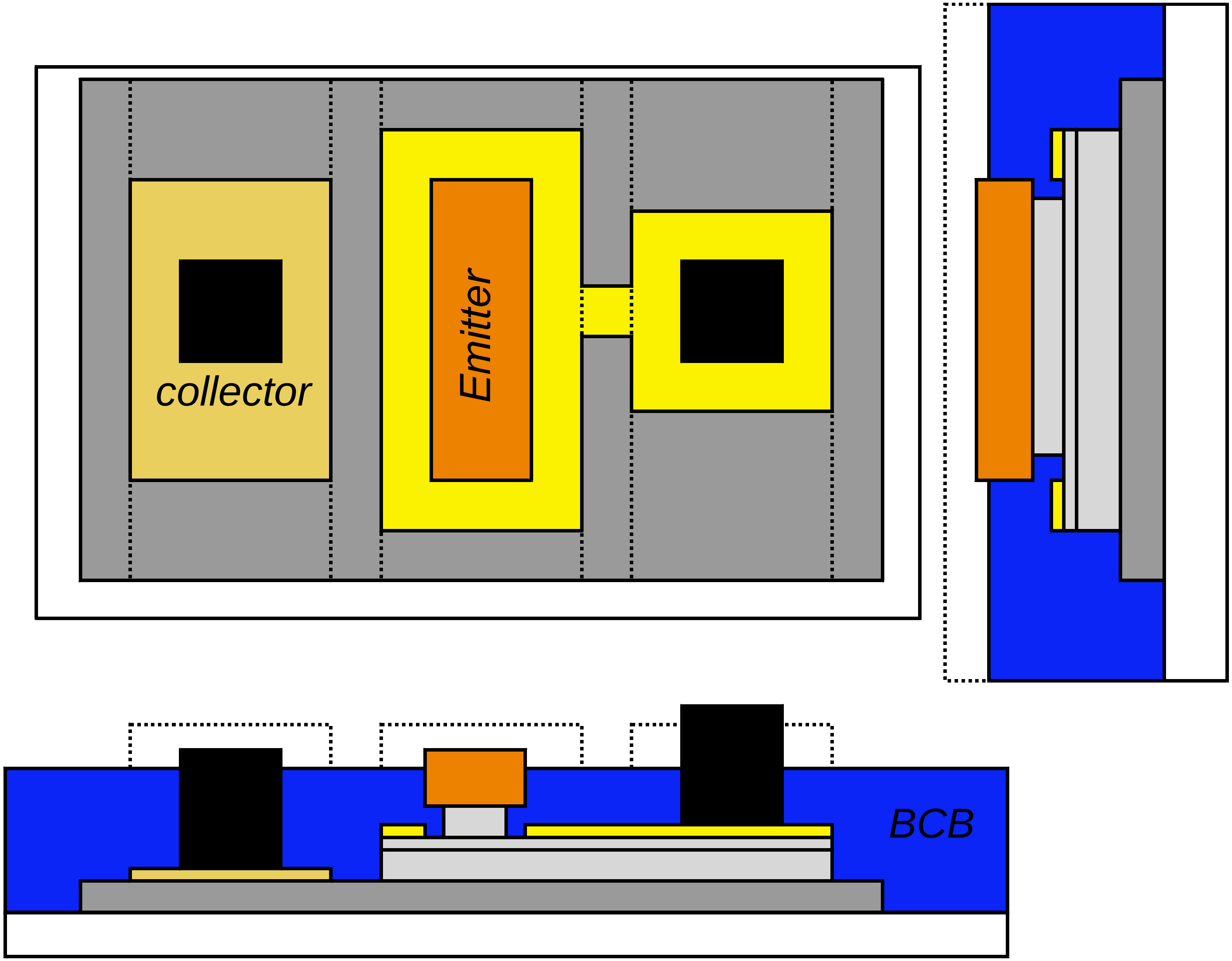
Technology Roadmaps for 40 / 80 / 160 Gb/s

80 Gb/s technology node:
Change from 40 Gb/s does not fully follow scaling laws. Why ?
Lithographic scaling eased by carbon base doping.
Current density scaling eased by reduced excess collector area.

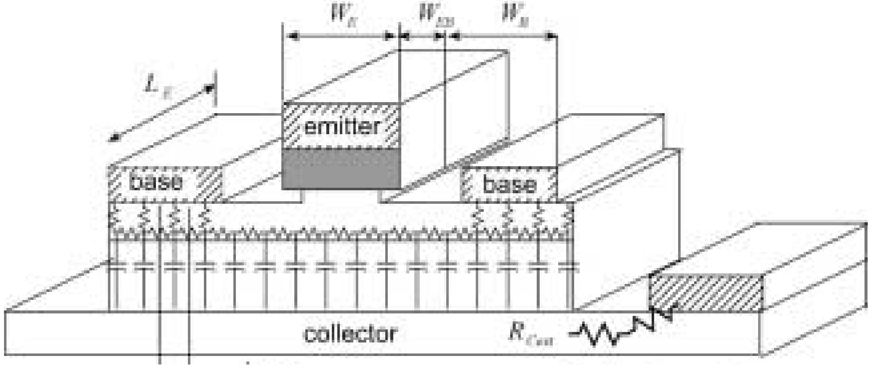
160 Gb/s technology node:
Direct application of scaling laws.
Aggressive current density and lithographic scaling required.
If further improved base contact resistance → relax lithographic scaling
Further reduce $A_{collector}/A_{emitter}$ ratio → relax current density scaling
…note that $A_{collector}/A_{emitter}$ <2.5 looks hard at deep submicron.

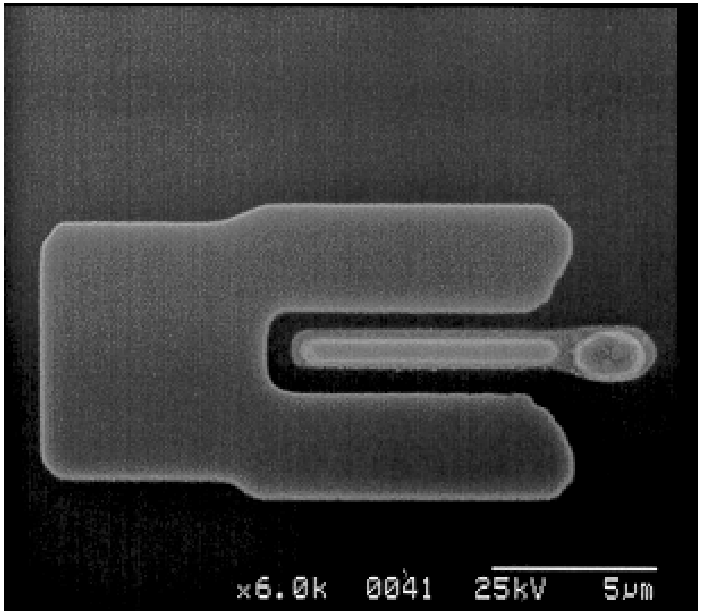
device structures

InP mesa HBT

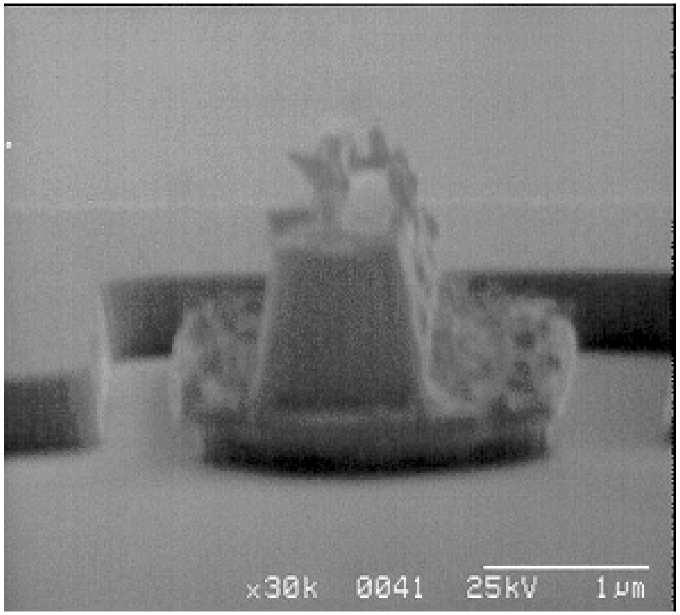


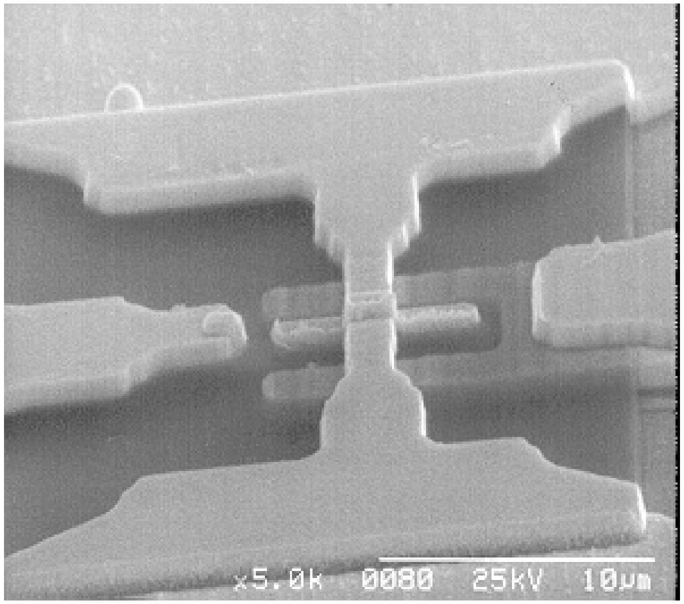
Narrow-Mesa HBTs: high f_τ & f_{max} if high base doping





0.5 µm emitter,
0.25 µm base
contacts

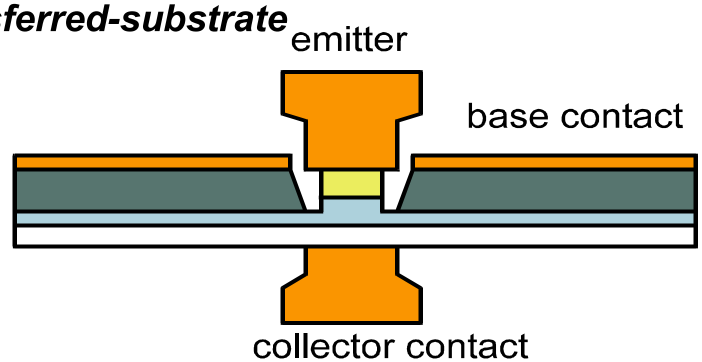




Mattias Dahlstrom

Low Ccb HBT structures

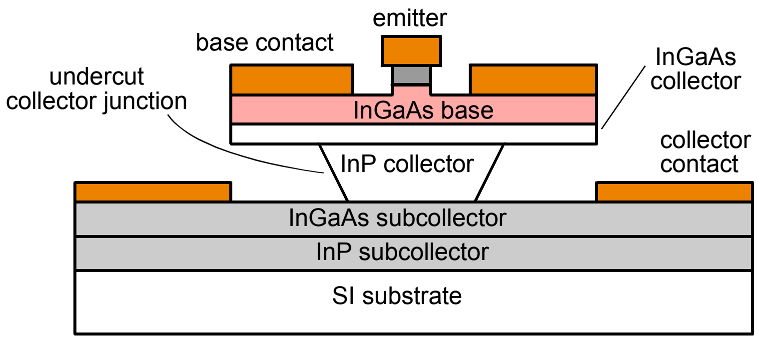
transferred-substrate



Extremely high demonstrated fmax
75 GHz (record) static frequency dividers

Too low yield for manufacturing (?)

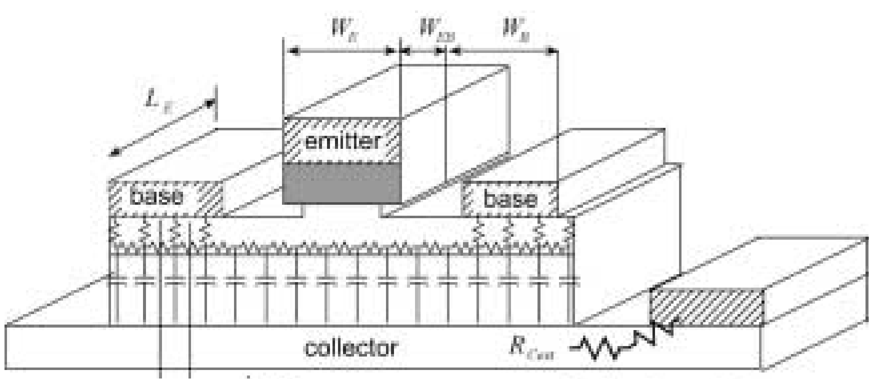
undercut-collector



Pursued by several research groups

Also has uncertain yield at submicron geometries

Narrow-mesa with ~1E20 carbon-doped base



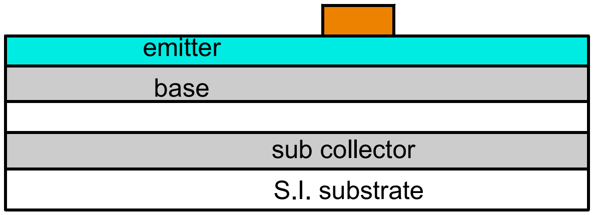
The conservative device structure

Yet, I assert that even this device is not viable of mass manufacturing if
> 3000 transistors per IC are sought

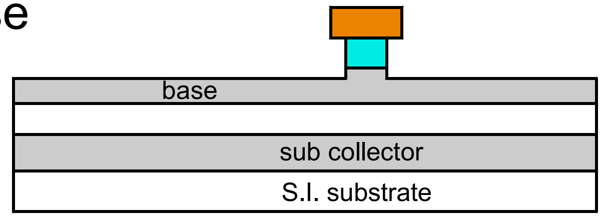
yield and fabrication

InP HBT limits to yield: ***non-planar process***

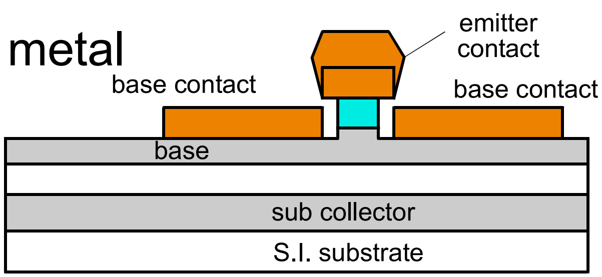
Emitter contact



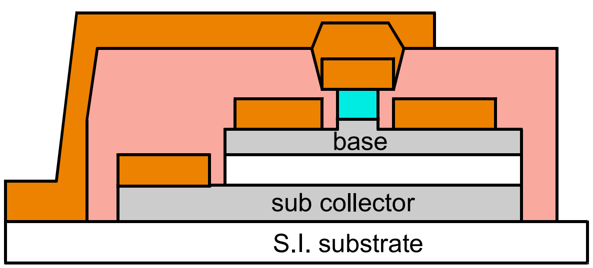
Etch to base



Liftoff base metal

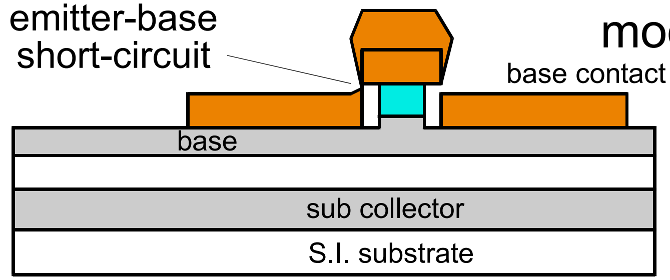


Emitter planarization, interconnects

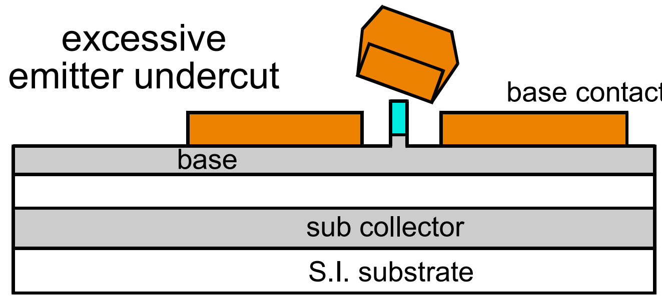


Failure modes

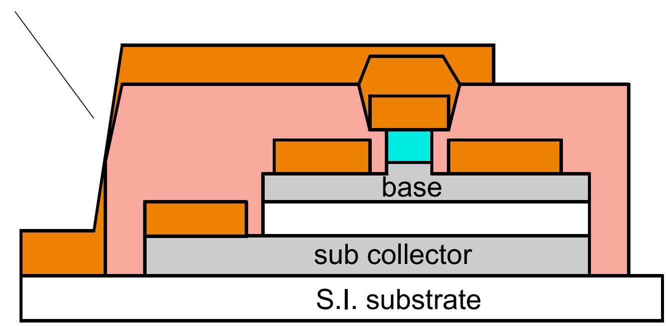
liftoff failure: emitter-base short-circuit



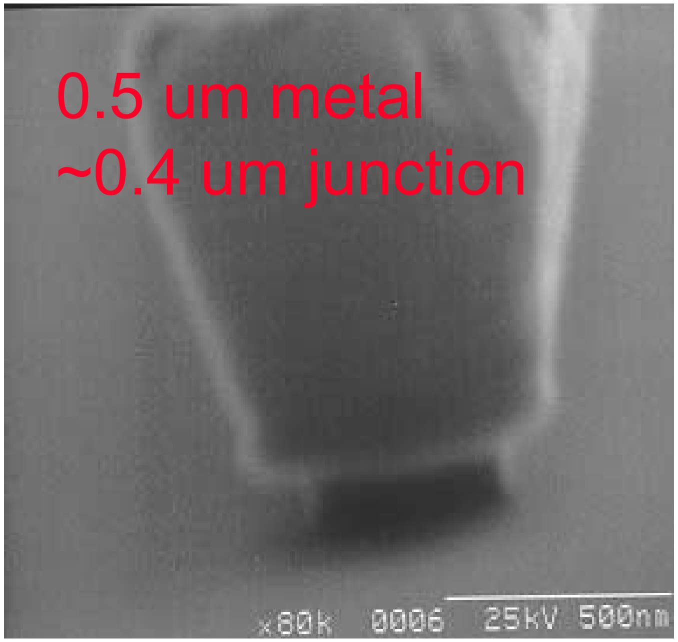
excessive emitter undercut

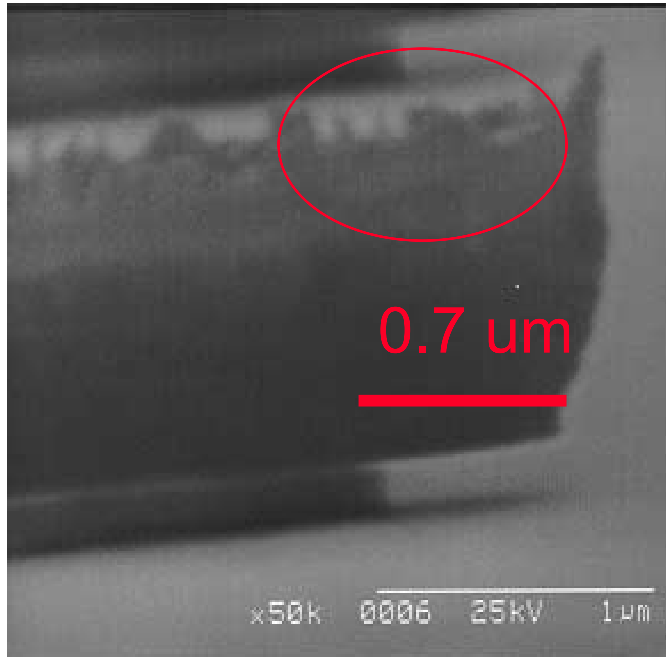


planarization failure: interconnect breaks



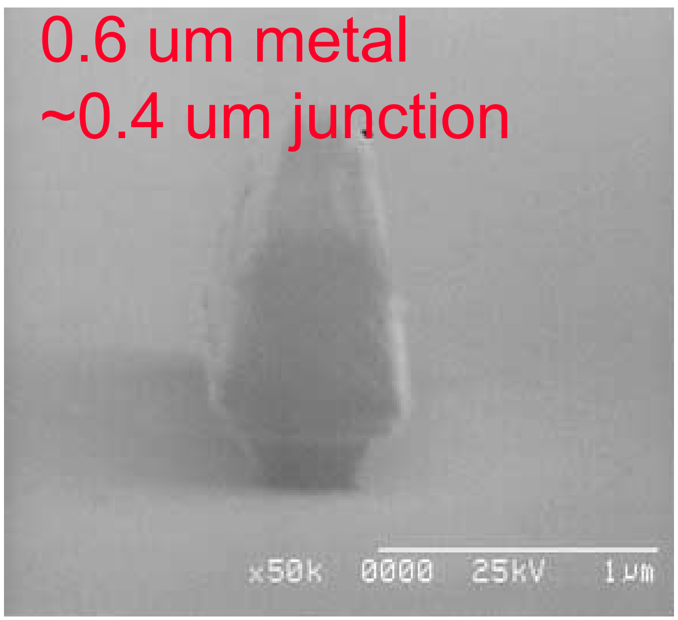
Yield degrades as emitters are scaled to submicron dimensions

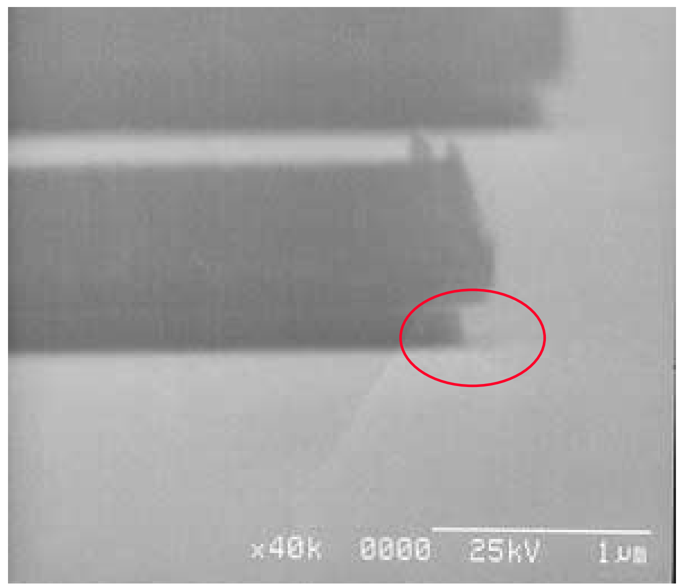




InP

Front and side views





InAlAs

Front and side views

Smaller emitters → lower yield. Need better fabrication process

InP vs. SiGe

Digital
InP has slightly higher speed, much less power
InP can't meet integration scales of many complex fast ICs

Analog:
Combined InP speed and breakdown are key advantages

mm-wave wireless / RF (60 GHz, etc)
No significant market yet
InP HBT could be strong contender (fast and cheap)

Fast, high-yield InP HBT IC processes are critically needed

InP vs. SiGe

III-V literature, III-V research community:
large inherent advantages in transport parameters over Si
research focused on transport physics, poorly tied to circuit design
$\rightarrow$ ***devices not well-tuned for circuits, poor parasitic reduction***
$\rightarrow$ ***university-like fabrication, low yield, low scales of integration***

Silicon research community
focused on ***SCALING****, closely tied to* ***circuit*** *design, focus on* ***YEILD***
strong ***extrinsic parasitic reduction***
result: very good SiGe HBT digital circuit speed, large fast ICs

InP HBT has fundamental advantages which will allow it to scale beyond SiGe HBT scaling limits, but must address:

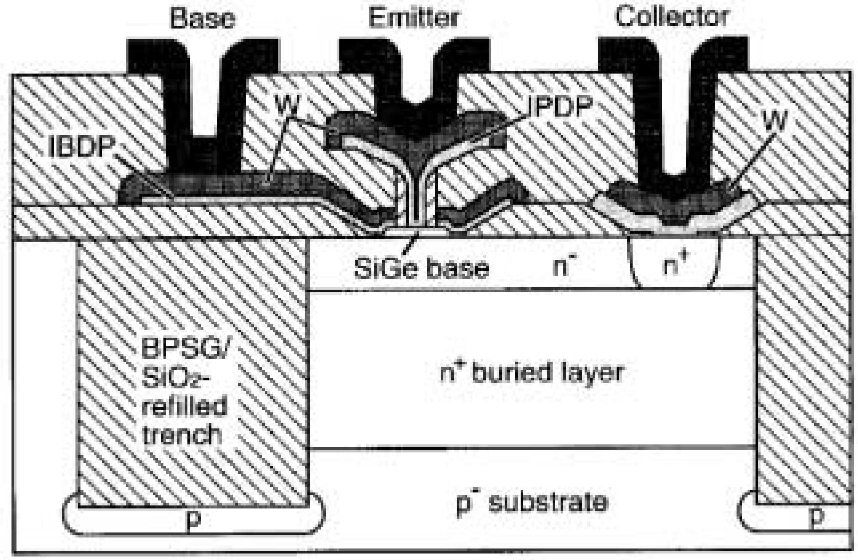
yield*: Silicon-like planar implanted / regrowth processes*
speed*: device scaling informed by understanding of circuit design*

InP vs. Si/SiGe HBTs: materials vs. scaling advantages

Good:
Narrow emitter: 0.18 um
High current density: 10 mA/um^2
Large emitter contact: low resistance
Polysilicon base contact: low resistance
SiO2 trenches: small collector capacitance
Planar device : high yield

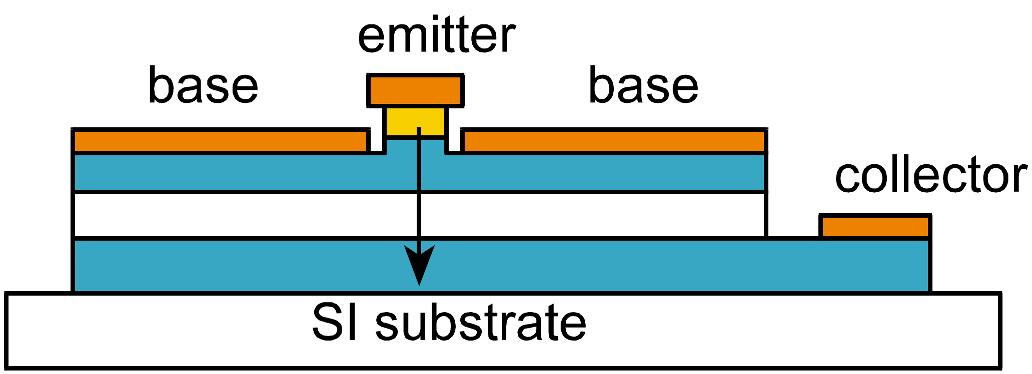
Bad:
High base sheet resistance,
Low electron velocity, low breakdown limits scaling.

Equal speed at 5x smaller scaling.
Loss of breakdown may soon slow scaling



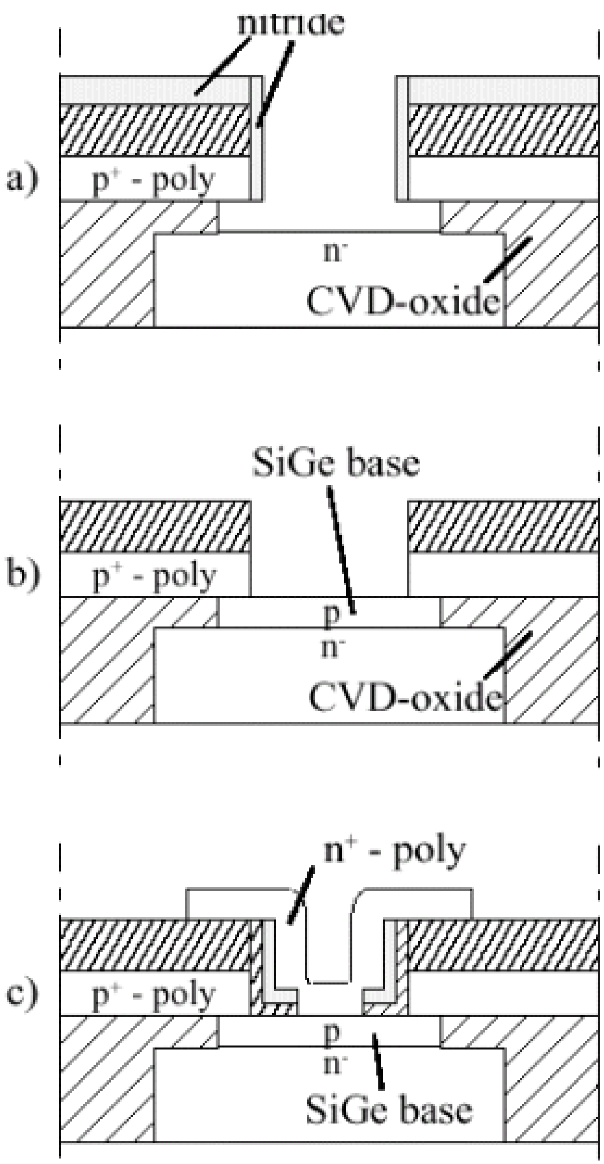
Good:
20x lower base sheet resistance,
5 x higher electron velocity,
4x higher breakdown-at same ft.

Bad:
Presently only scaled to ~ 1 um
Archaic mesa fabrication process:
large emitters, poor emitter contact:
low current density: 2 mA/um^2
high collector capacitance
nonplanar device : low yield



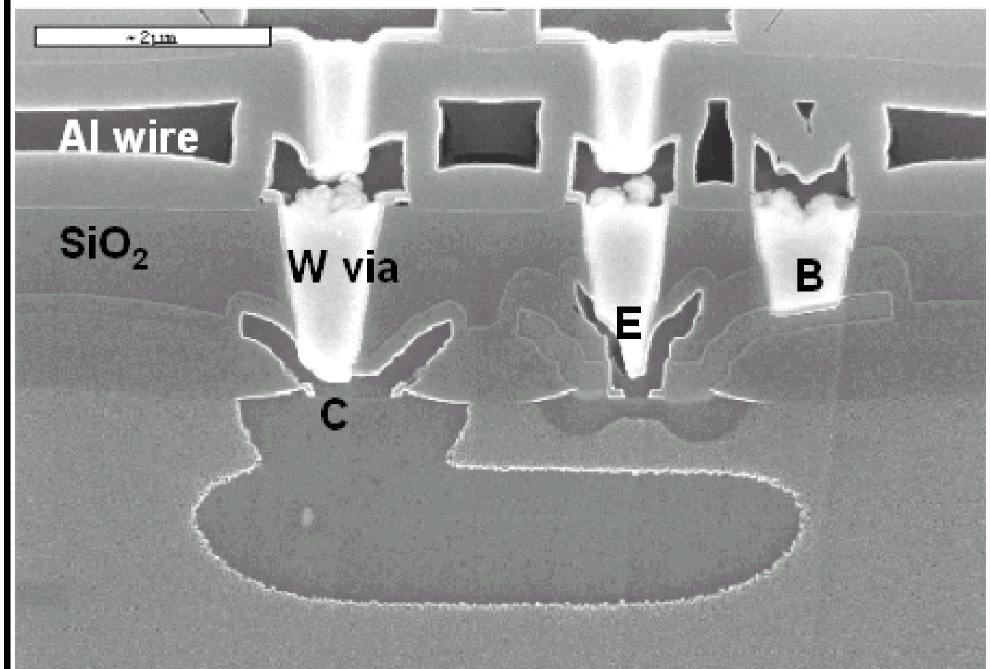
SiGe HBTs high yield: ***regrown emitter, planar process, VLSI interconnects***

0.2 um emitters are regrown, ***not etched***



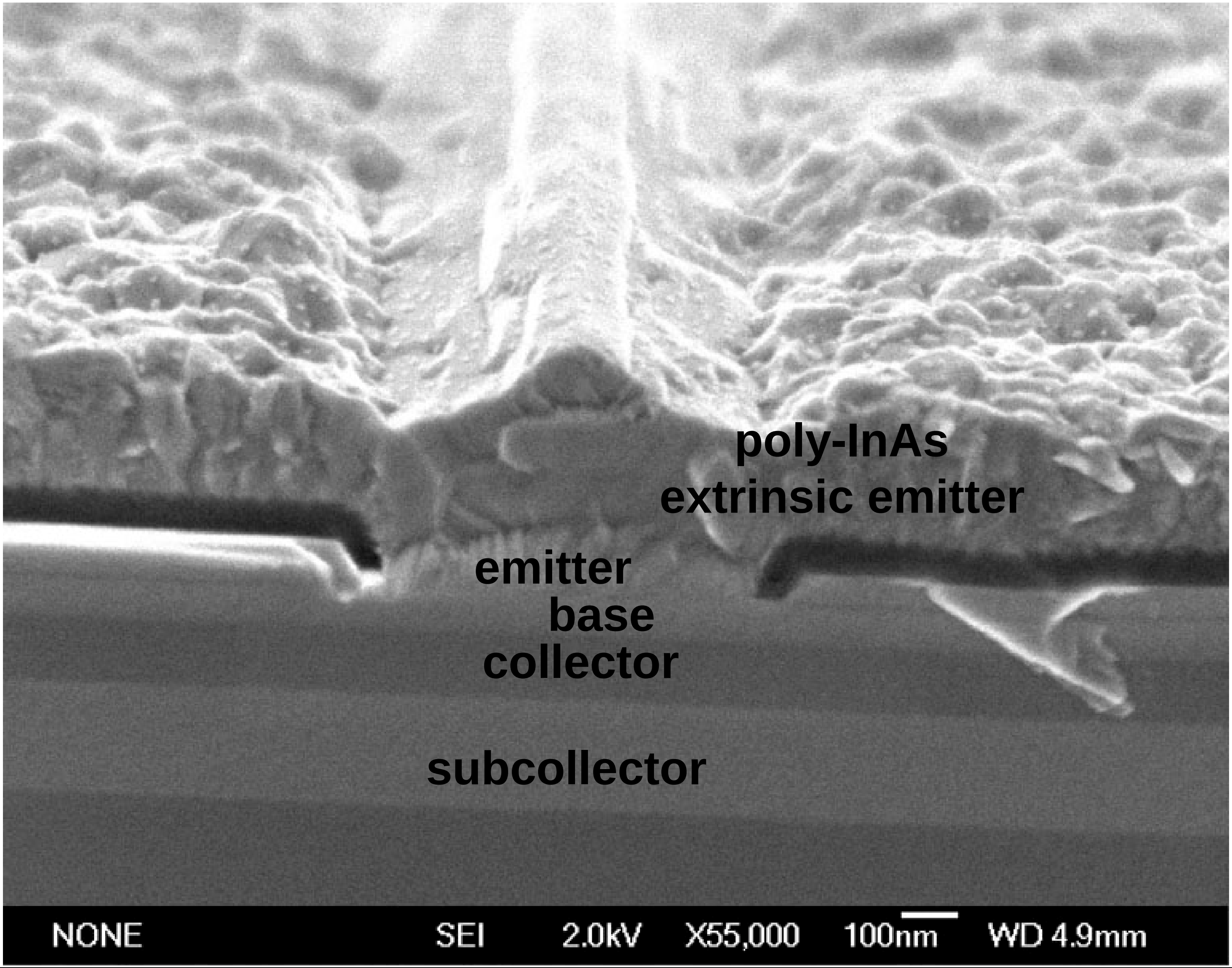
Wurzer et al. International Jountal of High Speed Electronics and Systems. 2001

Transistor is planar,
interconnects are standard for VLSI
(W/ Al with SiO_2)



Wurzer et al. International Jountal of High Speed Electronics and Systems. 2001

ONR *InAlAs/InGaAs/InP DHBT with polycrystalline extrinsic emitter regrowth.* UCSB
Dennis Scott

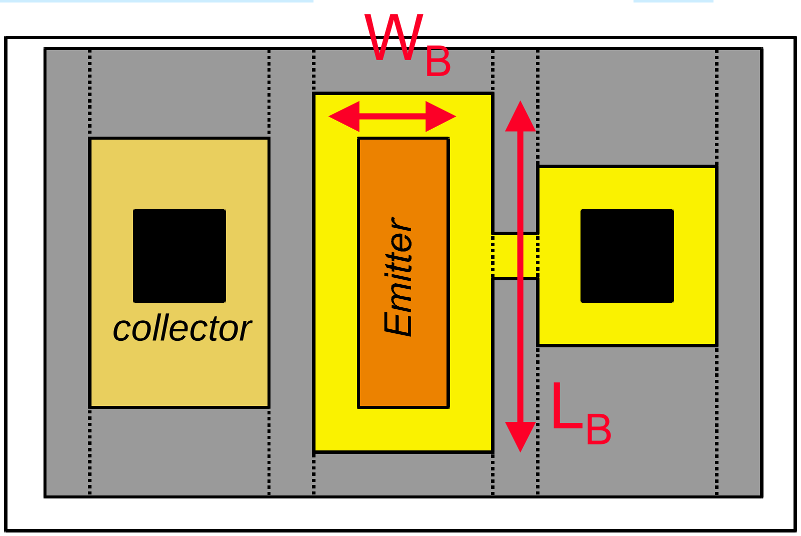


thermal resistance and thermal runaway

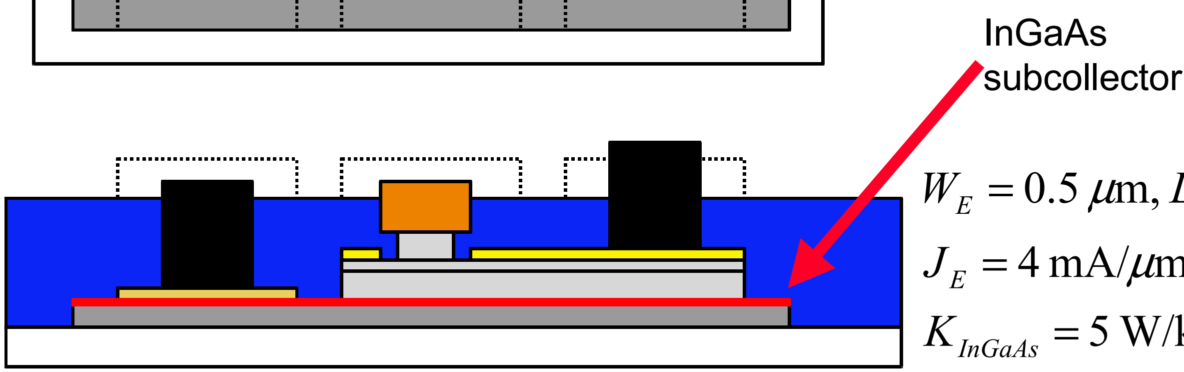
Thermal resistance and effect of subcollector

$$\theta_{JA} \approx \frac{T_{InP,c}/2}{K_{InP}W_E L_E} + \frac{T_{InGaAs}}{K_{InGaAs}W_B L_B} + \frac{1}{\pi K_{InP} L_B}\ln\left(\frac{L_B}{W_B}\right) + \frac{1}{\pi K_{InP} L_B}$$

ΔT, 2000 Å InGaAs	7	127	16	11
ΔT, 200 Å InGaAs	7	13	16	11



Approximation:
InGaAs dominates thermal resistance
→ heat flows through InGaAs in area equal base mesa (excluding pad)



$W_E = 0.5\ \mu\text{m}, L_E = 3\ \mu\text{m}, W_B = 0.7\ \mu\text{m}, L_E = 3.25\ \mu\text{m},$

$J_E = 4\ \text{mA}/\mu\text{m}^2, V_{CE} = 1.2\ \text{V}$

$K_{InGaAs} = 5\ \text{W/k-m}\quad K_{InP} = 68\ \text{W/k-m}$

W. Liu, H-F Chau, E. Beam III, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors", IEEE Transactions on Electron Devices, vol.43, (no.3), IEEE, March 1996. p.388-95.

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Poor performance observed in multi-finger DHBT

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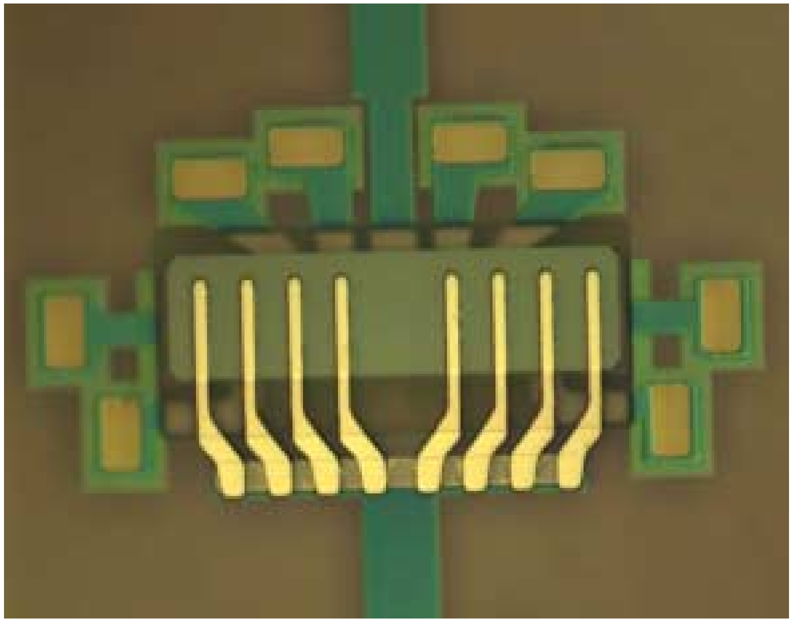
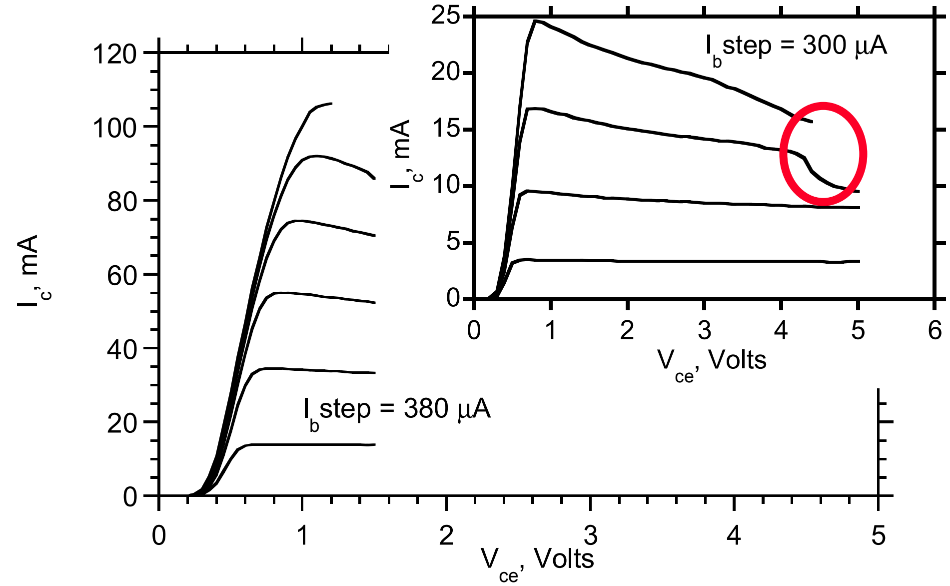
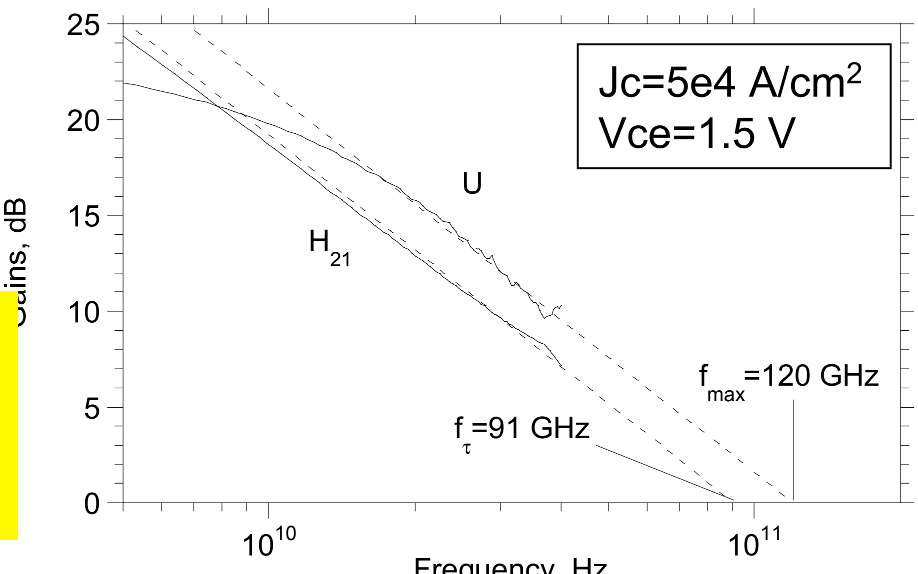




8 finger common emitter DHBT
Emitter size: 16 um x 1 um
Ballast resistor (design):9 Ohm/finger



current hogging observed
fmax also low due to high
base feed resistance

W. Liu, H-F Chau, E. Beam III, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors", IEEE Transactions on Electron Devices, vol.43, (no.3), IEEE, March 1996. p.388-95.

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Restrictions on DHBT sizing: distributed base feed resistance

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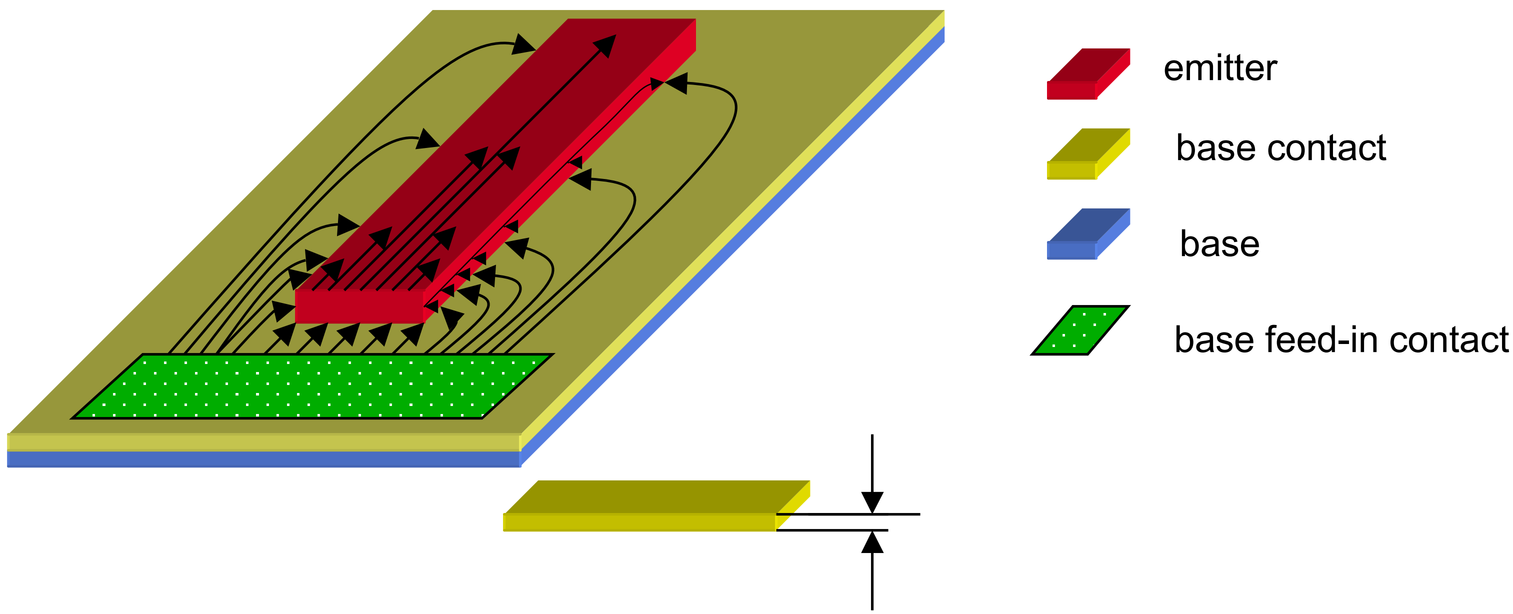

Self-aligned base contact thickness=0.08 μm
Leads to feed sheet resistance:
ρ = 0.3 Ω/□
restricts emitter length to ~15 μm

Excess Rbb, hence reduced f_{max}
(big HBT has big C_{cb}, small R_{bb}, hence even small excess R_{bb} reduces f_{max})

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DHBT thermal stability: multiple emitter fingers

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Yun Wei

Assume initial temperature difference δT between 2 fingers

$$\frac{dV_{be}}{dT} = -1.1\,\text{mV/K at constant } I_c$$

$$\delta T \Rightarrow \delta V_{be} = \frac{dV_{be}}{dT}\delta T \Rightarrow \delta I_C = \frac{1}{R_{ex} + R_{ballast} + kT/qI_E}\delta V_{be}$$

$$\Rightarrow \delta P = V_{CE}\delta I_C \Rightarrow \delta T = \theta_{JA}\delta P$$

Unstable unless

$$K_{\text{thermal stability}} = \left|\frac{dV_{be}}{dT}\right| \frac{V_{CE}\theta_{JA}}{R_{ex} + R_{ballast} + kT/qI_E} < 1$$

W. Liu, H-F Chau, E. Beam III, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors", IEEE Transactions on Electron Devices, vol.43, (no.3), IEEE, March 1996. p.388-95.

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Thermal runaway within a finger

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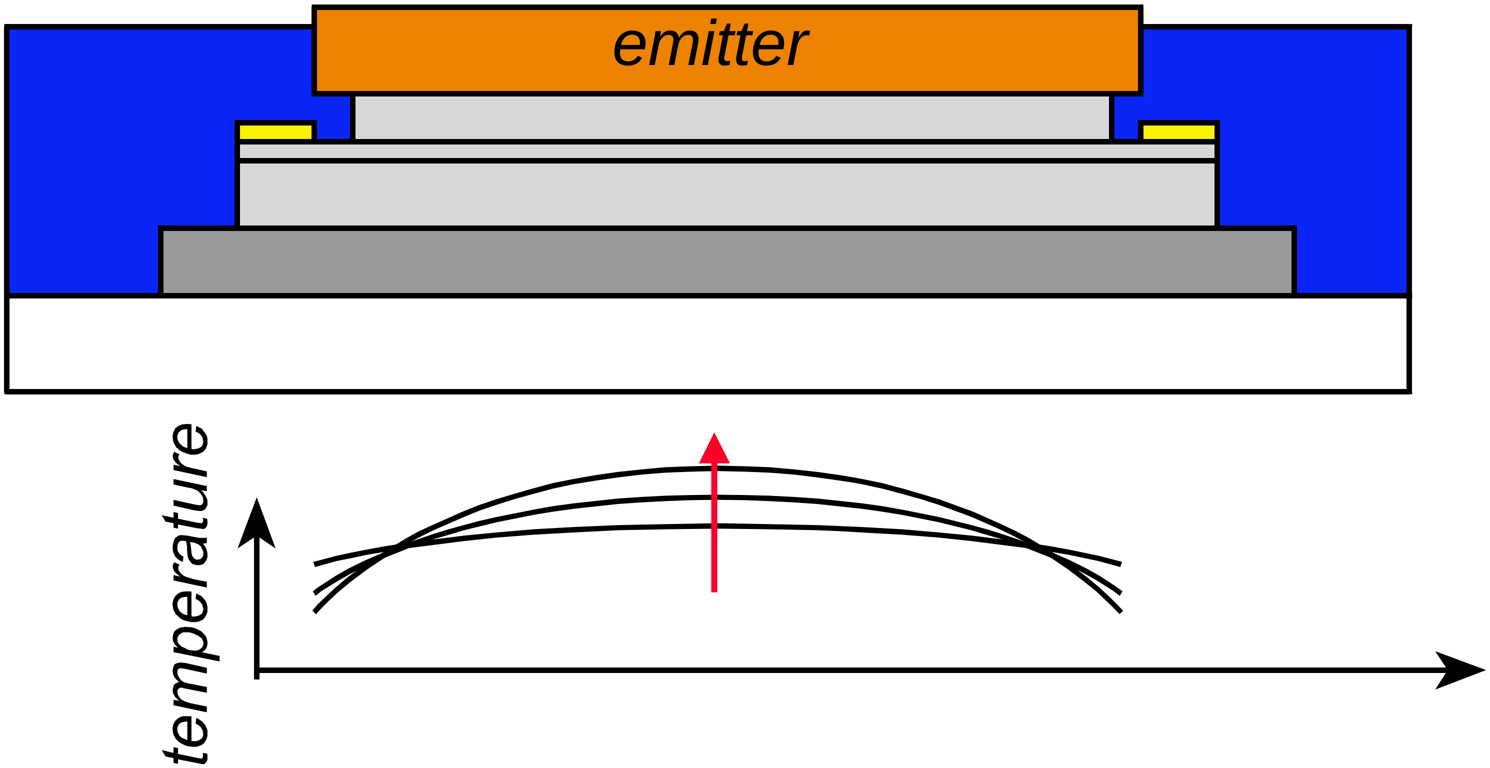

With long emitter finger, current-crowding can occur within finger

- Long finger: temperature can vary along length of emitter finger
  - loss of strong thermal coupling
- Temperature gradients along finger results in nonuniform current distribution
  - center of stripe gets hotter → carries more current → gets hotter → …
  - Premature Kirk-effect-induced collapse in f_t.

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Current hogging observation: multi-finger DHBT

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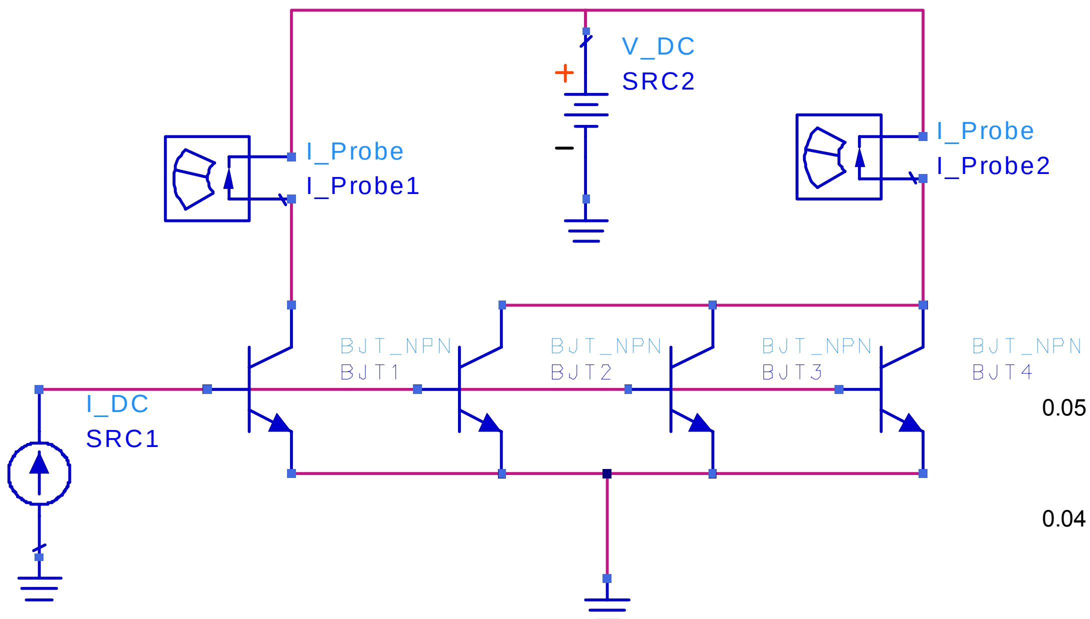

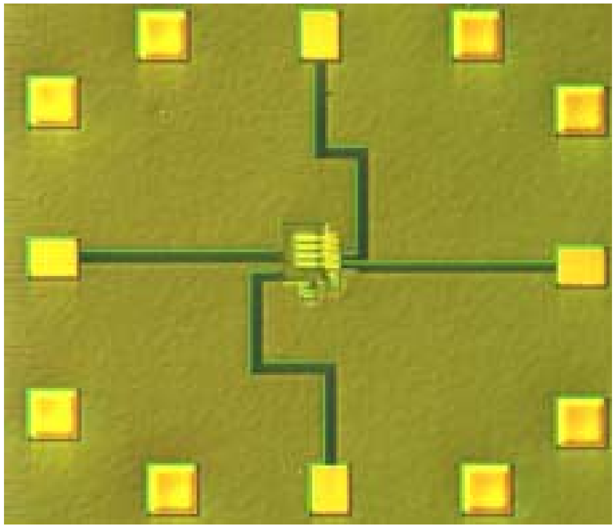

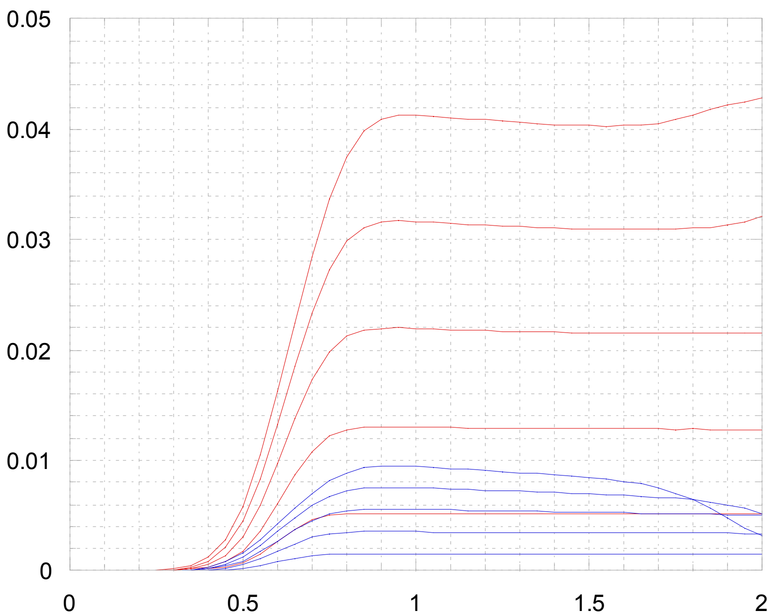

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Measuring DHBT thermal resistance

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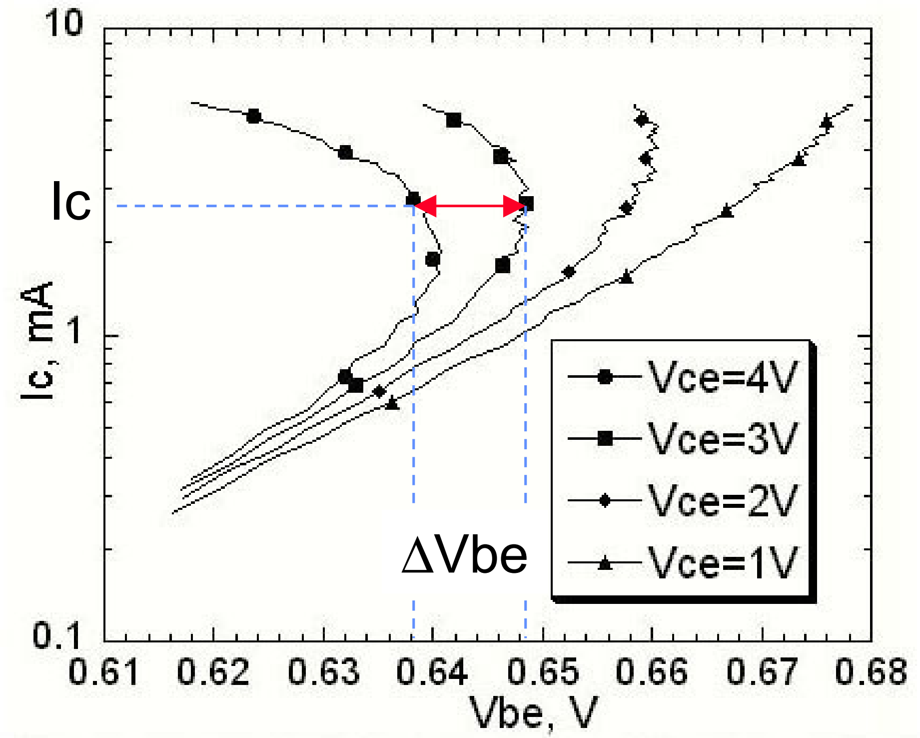
$$\delta V_{be}\Big|_{\text{fixed } I_c} = \frac{dV_{be}}{dT}\frac{dT}{dP}\frac{dP}{dV_{CE}}\delta V_{CE} = \left(-1.1\,\text{mV/K}\right)\cdot\theta_{JA} I_C \delta V_{CE}$$

$$\Rightarrow \theta_{JA} = \frac{dV_{be}}{dV_{CE}}\Bigg|_{\text{fixed } I_c} \times \frac{1}{I_C\left(-1.1\,\text{mV/K}\right)}$$



W. Liu, H-F Chau, E. Beam III, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors", IEEE Transactions on Electron Devices, vol.43, (no.3), IEEE, March 1996. p.388-95.

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Large current high breakdown voltage broadband InP DHBT

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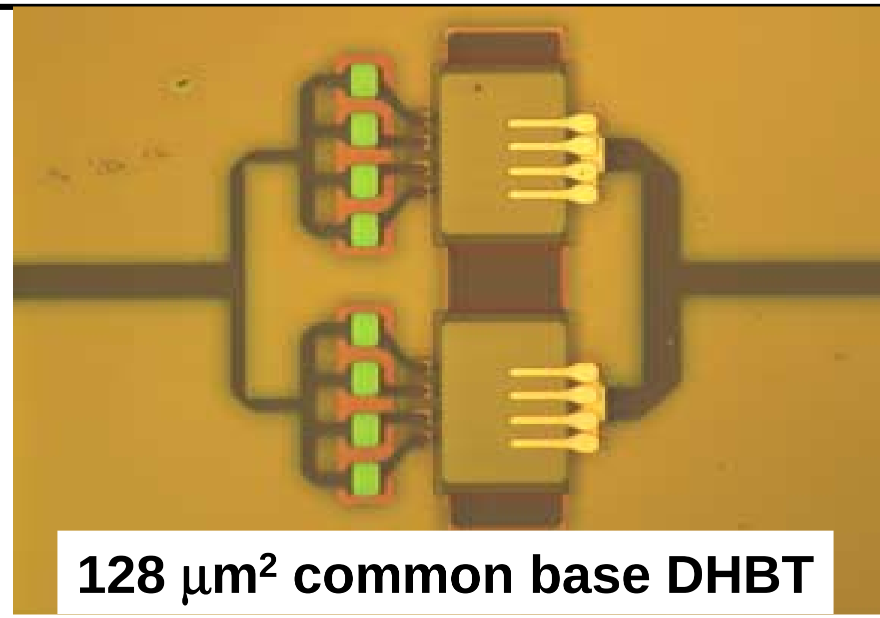
Objectives: f_{max}>300 GHz, *BVCEO*>6 V, J_{max}~1x10^5 A/cm^2

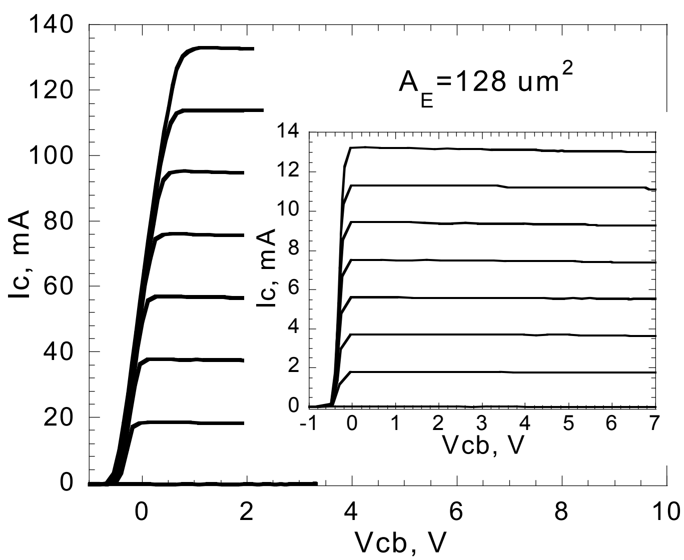
Approach: transferred-substrate multi-finger InP DHBTs, HBT thermal analysis

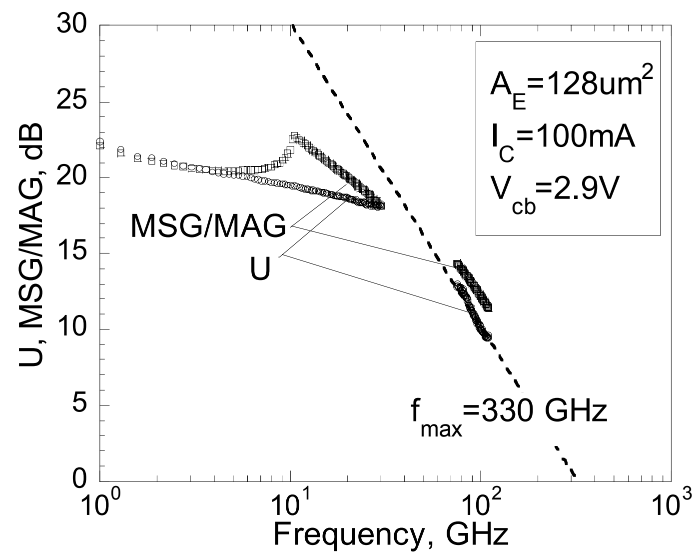
Simulations: large signal HBT spice model

Accomplishments:
f_{max}>330 GHz, Bv_{ce}>7 V, J_{max}>1x10^5 A/cm^2



128 μm^2 common base DHBT





On-wafer characterization of HBTs

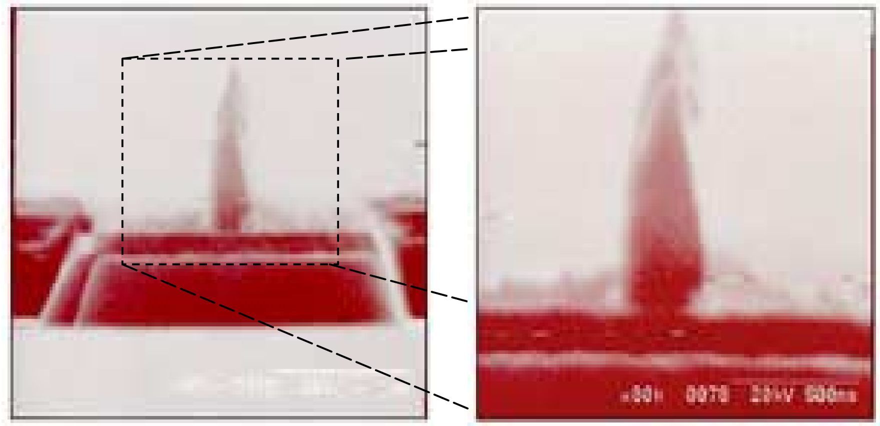
accurate and otherwise

Miguel Urteaga

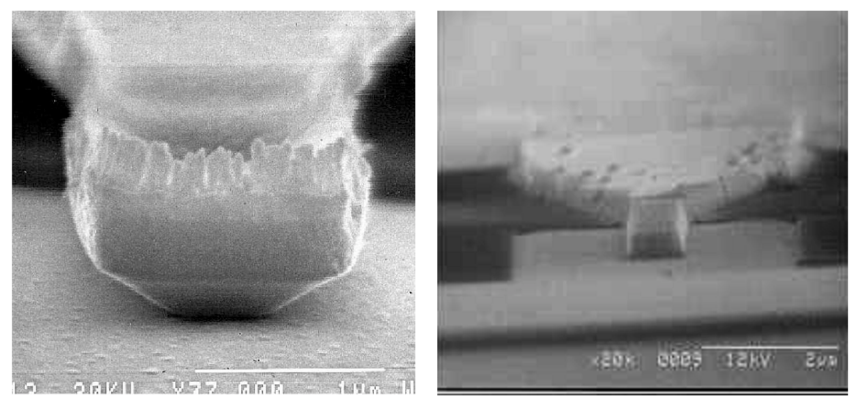
Ultra-high f_{max} Submicron HBTs

- Electron beam lithography used to define submicron emitters and collectors
- Minimum feature sizes
  - ⇒ 0.2 µm emitter stripe widths
  - ⇒ 0.3 µm collector stripe widths
- Improved collector-to-emitter alignment using local alignment marks
- Aggressive scaling of transistor dimensions predicts progressive improvement of f_{max}

As we scale HBT to <0.4 um,
f_{max} keeps increasing,
measurements become ***very*** difficult



0.3 µm Emitter before polyimide planarization



Submicron Collector Stripes
(typical: 0.7 um collector)

140-220 GHz On-Wafer Network Analysis

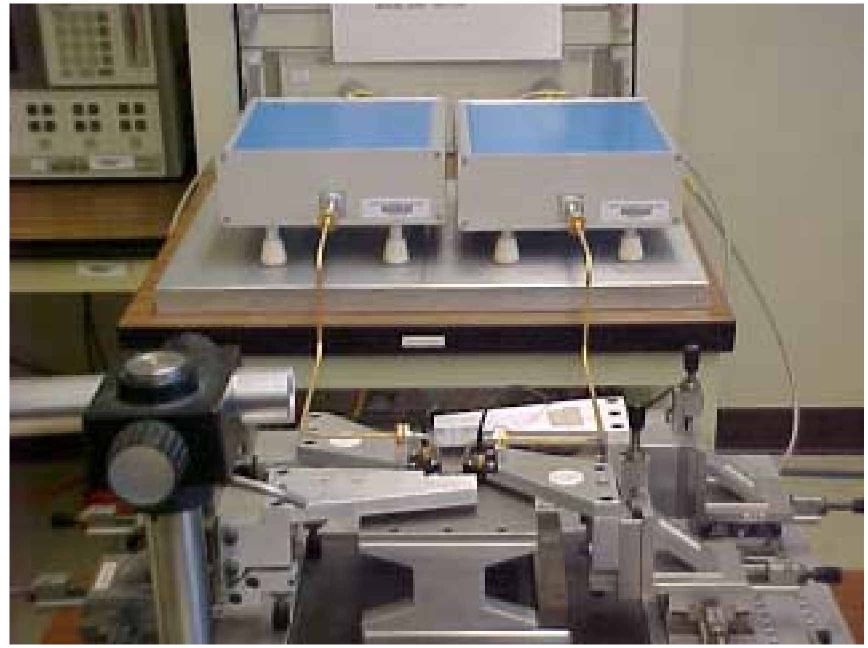
- HP8510C VNA, *Oleson Microwave Lab* mm-wave Extenders

- *GGB Industries* coplanar wafer probes

- connection via short length of WR-5 waveguide

- Internal bias Tee's in probes for biasing active devices

- 75-110 GHz set-up is similar



UCSB 140-220 GHz VNA Measurement Set-up

Miguel Urteaga

Accurate Transistor Measurements ***Are Not Easy***

- Submicron HBTs have **very low** C_{cb} (**< 3 fF**)
- Characterization requires accurate measure of very small S12
- Standard 12-term VNA calibrations do not correct S12 background error due to probe-to-probe coupling

Solution

Embed transistors in sufficient length of transmission line to reduce coupling

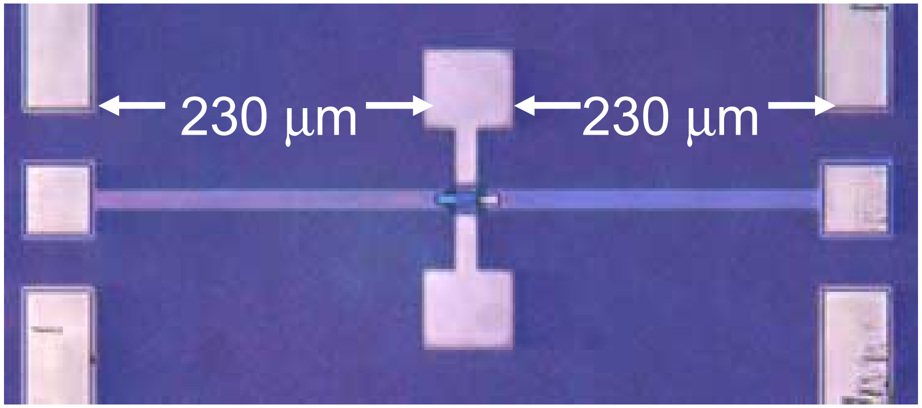
Place calibration reference planes at transistor terminals

Line-Reflect-Line Calibration

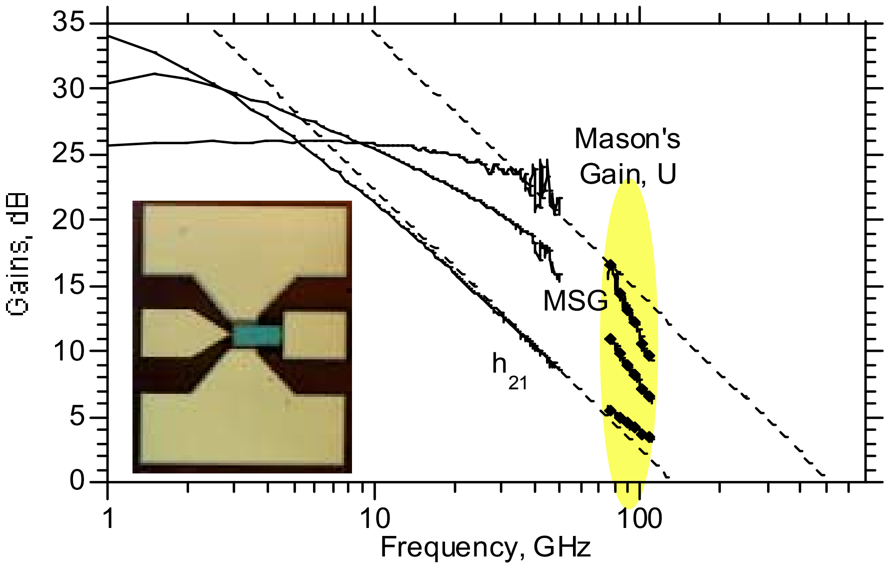
Standards easily realized on-wafer

Does not require accurate characterization of reflect standards

Characteristics of Line Standards are well controlled in transferred-substrate microstrip wiring environment



Transistor in Embedded in LRL Test Structure

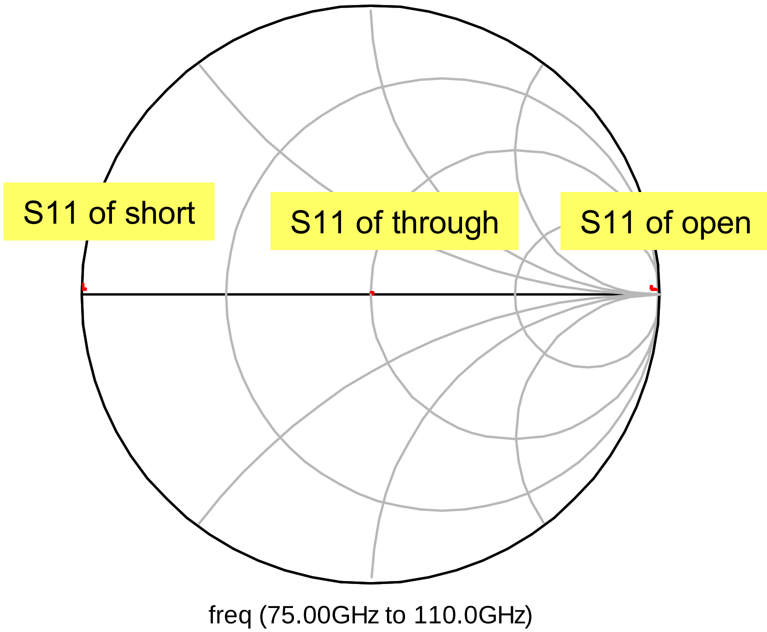


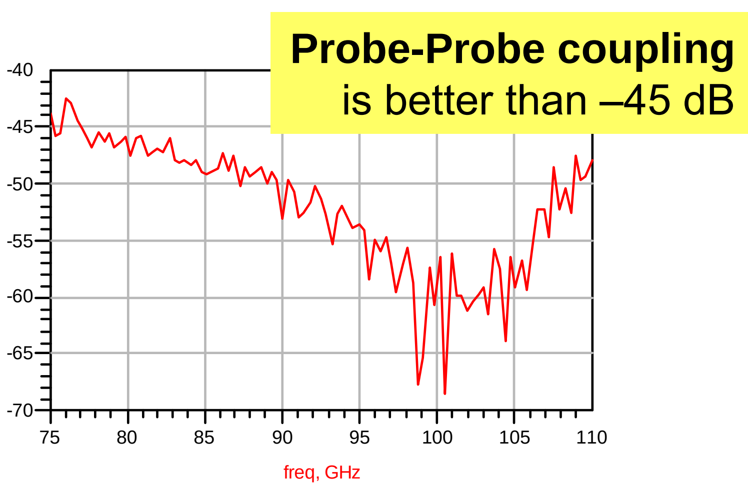
Corrupted 75-110 GHz measurements due to excessive probe-to-probe coupling

Miguel Urteaga

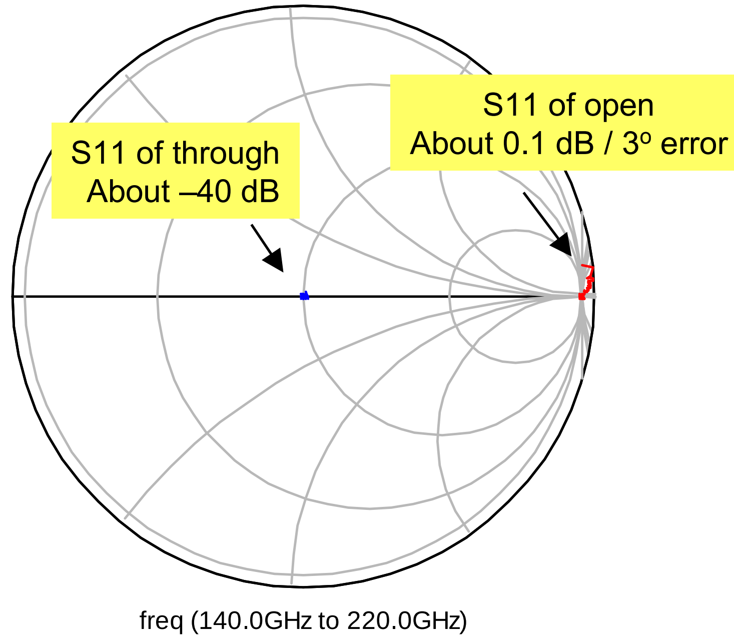
Can we trust the calibration ?

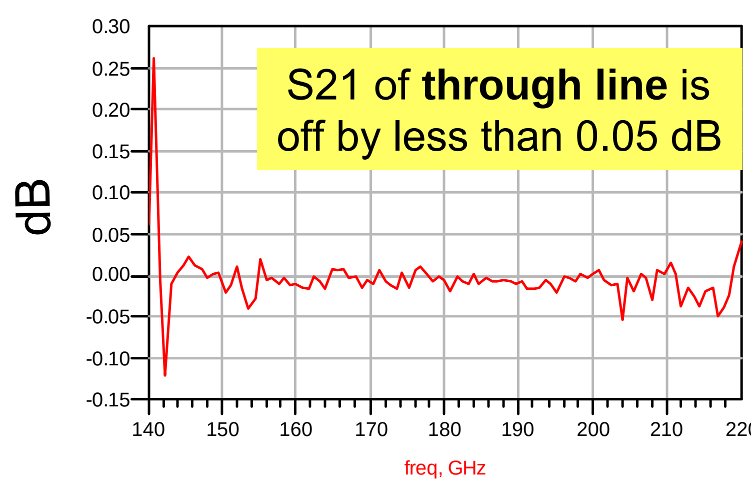
75-110 GHz calibration looks ***Great***





140-220 GHz calibration looks OK

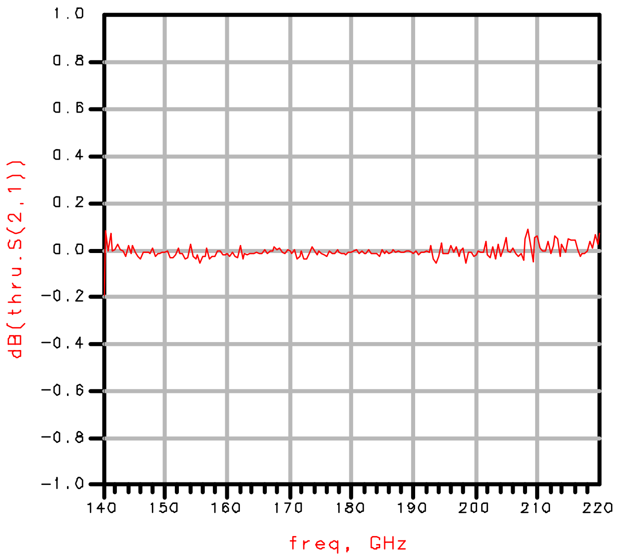




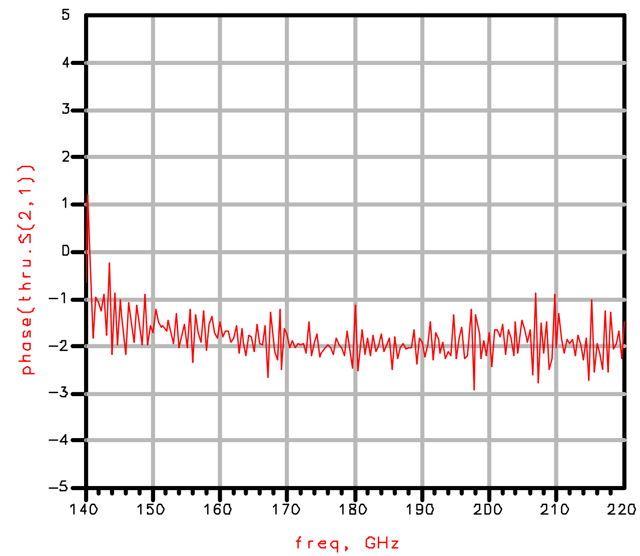
Miguel Urteaga

140-220 GHz Calibration Verification: Measurement of Thru Line after Calibration

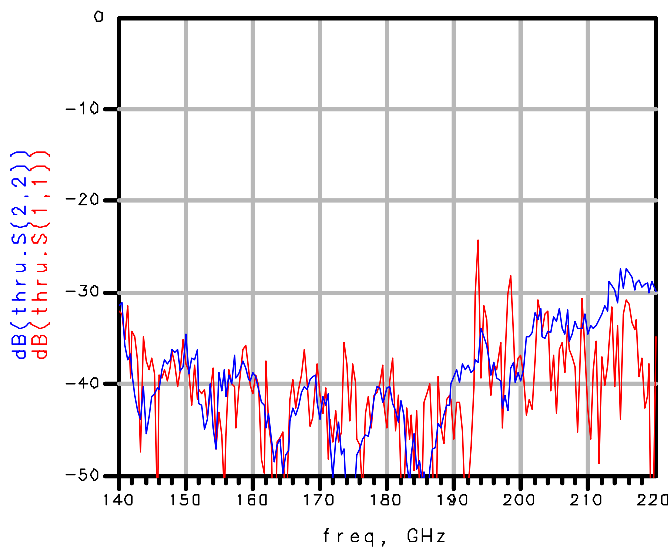
Magnitude S21 (dB)



Phase S21 (degrees)



S11, S22 (dB)



transistor results

Ultra-high f_{max} Transferred-Substrate HBTs

• Substrate transfer provides access to both sides of device epitaxy

• Permits simultaneous scaling of emitter and collector widths

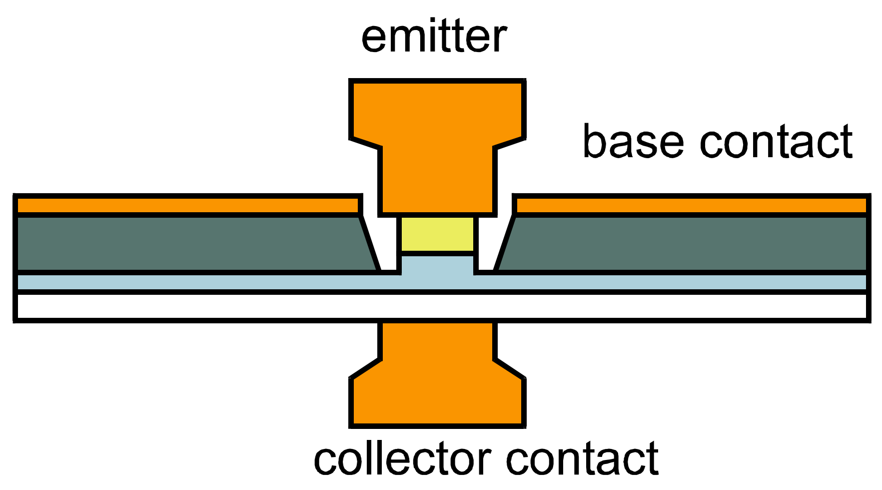
• Maximum frequency of oscillation

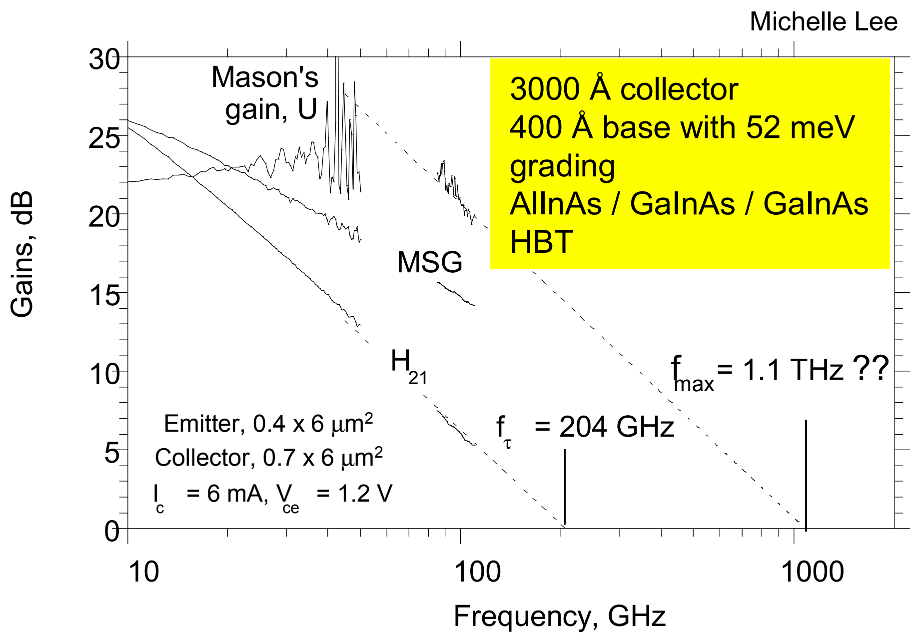
$$\Rightarrow \quad f_{\max} \cong \sqrt{f_\tau / 8\pi R_{bb} C_{cb}}$$

• Sub-micron scaling of emitter and collector widths has resulted in record values of **extrapolated** f_{max}

• **Extrapolation begins where measurements end**

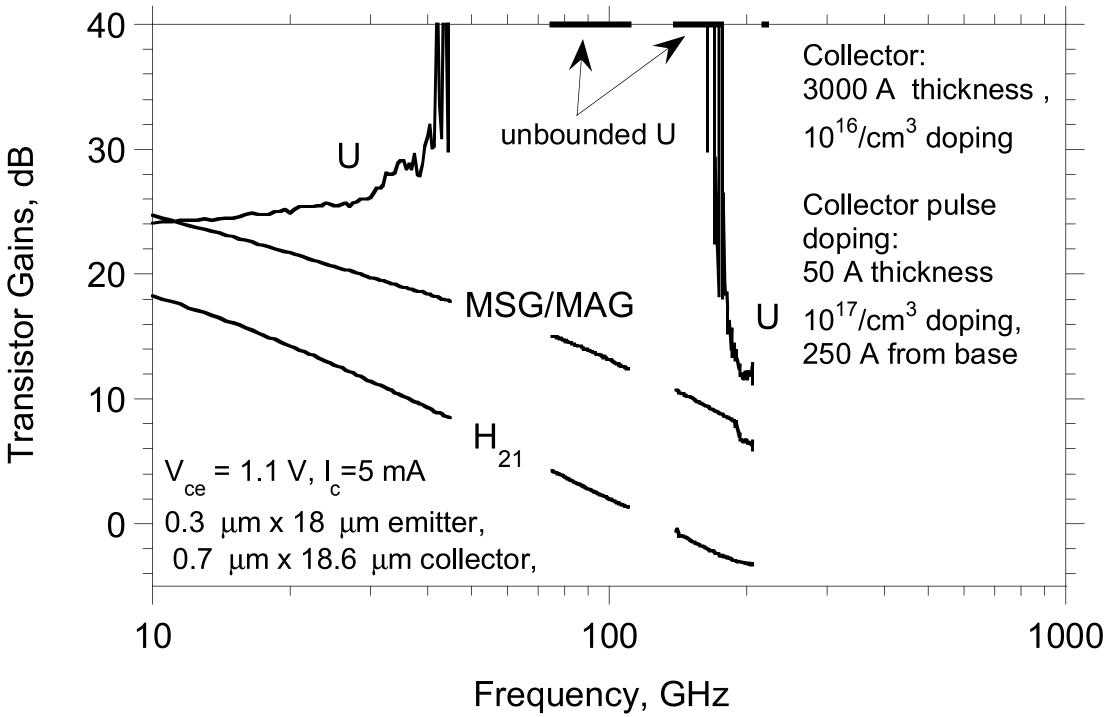
• **New 140-220 GHz Vector Network Analyzer (VNA) extends device measurement range**

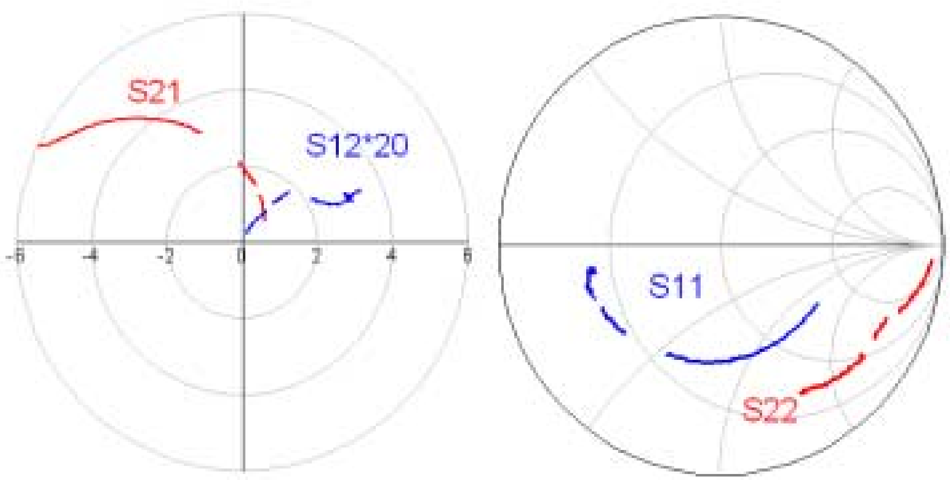


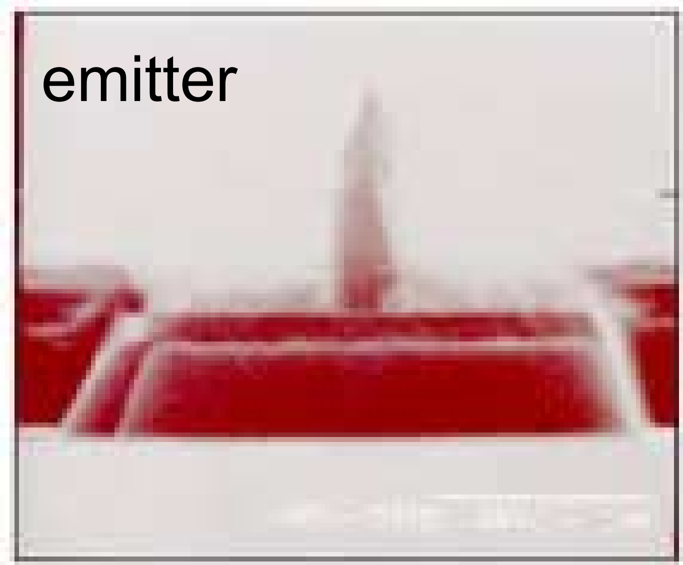


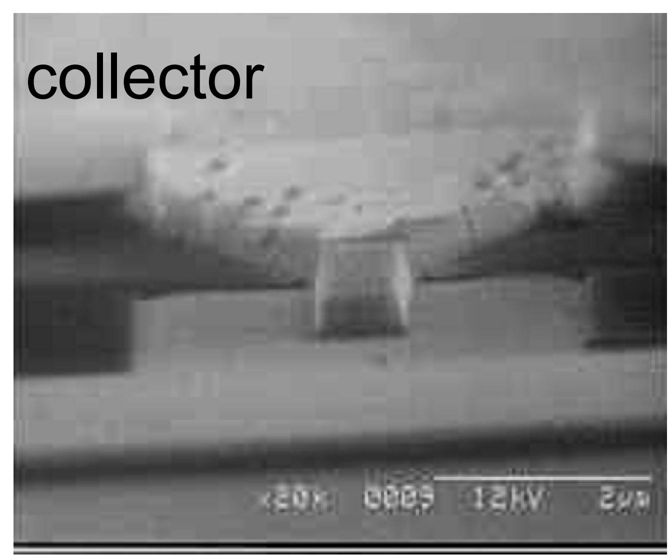
Submicron InAlAs/InGaAs HBTs: Unbounded Unilateral power gain 45-170 GHz

UCSB
ONR
Miguel Urteaga









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Negative Unilateral Power Gain ???

Can U be Negative?

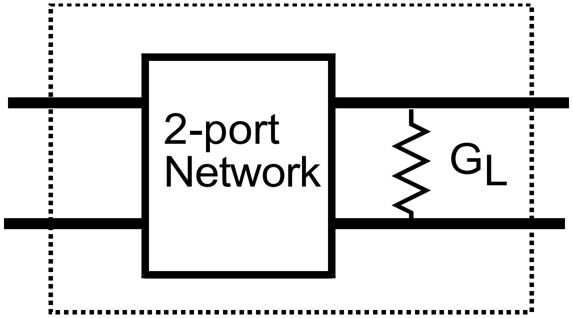
YES, if denominator is negative

This may occur for device with a negative output conductance (G_{22}) or some positive feedback (G_{12})

$$\mathbf{U} = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})}$$

What Does Negative U Mean?

Device with negative U will have infinite Unilateral Power Gain with the addition of a proper source or load impedance



$$\mathbf{U} = \frac{|Y_{21} - Y_{12}|^2}{4[G_{11}(G_{22} + G_L) - G_{21}G_{12}]}$$

Select G_L such that denominator is zero:

$$\mathbf{U} = \infty$$

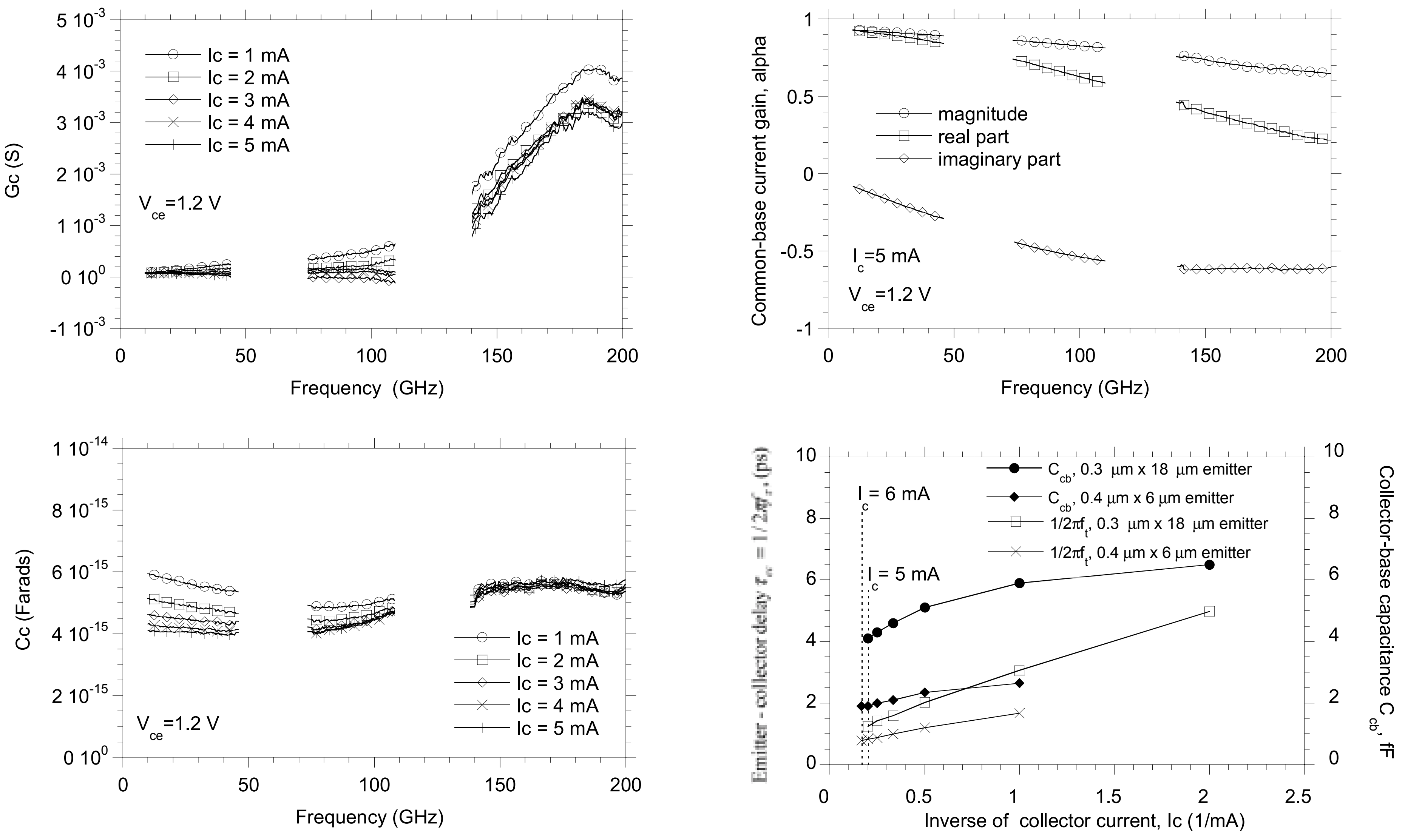
AFTER Unilateralization

- Network would have negative output resistance
- Can support one-port oscillation
- Can provide infinite two-port power gain

Simple **Hybrid- π HBT model will NOT show negative U**

DC-200 GHz parameters of 0.3 μm Emitter / 0.7 μm Collector HBTs:

Miguel Urteaga

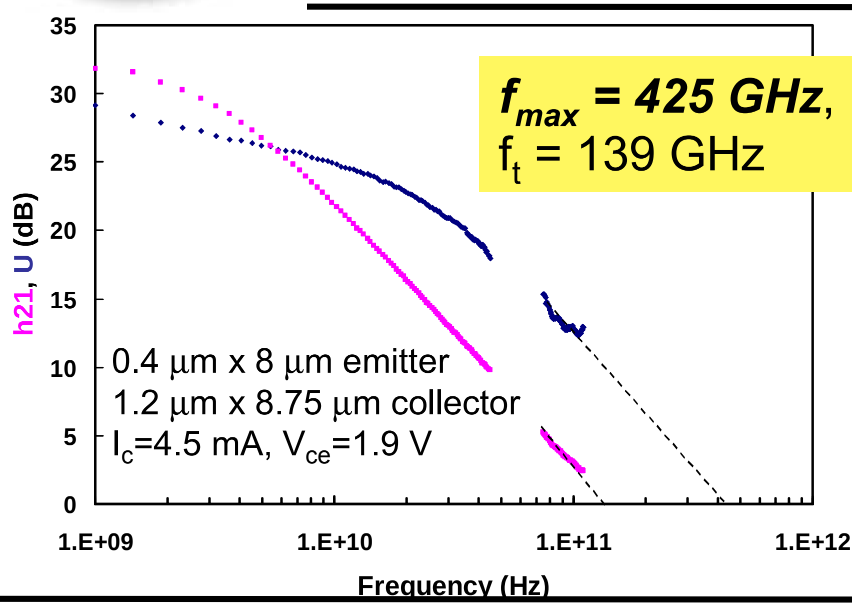


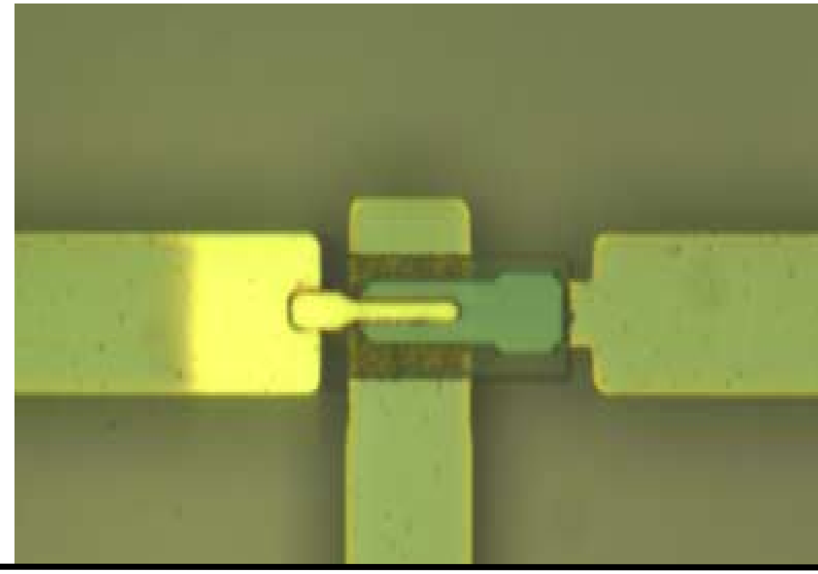
No evidence whatsoever of the postulated base pushout phenomenon of Jäckel et al

(this theory also uses an erroneous hole mobility, error due to calculus derivatives chain rule error)

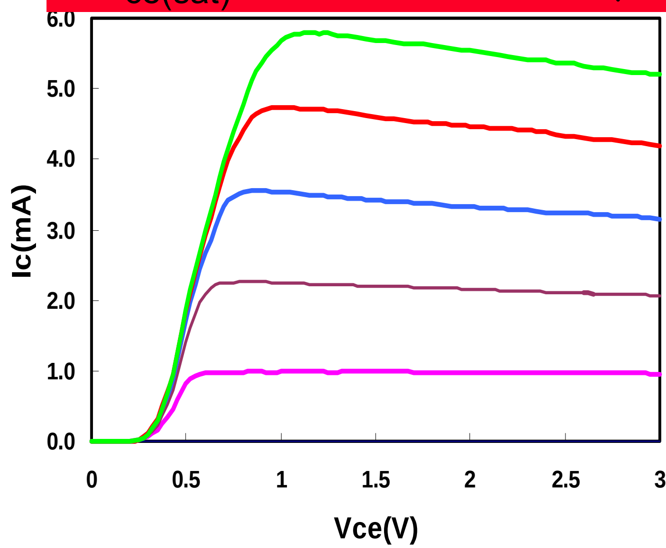
transferred-substrate DHBTs

UCSB
Sangmin Lee

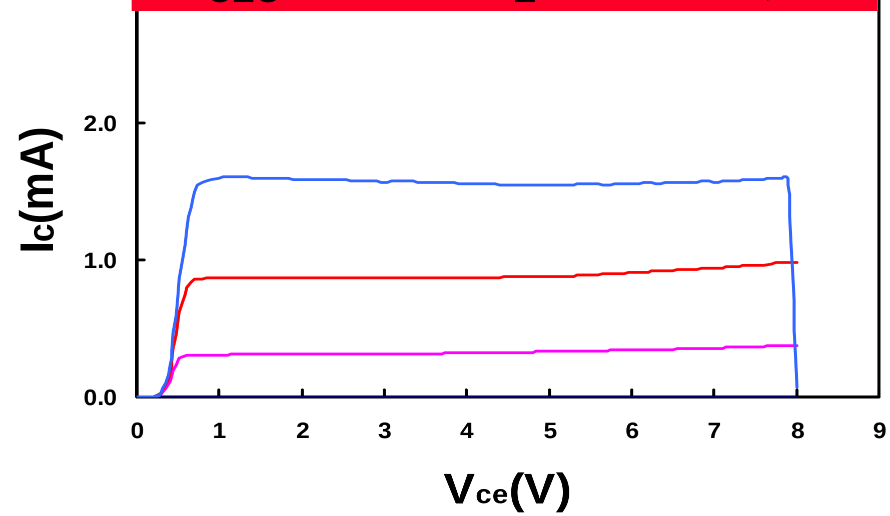




$V_{ce(sat)}$ ~1 V at 1.8 mA/µm^2



BV_{CEO} = 8 V at J_E =0.4 mA/µm^2



much wider bandwidth devices coming soon (we hope…)

UCSB
IQE
Mattias Dahlstrom / Amy Liu

Wideband Mesa InP/InGaAs/InP DHBTs

Walsin
ONR

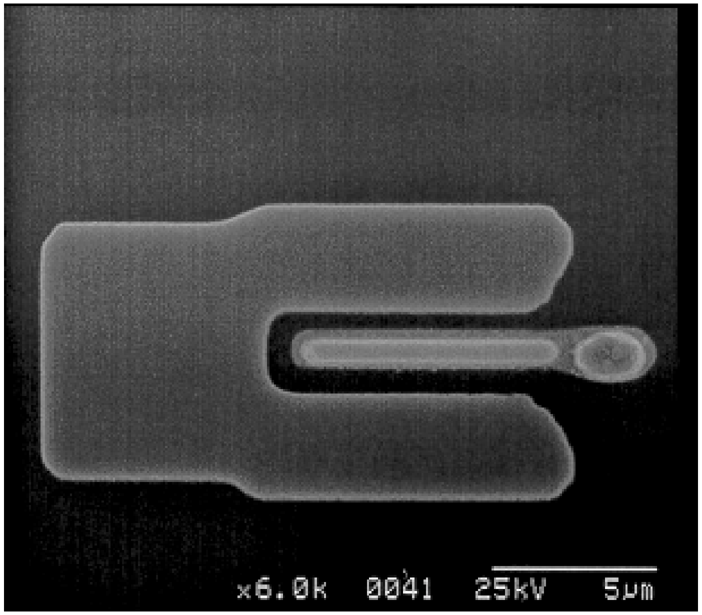
We have obtained high f_t and very high f_{max} in mesa DHBTs with C-doped InGaAs bases

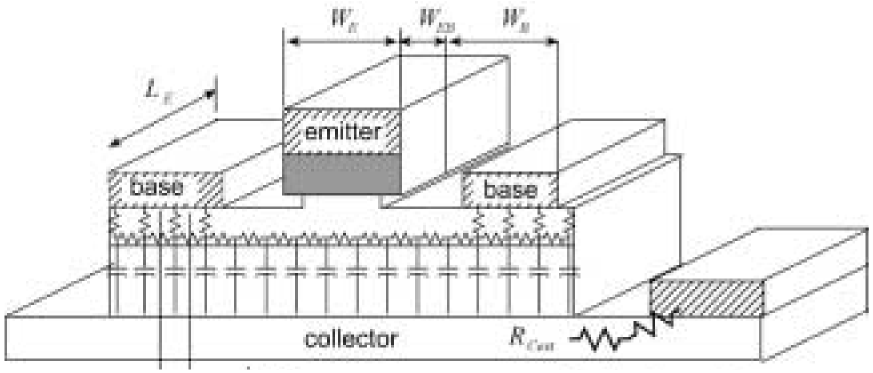
Devices have very narrow base mesas and extremely low base contact resistivity

Unlike transferred-substrate HBTs, which have very low C_{cbx} , these devices have significant extrinsic collector-base junction areas.

→ further effort needed in excess Ccb reduction for >100 GHz digital ICs

Results to be presented soon

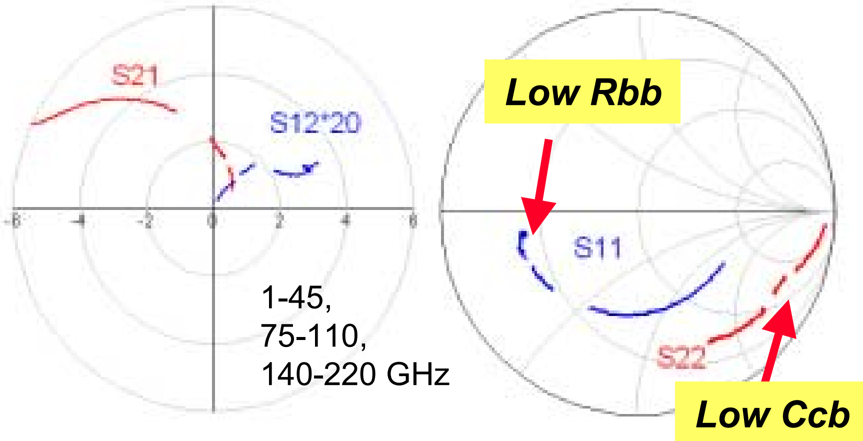




Comparing High-f_{max} HBTs

Miguel Urteaga

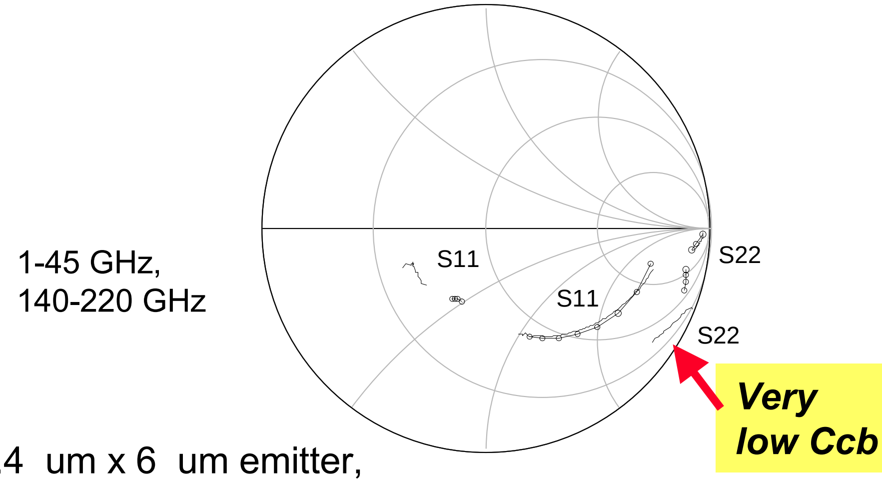
Transferred-Substrate HBT:



0.3 um x 18 um emitter,
0.7 um x 19 um collector. 130 GHz ft, fmax very high

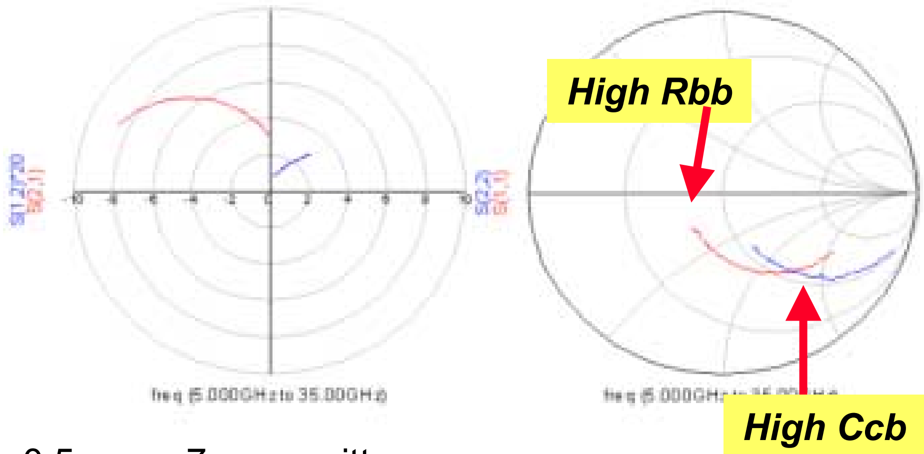
Transferred-Substrate HBT:

Miguel Urteaga



0.4 um x 6 um emitter,
0.7 um x 6.4 um collector. 130 GHz ft, fmax very high

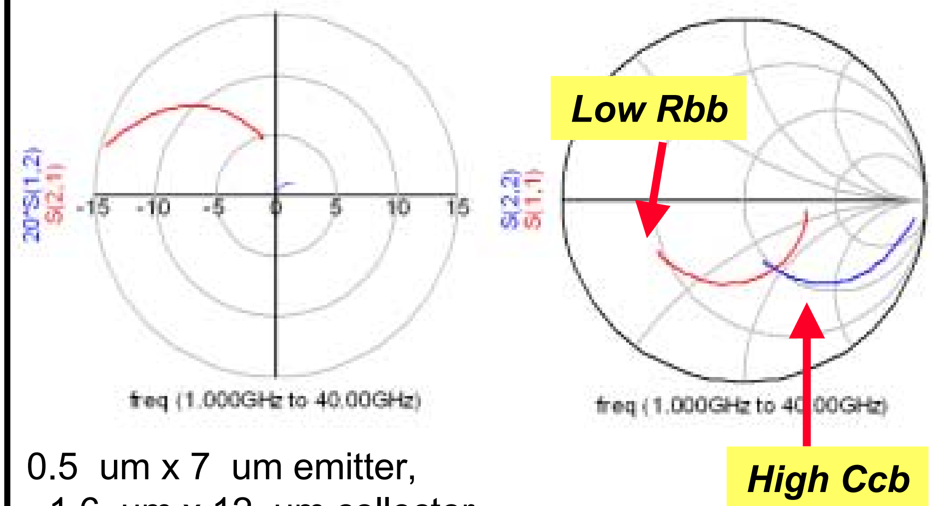
Good (not record) mesa HBT



0.5 um x 7 um emitter,
2.7 um x 12 um collector. 200 GHz ft, 200 GHz fmax

PK Sundararajan

Fast C-doped-base mesa HBT



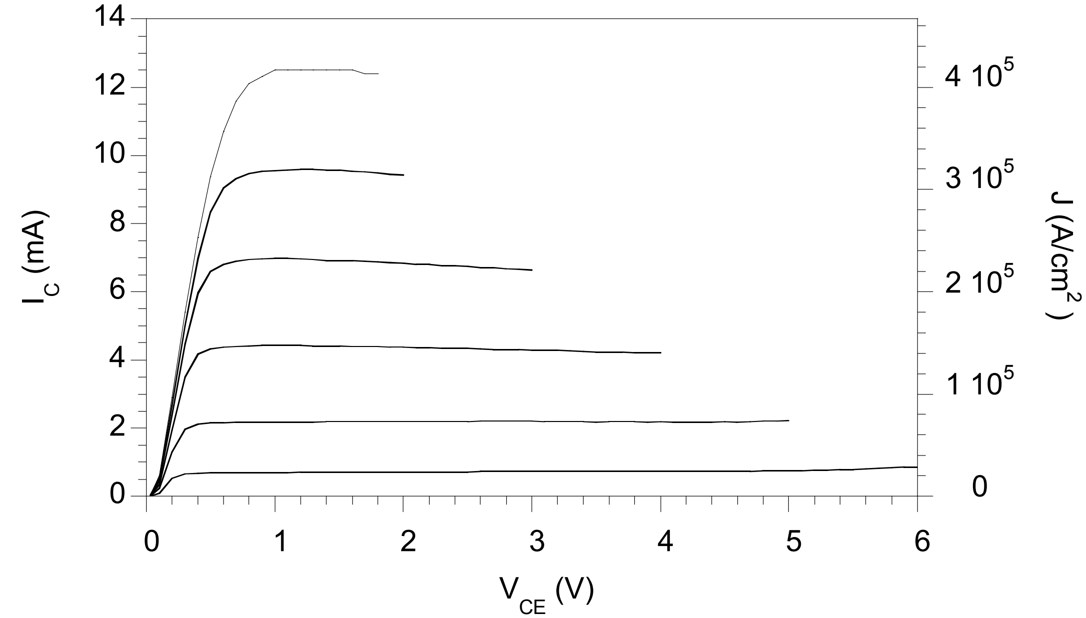
0.5 um x 7 um emitter,
~1.6 um x 12 um collector.
>250 GHz ft, high fmax

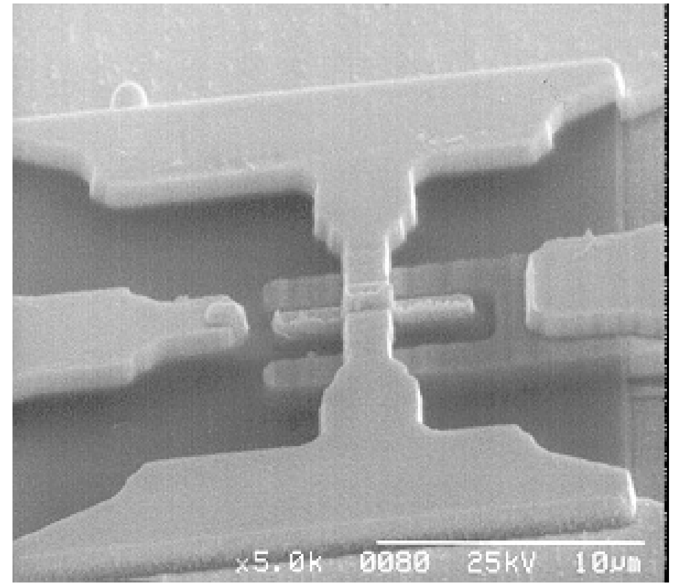
Mattias Dahlstrom

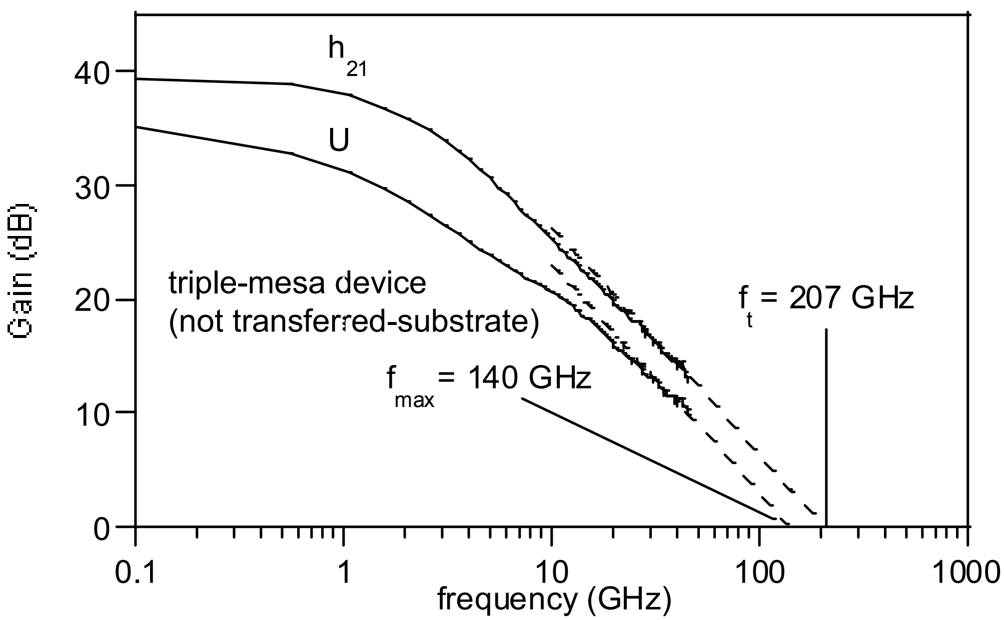
InP/InGaAs/InP *Metamorphic* DHBT ***on GaAs substrate***

UCSB

Young-Min Kim







Growth:
- 400 Å base, 2000 Å collector
- GaAs substrate
- InP metamorphic buffer layer (high thermal conductivity)

Processing
- conventional mesa HBT
- narrow 2 um base mesa, 0.4 um emitter

Results
- 207 GHz f_t, 140 GHz f_{max},
- >6 Volt BVCEO, β=76

IC results

75 GHz HBT master-slave latch connected as ***Static*** frequency divider

UCSB

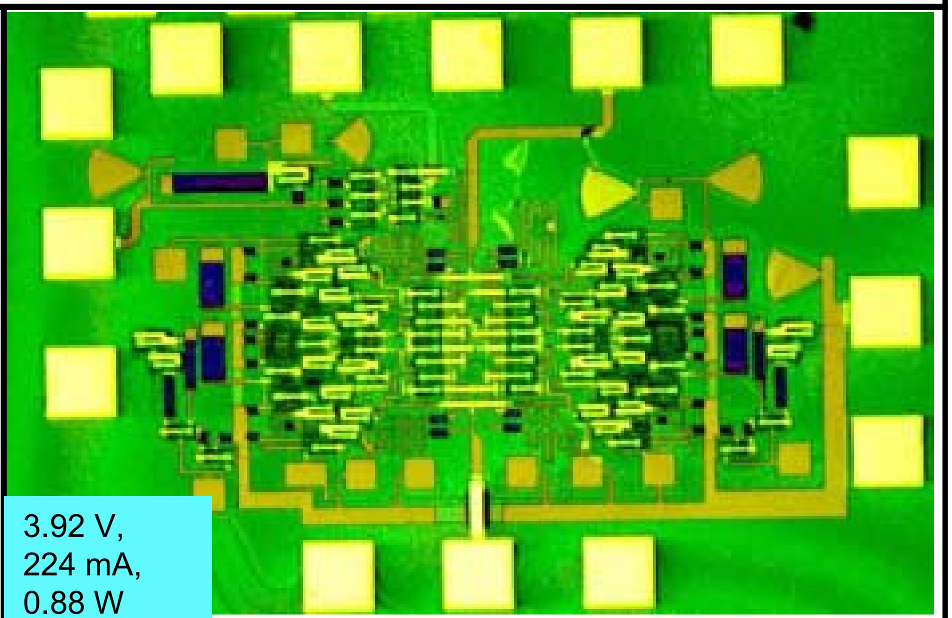
Thomas Mathew
Michelle Lee
Hwe-Jong Kim

technology:

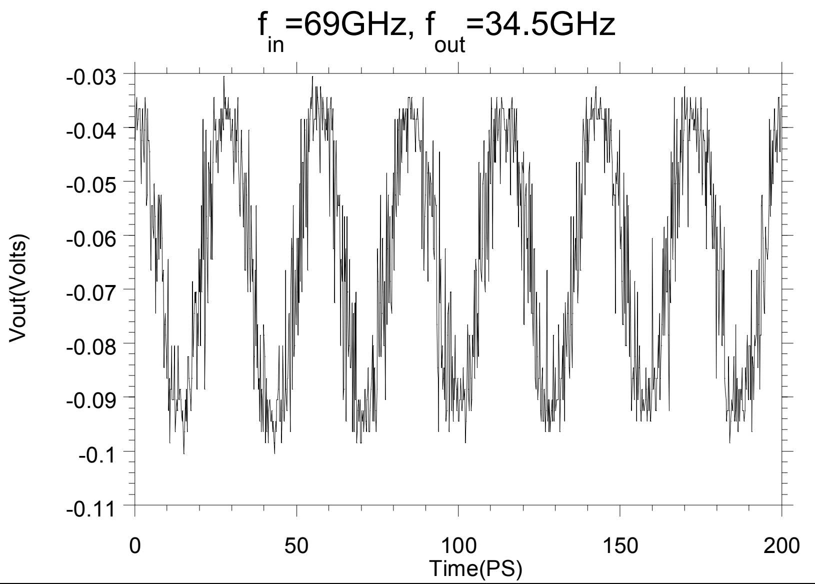
400 Å base, 2000 Å collector HBT
0.7 um mask (0.6 um junction) x 12 um emitters
1.5 um mask (1.4 um junction) x 14 um collectors
1.8×10^5 A/cm^2 operation, 180 GHz ft, 260 GHz fmax

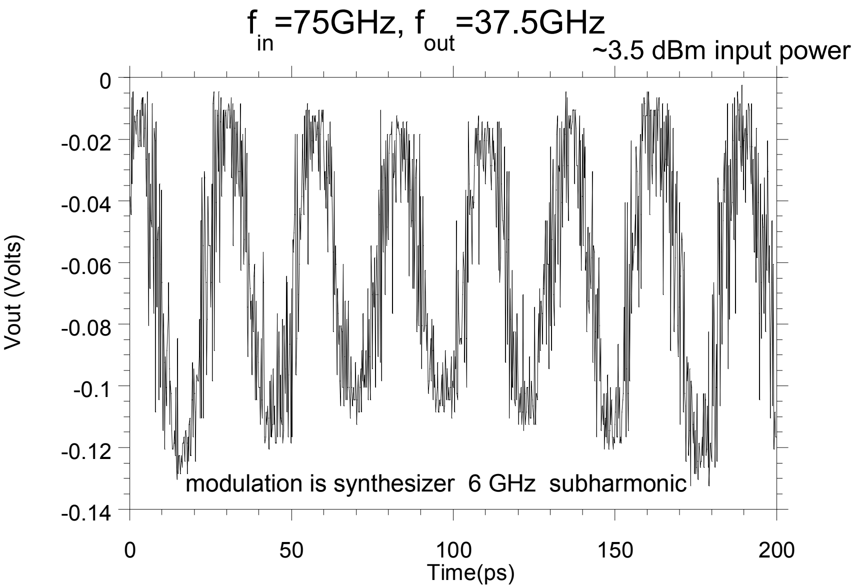
simulations: 95 GHz clock rate in SPICE

test data to date:
tested, works over full 26-40 and 50-75 GHz bands



3.92 V,
224 mA,
0.88 W





18 GHz Σ–Δ ADC

UCSB

S Jaganathan

Design

comparator is 75 GHz flip flop

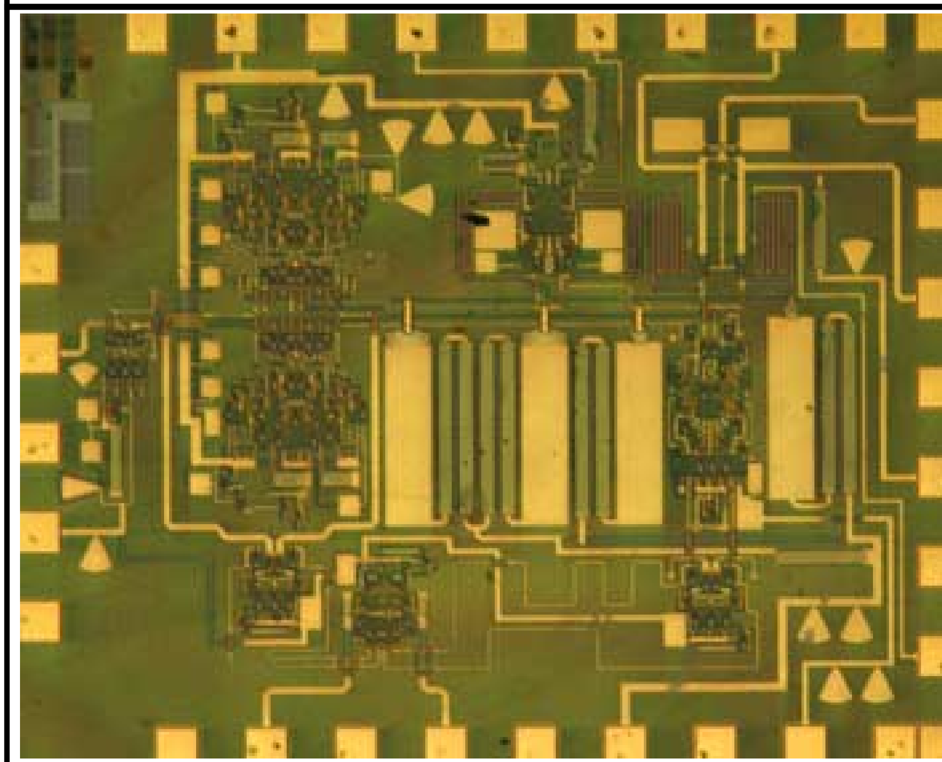
DC bias provided through 1 KΩ resistors

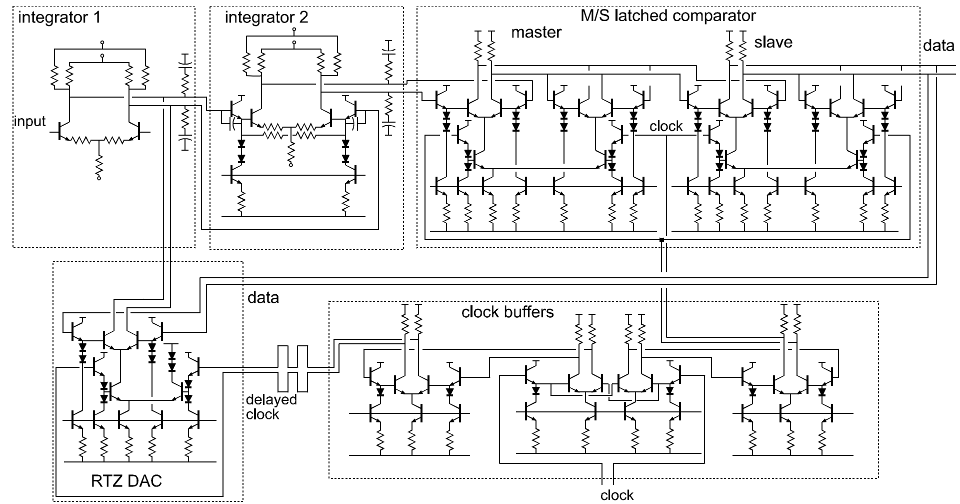
Integration obtained with 3 pF capacitors

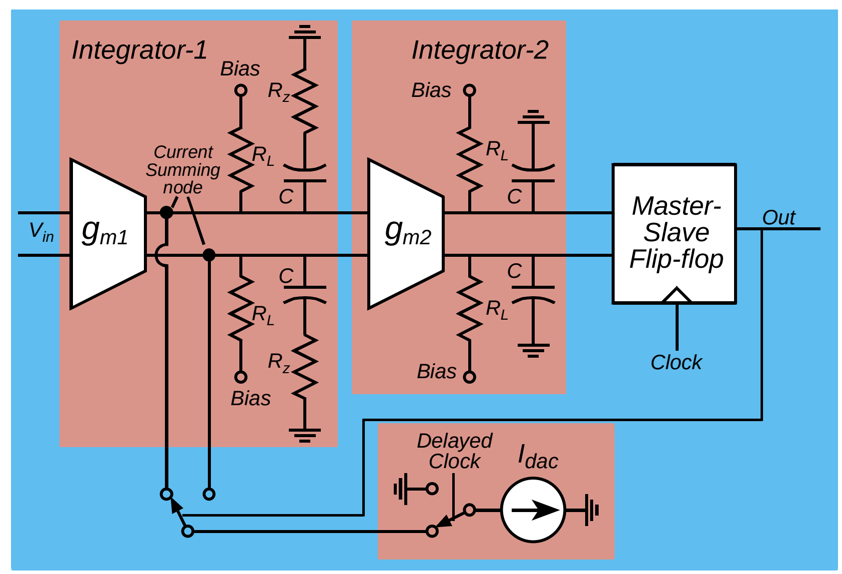
RTZ gated DAC

Integrated Circuit

150 HBTs, 1.2 x 1.5 mm, 1.5 W

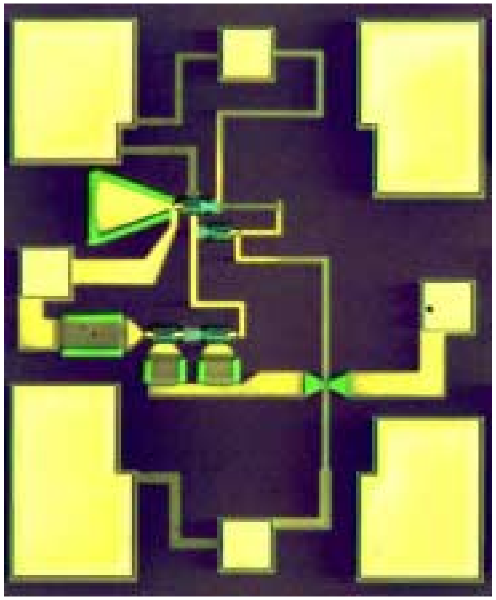




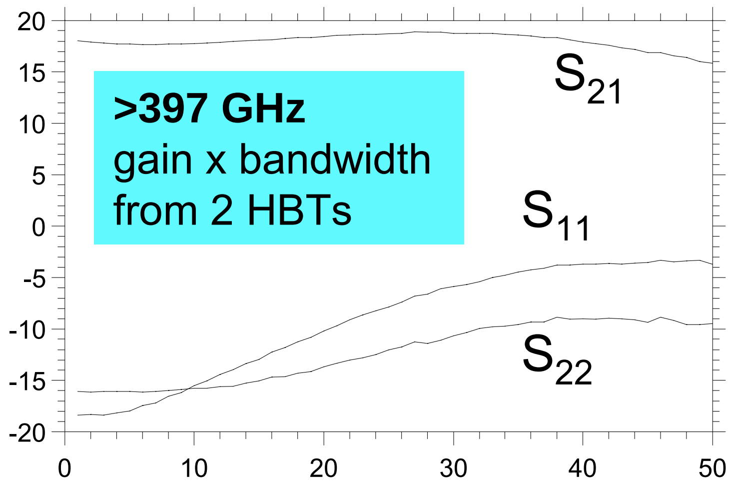


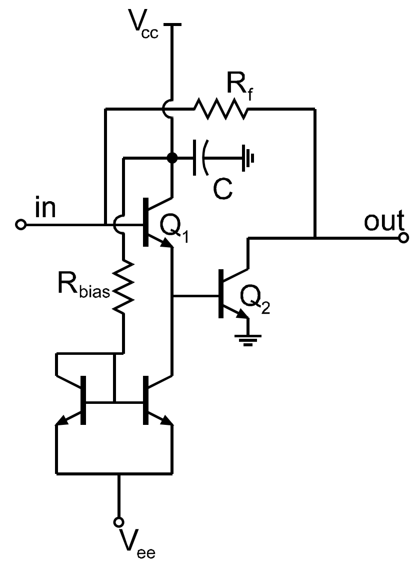
High Speed Amplifiers

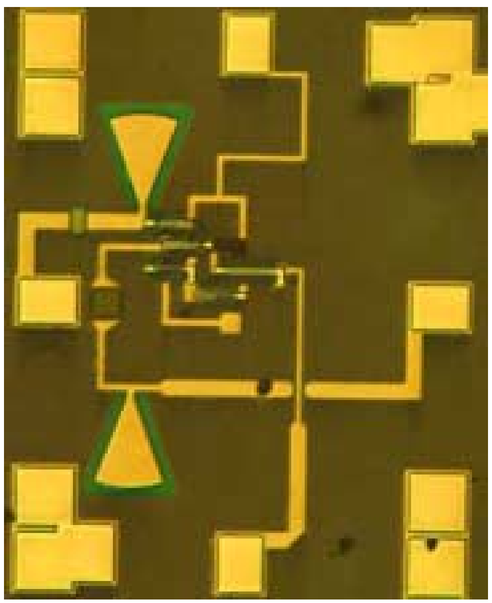
UCSB
Dino Mensa
PK Sundararajan



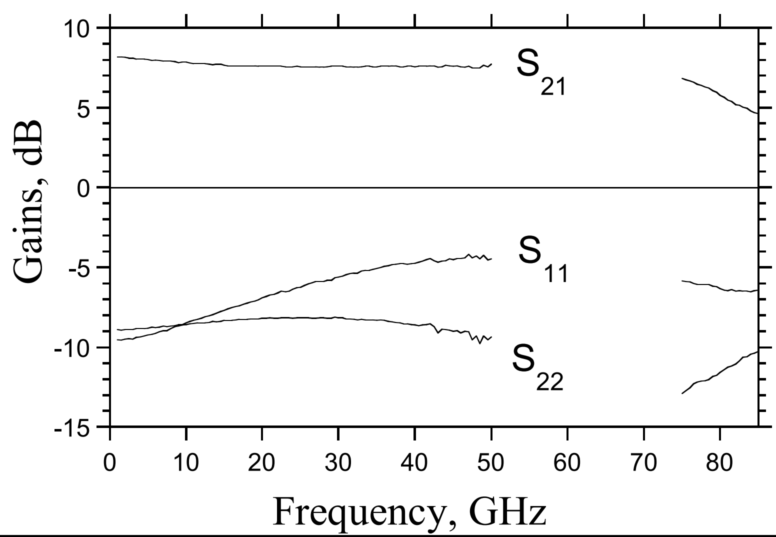
18 dB, DC--50+ GHz

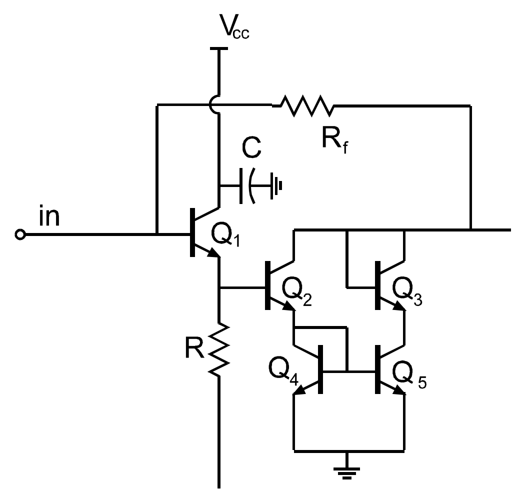






8.2 dB, DC-80 GHz





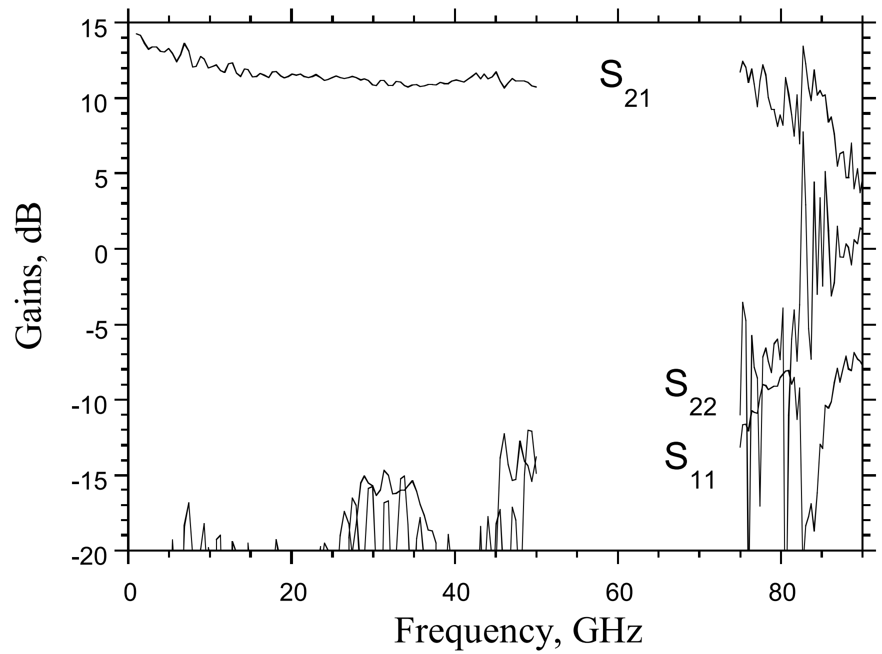
AFOSR

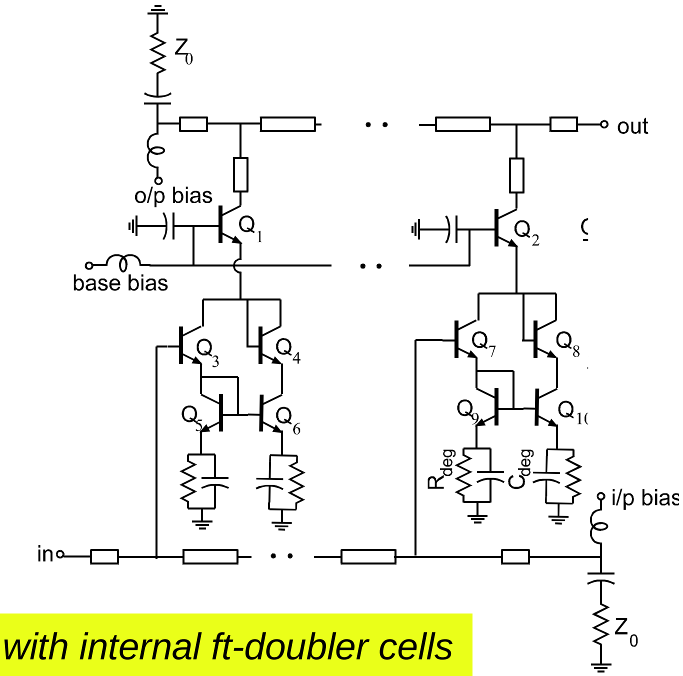
HBT distributed amplifier

11 dB, DC-87 GHz

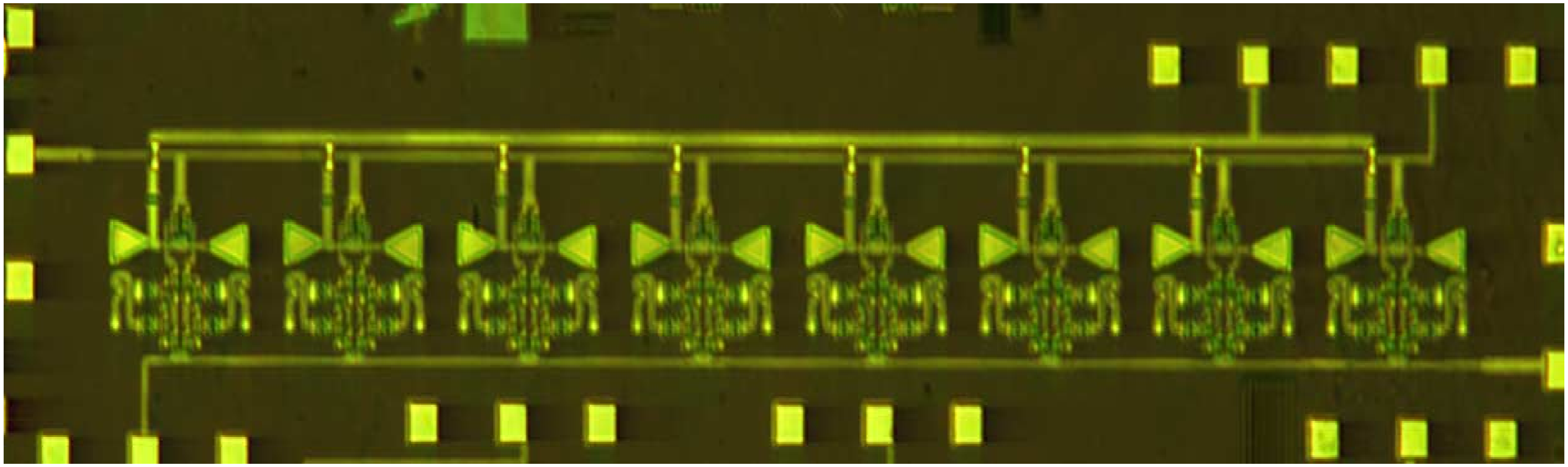
UCSB

PK Sundararajan





TWA with internal ft-doubler cells

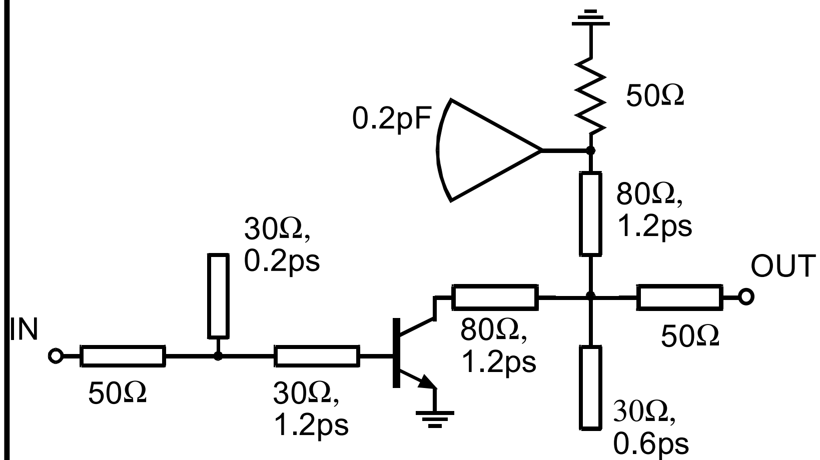


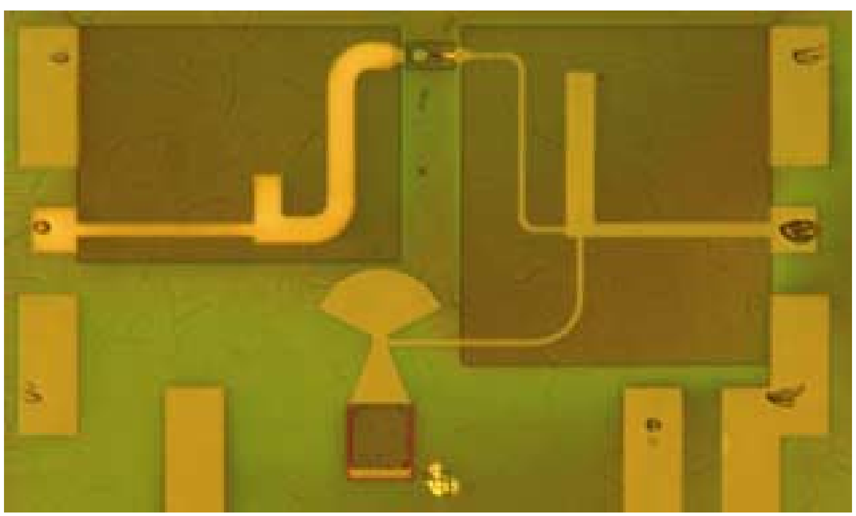
Submicron HBT Program

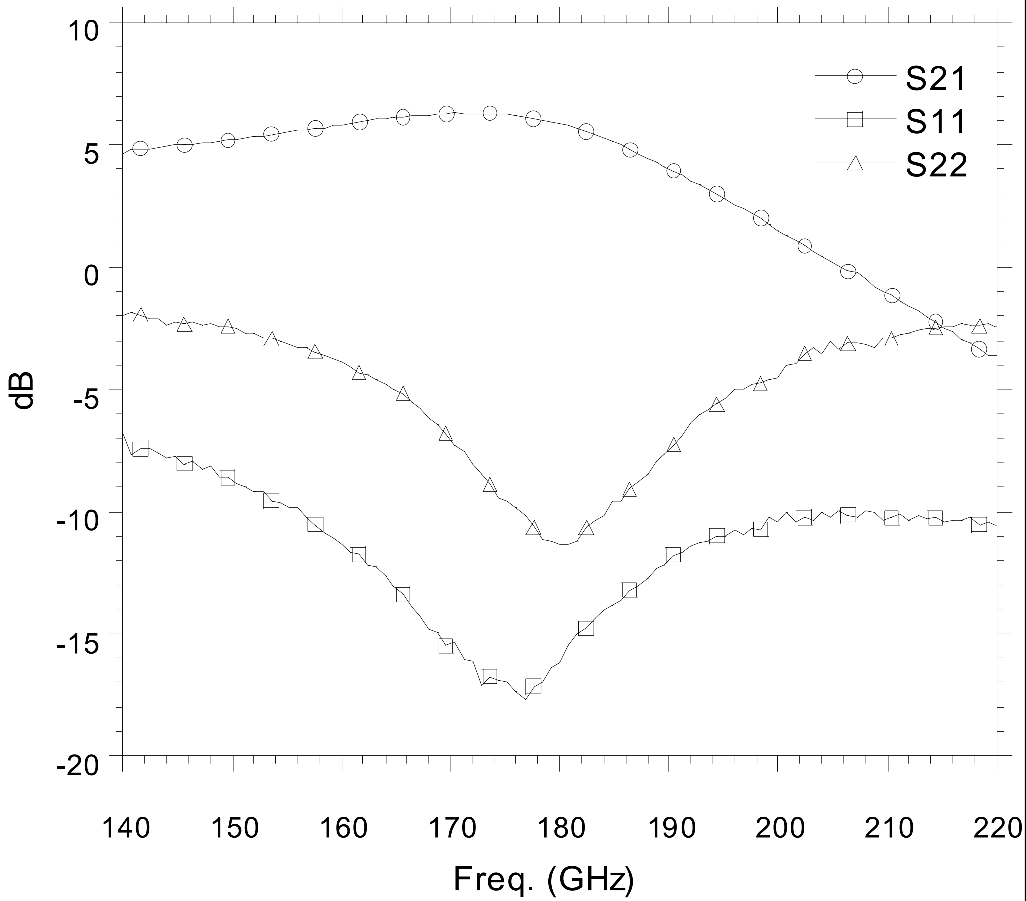
175 GHz Single-Stage Amplifier

UCSB

Miguel Urteaga







6.3 dB gain at 175 GHz

ARO MURI

40 mW, W-band InP DHBT power amplifiers

UCSB

Yun Wei

Objectives: W band, P_{1dB}>9 dBm, P_{sat}>12 dBm

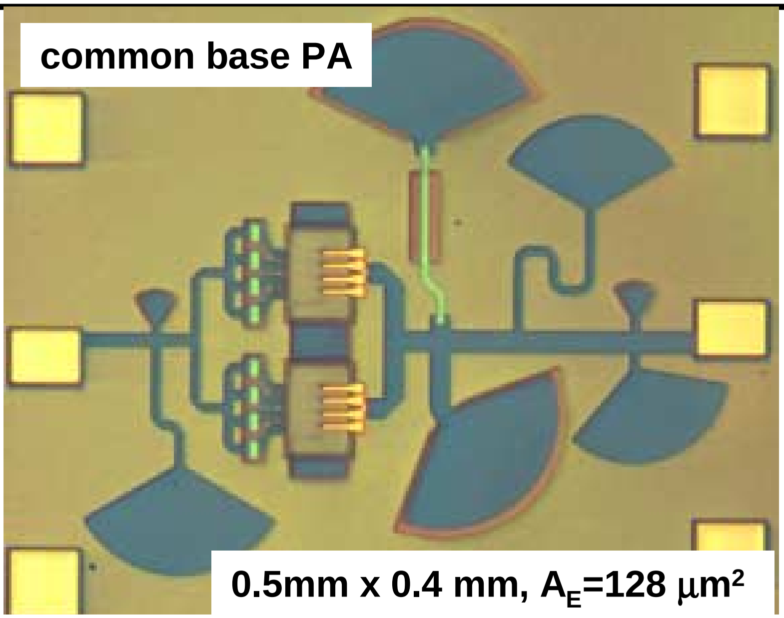
Approach: transferred-substrate InP DHBTs, microwave amplifier design

Simulations: S-parameter and harmonic simulation in ADS

Accomplishments:
f_0=85 GHz, BW_{3dB}=28 GHz,

G_T=8.5 dB, P_{1dB}=14.5 dBm, $P_{sat=}$16dBm

common base PA



0.5mm x 0.4 mm, A_E=128 μm²