INTERCONNECTS IN 50-100 GHZ INTEGRATED CIRCUITS

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Abstract

Integrated circuits operating at greater than 50 GHz face several difficulties imposed by the IC wiring environment. Interconnect impedances are difficult to control in complex ICs, and common-lead ground-return inductance results in inadvertent circuit coupling both on-wafer at the IC-package interface. Substrate electromagnetic resonances limit the maximum IC die size. Microstrip wiring environments using thin spin-cast polymer layers address many of these difficulties. We will describe IC results, including 87 GHz HBT digital ICs and 194 GHz tuned HBT amplifiers.

Introduction

The bandwidth of electronics continues to increase. ICs for 40Gb/s optical fiber transmission are nearing commercial release, and 80-160 Gb/s ICs are an active research topic. Mixed-signal ICs (ADCs and DACs) are migrating towards > 10 GHz sample rates, and monolithic mm-wave ICs (MIMICs) have been demonstrated to 215 GHz. MIMICS use transmission-line tuning networks; interconnects must have low loss and precisely controlled impedance and velocity. Mixed-signal and optical transmission ICs are complex (1000-10,000 transistors), and require a wiring environment which maintains control of signal integrity and has predictable characteristics to enable robust computer-aided design (CAD).

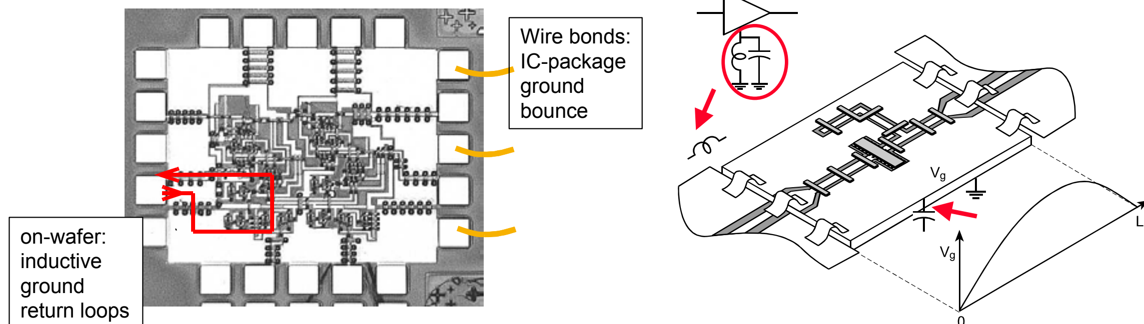

Fig. 1: Difficulties in wiring and packaging of ICs with random or controlled-impedance top-surface interconnects include ground-return inductance on-wafer or in packaging, and parallel-plate substrate modes.

Difficulties with Various Wiring Environments

In low-frequency ICs, electromagnetic characteristics of the wiring are ignored, and circuit nodes are connected by metal lines on the IC top surface without consideration of the interconnect characteristic impedance or delay. These are random interconnects. In contrast, coplanar waveguide (CPW) provides controlled line characteristics for IC top-surface wiring. Microstrip transmission lines are extensively used in MIMICs. Here the IC substrate serves as the wiring dielectric, with the ground plane placed on the IC bottom surface and ground connections provided by through-wafer vias. As first demonstrated in ICs by NTT, thin-film-dielectric microstrip interconnects can also be fabricated on ICs by using wiring and ground planes on the IC top surface, separated by deposited dielectric films of a few microns thickness. Thin-film-dielectric microstrip interconnect environments have key advantages for mixed-signal ICs at > 10 GHz clock frequencies.

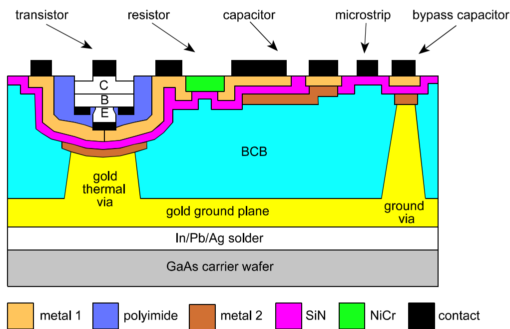

Fig. 2: Transferred-substrate HBT IC cross-section with 5 um thin-film-dielectric microstrip wiring.

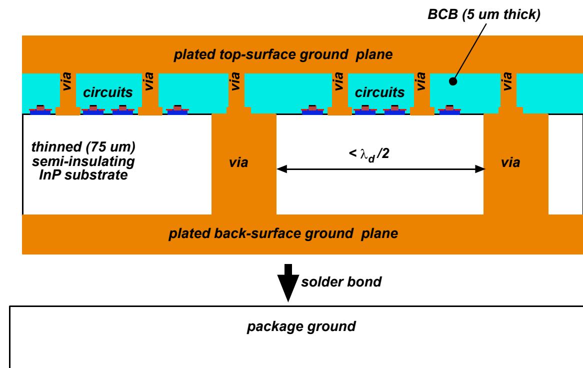

Fig. 3: HBT IC with top-surface thin-film-dielectric microstrip wiring and through-wafer vias for suppression of substrate modes and package ground bounce. Present UCSB ICs employ the upper ground plane but omit the substrate vias.

There are difficulties with both on-wafer propagation and with packaging. With top-surface wiring, wire bonds to the IC pads connect the IC and package grounds. These have ~ 0.3 pH/micron inductance, through which signal ground-return currents must pass, generating a potential difference between IC and package grounds. Signal lines are thus coupled, and signal distorted through ringing. Digital-analog coupling reduces ADC dynamic range, reduces optical receiver sensitivity, and cause PLLs to lock inadvertently to digital switching noise. In amplifiers, IC-package ground inductance degrades gain and can induce oscillation; ground inductance has much greater impact than signal lead parasitic inductance. Common-lead inductance between the IC and package grounds must be very small. Differential connections are only a partial solution, because common-mode rejection ratios are low

Complex CPW ICs face serious packaging difficulties. By bonding the IC to a heat transfer metal surface in the package, a parasitic parallel-plate resonator is created between this surface and the IC top-surface wiring plane. The IC and package grounds are connected at the IC periphery, resulting in c/2nL substrate resonant frequencies. To avoid resonances within the DC-50 GHz bandwidth, the smaller of the two die dimensions must be kept below 0.8 mm. Nonzero bond wire inductance further reduces the resonant frequency.

If the IC substrate is used as the dielectric, microstrip wiring then employs the IC bottom surface as the ground plane. The IC-package ground-ground interface then has minimal length, and a cross-sectional area equal to that of the IC and ~1,000:1 larger than that of a wire bond. IC-package ground bounce is eliminated. While suitable for MIMICs, conventional substrate-dielectric microstrip wiring faces numerous difficulties with on-wafer signal integrity if used in mixed-signal and optical transmission ICs.

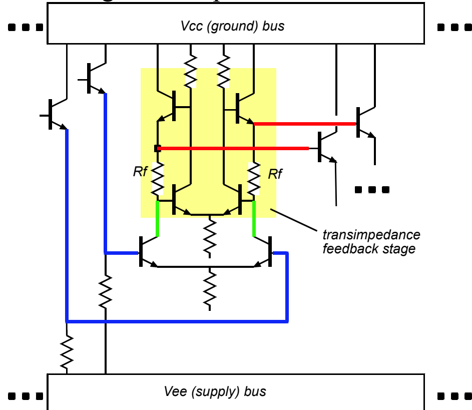

Fig. 4: Typical transconductance-transimpedance amplifiers terminate key interconnects (colored) in alternating low and high impedances, hence are very sensitive to wiring parasitics.

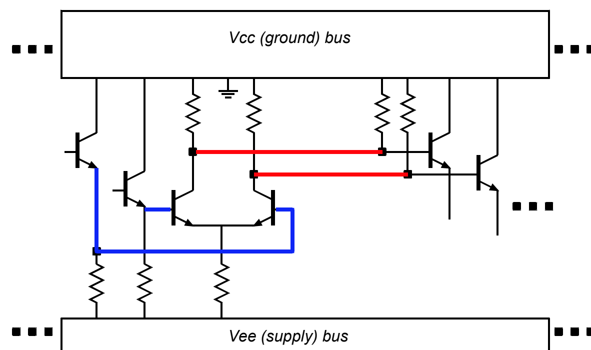

Fig. 5: Simple transconductance-resistance gain stages are readily adapted to terminated line impedances.

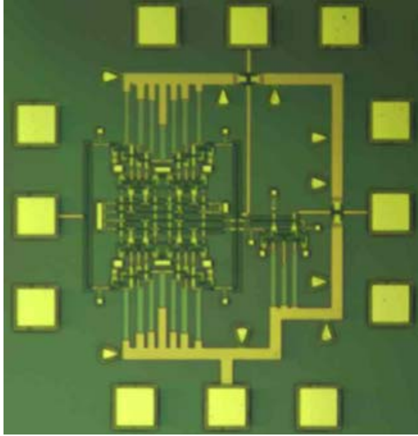

Fig. 6: 87 GHz HBT master-slave latch before ground plane plating.

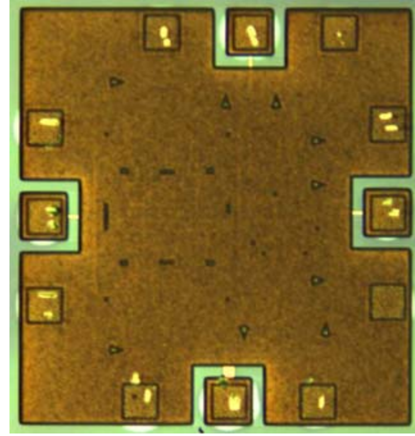

Fig. 7: HBT latch after ground plane plating.

IC wiring also impacts signal integrity for on-wafer connections. For minimal circuit coupling, the IC wiring environment should have minimum inductance in the on-wafer ground system. Long interconnects between circuit blocks have time-of-flight comparable to a bit period, and must be terminated in Zo at source or load. Hence, line impedances must be easily determined from the IC layout. For shorter interconnects, within a circuit block, lines are short and terminated lines not required. Nevertheless, wire inductance and capacitance still have substantial impact upon amplifier gain flatness and logic gate ringing. For success in CAD, line impedances and velocities must be predictable and easily determined from the IC layout even for short interconnects whose time-of-flight is much shorter than a pulse period or length much shorter than a wavelength.

Conventional substrate-dielectric microstrip wiring is not suitable for mixed-signal and optical transmission ICs. While line impedances are well controlled and ground bounce is minimal, via inductance can only be reduced by reducing substrate thickness. Vias for a 100 micron thick substrate have ~10 pH inductance, j6 Ohms impedance at 100 GHz. Lines will strongly couple unless spaced laterally at greater than one substrate thickness. For a 100 micron substrate, interconnects in a complex IC are then strongly coupled, and the Zo of the many interconnects hard to determine. IC fabrication constraints prevent via spacings much smaller than the substrate thickness. To avoid these limitations in complex ICs, microstrip lines must have dielectric thicknesses of less than 10 microns, below that which a semiconductor substrate can be reliably thinned.

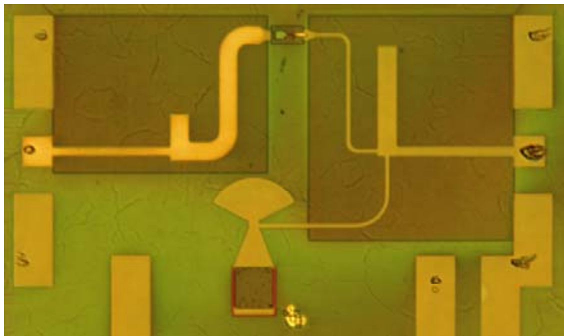

Fig. 8: One-HBT (transferred-substrate) 6.3 dB gain amplifier at 175 GHz

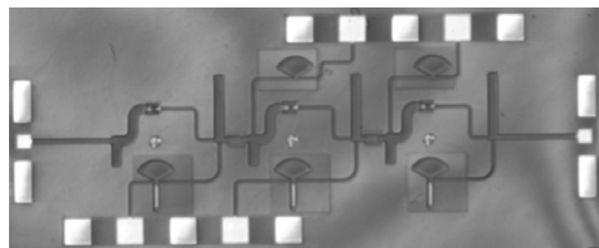

Fig. 9: Three-stage (transferred-substrate) 8.5dB gain amplifier at 195 GHz

Mixed-signal and optical transmission ICs use top-surface wiring, combining random and CPW connections. As each CPW signal line interrupts the ground plane of adjacent CPW lines, CPW can be used only on the long lines between circuit blocks. Interconnects within IC blocks are random, with distant and ill-defined ground returns, line impedances are not well known, and inductance and capacitance of even short interconnects cause IC performance to deviate significantly from design. In one case, a 40 GHz broadband amplifier, introduction of a 100 micron interconnect produced a 1 dB increase in gain peaking per stage. Design discrepancies are reduced by employing circuits that are less sensitive to interconnect characteristic impedance. While transconductance-transimpedance amplifiers provide wide bandwidths, the interfaces alternate between very low and very high impedances, and circuit

response is thus sensitive to the inductance and capacitance even of short interconnects. In contrast, amplifiers with 75-Ohm interface impedances will show well-controlled frequency response in the presence of short interconnects whose Zo is in the range of 50-100 Ohms, and moderate uncertainty in line parameters can be tolerated.

Thin-Film Microstrip Wiring Environments

Thin-film-dielectric microstrip wiring provides controlled-impedance interconnects within dense mixed-signal ICs. The associated ground plane eliminates signal coupling through on-wafer ground-return inductance. The wiring is added to an IC process with the addition of a dielectric layer and ground plane above the IC top-surface wiring planes. The required IC fabrication processes are readily implement; a 5-micron thick Benzocyclobutene (BCB) polymer film is applied by spin casting, vias etched in the BCB, and the top ground plane deposited by metal evaporation. BCB has a low dielectric constant of 2.7, and a 3-micron width conductor has controlled 80-Ohm impedance. Because the dielectric is thin, ground via inductance is greatly reduced. Interconnects are not significantly coupled for > 10 micron line spacings greater than. Ground vias can be closely spaced, as required in complex ICs. There are disadvantages. Given the thin dielectrics, skin loss is much larger than conventional microstrip of similar impedance, and maximum current is proportionally reduced. The ground plane reduces line impedances and increases capacitance, thereby increasing node charging times on unterminated interconnects. .

Thin-film-dielectric microstrip wiring does not reduce the package-IC ground inductance unless the IC is flip-chip bonded to the package. Flip-chip bonding carries difficulties in package thermal design, as the wiring dielectrics are poor thermal conductors. We plan to address packaging by thinning the substrate adding through-wafer vias at $< \lambda_d / 4$ spacing.

IC Results

High-speed integrated circuit efforts at UCSB have included digital, mixed-signal, and optical transmission ICs, with clock rates in the 10-87 GHz range, and millimeter-wave amplifiers in W-band (75-110 GHz) and D-band (140-220 GHz). Demonstrated ICs include 87-GHz digital latches, 20 GHz clock rate oversampled ADCs, and single transistor amplifiers with 6.3 dB gain at 174 GHz. Some ICs were fabricated in an InP-based transferred-substrate heterojunction bipolar transistor (HBT) IC process that incorporates a microstrip IC wiring environment having a thin polymer dielectric substrate, permitting controlled-impedance interconnects within complex ICs. Other ICs were fabricated in a conventional mesa fabrication process, although this again employs thin-dielectric microstrip wiring. In design of these ICs, circuit simulations include the parameters of all interconnects . Because the interconnects are microstrip lines with minimal line-line coupling, line parameters are directly determined from the known conductor widths and lengths. Interconnect electromagnetic simulation from the IC mask layout is required only for mm-wave tuned amplifier designs, wherein matching network impedances must be closely modeled for accurate control of the amplifier passband

Conclusions

Simple 10-200 GHz MIMICs are adequately served by conventional through-substrate microstrip wiring. In contrast, > 50 GHz ADCs, DACs, and optical fiber ICs combine high signal frequencies with high circuit complexity and density, and improved wiring systems are required. On-wafer thin-film-dielectric microstrip wiring addresses on-wafer wiring requirements for such ICs, while the IC-package interface may, among other method, be addressed though use of through-wafer vias placed on a grid at < 500 microns separation.

Acknowledgments

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