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Submicron InP Bipolar Transistors: Scaling Laws, Technology Roadmaps, Advanced Fabrication Processes

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Despite the superior integration scales of CMOS, bipolar ICs continue to find applications in 10-40 Gb/s and higher optical transmission systems, in RF/microwave transceivers, and in high-frequency ADCs and DACs. InP and SiGe heterojunction bipolar transistors (HBT) presently compete for the highest-frequency applications.

As compared to SiGe, InP HBTs offer ~ 4:1 larger collector electron velocities, ~6:1 smaller base sheet resistance, and ~5:1 larger (breakdown$\times f_\tau$) product. SiGe processes are much more highly scaled in both junction dimensions (0.2 μm vs. 1 μm emitter junction widths) and in current density (100 vs. 1000 kA/cm^2), while the extensive use of polycrystalline semiconductor regrowths over buried dielectric spacer layers provides much better reduction of the extrinsic base and emitter resistances and the extrinsic collector-base capacitance. Digital circuit speed is therefore comparable in the two technologies. SiGe HBT processes are more nearly planar than InP, and submicron emitters are formed not by semiconductor etching but by semiconductor regrowth. For these reasons SiGe HBT processes exhibit much higher yield (hence lower IC cost) than InP in the high-volume fabrication of large ICs, although InP is cheaper than high-end SiGe in lower-volume production due to the simpler fabrication facilities required.

Transistor bandwidths are increased through either scaling or through improved semiconductor transport characteristics. Historically, gains in SiGe HBT and CMOS performance were obtained through aggressive scaling, while III-V (GaAs and InP) devices have relied upon superior electron transport and employ large (1-2 μm) device dimensions. For 50-200 GHz operation, III-V HBTs must also be scaled to submicron dimensions. Additionally, transistor development must be guided by IC performance, rather than by the figures of merit of current-gain (f_τ) and power gain ($f_{\max}$) cutoff frequencies. Critical factors for optical fiber ICs and logic are low emitter access resistance, moderately low base resistance, and very high ratio of current to depletion-layer capacitances.

We have developed scaling laws which describe the adjustments in HBT parameters required for a balanced and proportional improvement in device bandwidth in an arbitrary circuit [1,2]. For each 2:1 improvement in bandwidth, the collector layer must be thinned 2:1, the base thinned $\sqrt{2}$:1, the emitter current density increased 4:1, and the emitter resistance per unit area reduced 4:1. Emitter and collector junction widths must both decrease 4:1. If the base contacts lie above the active collector-base junction, the contact width and the contact resistivity must both also decrease 4:1; in device structures where the contacts do not lie above the collector-base junction, the contact width and contact resistivity can remain unscaled. Scaling rates can be relaxed with appropriate material or process improvements: emitter current density can be proportionally reduced if the ratio of collector to emitter junction areas is reduced, while emitter and collector junction widths can be increased if the base contact resistivity is reduced more rapidly than is stated in the scaling laws above. Based upon these scaling laws, Table 1 summarizes the key device parameters required for operation of InP HBTs at 40, 80, and 160 Gb/s, as determined by computing [2] the maximum frequency of a master-slave latch, the key digital building block in the MUX/CMU and DMUX/CDR.

Past efforts in InP HBT scaling at UCSB have focused on the transferred-substrate HBT, for which have devices with emitter dimensions as small as 0.2 μm . These exhibit extremely high power gains at very high frequencies (6-12 dB power gain at 200 GHz), but are difficult to fabricate. Further, the transferred-substrate structure does not adequately address current density or emitter resistivity scaling. We have demonstrated very high gain mm-wave amplifiers using transferred-substrate HBTs, including a single-HBT amplifier with 6.3 dB gain at 175 GHz. With more conventional mesa InP HBTs, we have obtained 280 GHz f_τ, > 450 GHz $f_{\max}$, and 7.5 Volt breakdown [3], and have demonstrated both 87 GHz fully static frequency dividers [4] and 10-GHz clock-rate $\Delta-\Sigma$ ADCs.

Such mesa HBTs cannot produce either the deep submicron junction scaling or the large-scale integration now obtained in SiGe. Present HBT efforts at UCSB are therefore now focused development of an InP HBT process flow and device structure closely modeled on that of the SiGe device [5]. Our first results in this effort include InAlAs/InGaAs/InP DHBTs having narrow emitter junctions and wide and low-resistance polycrystalline InAs extrinsic emitters formed by MBE regrowth over patterned silicon nitride masking layers.

References

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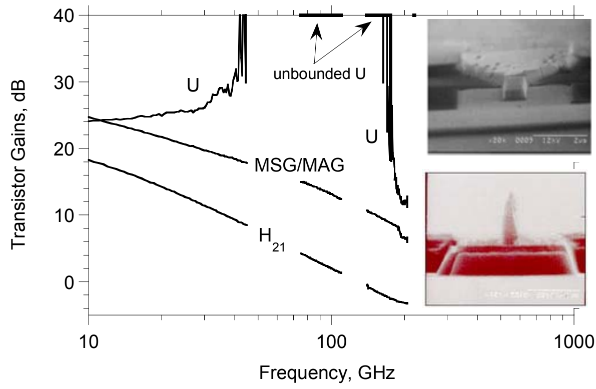

Fig. 1 : Measured mm-wave gains of a InAlAs / InGaAs / InGaAs deep submicron transferred-substrate HBT.

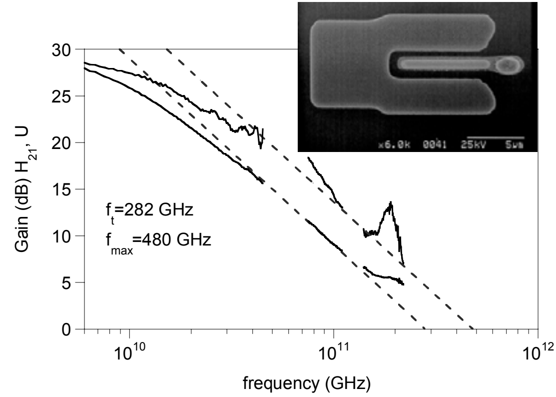

Fig. 2: Measured mm-wave gains of an InP / InGaAs / InP mesa DHBT with a carbon-doped InGaAs base.

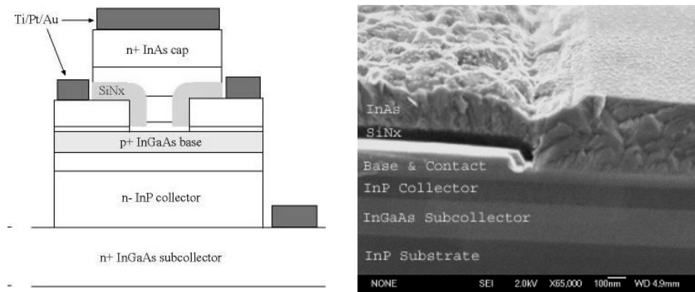

Fig. 3: Schematic cross-section and SEM of InP DHBT with a monocrystalline emitter and polycrystalline InAs extrinsic emitter.

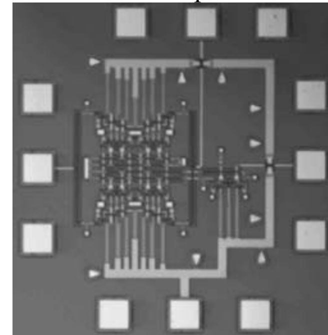

Fig.4: 87 GHz master-slave latch in the InP mesa HBT process

Parameter	Generation 1	Generation 2	Generation 3
Simulated MS-DFF speed	62 GHz	125 GHz	237 GHz
Emitter Junction Width	1 μm	0.8 μm	0.2 μm
Parasitic Resistivity	50 Ω-μm^2	20 Ω-μm^2	5 Ω-μm^2
Base Thickness	400Å	300Å	250Å
Doping	4 10^{19} /cm^2	6 10^{19} /cm^2	8 10^{19} /cm^2
Sheet resistance	750 Ω	700 Ω	700 Ω
Contact resistance	150 Ω-μm^2	20 Ω-μm^2	10 Ω-μm^2
Collector Junction Width	3 μm	1.6 μm	0.4 μm
Collector Thickness	3000 Å	2000 Å	1000 Å
Current Density	1 mA/μm^2	2.3 mA/μm^2	9.3 mA/μm^2
$A_{collector}/A_{emitter}$ (area ratio)	4.55	2.6	2.6
f_τ	170	260	500
f_{max}	170	440	1000
C_{cb} / I_c	1.7 ps/V	0.63 ps/V	0.31 ps/V
$C_{cb}\Delta V_{logic} / I_c$	0.5 ps	0.19 ps	0.093 ps
$R_{bb} /(\Delta V_{logic} / I_c)$	0.8	0.65	0.52
$C_{je}(\Delta V_{logic} / I_C)$	1.7 ps	0.72 ps	0.18 ps
$R_{ex} /(\Delta V_{logic} / I_c)$	0.1	0.15	0.15

Table 1: Technology roadmap for the migration of InP HBT technology from 40 Gb/s through 80 and 160 Gb/s operation.

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