40 GHz MMIC Power Amplifier in InP DHBT Technology

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Abstract

We report a 40 GHz MMIC power amplifier in InP DHBT technology that exhibits 14 dBm output power at 1 dB gain compression and 17 dBm saturated output power with 4 dB associated gain. The small-signal power gain is 6.8 dB, the input return loss is less than –20 dB and the output return loss is less than -6 dB. The peak power added efficiency is 12.5%.

I. Introduction

Ka band power amplifiers have been broadly applied in satellite communication systems, wireless LANs, local multipoint distribution system, personal communications network links, and digital radio.

Although single heterojunction bipolar transistors (SHBT) have demonstrated high linearity and current density, the low breakdown voltage limits output power [1]. We have recently reported 0.5 um InP double heterojunction transistors (DHBT) in transferred-substrate technology having 7-volt collector breakdown voltage (BV_{CEO}) and 425 GHz maximum oscillation frequency (f_{max}) [2]. In the same process, multi-finger [3] DHBTs with emitter area of 16 um^2 per finger have been developed. These DHBTs exhibit 330 GHz small signal f_{max} at 100 mA bias current and 8 V breakdown at low current [4].

Here we report 40 GHz power amplifier employing this multi-finger DHBT. The amplifier achieves 6.8 dB power gain and 14 dBm output power at 1dB gain compression. The saturation output power is 17 dBm with a corresponding power gain of 4 dB and the peak power added efficiency is 12.5%. The die area of the power amplifier is only 0.6mm x 0.7 mm.

II. Circuit design and fabrication

The amplifier is designed in the Cascode topology, taking advantage of the DHBT's high breakdown voltage. Thermal stability is a major design concern. As shown in Fig.1, in the multi-finger Cascode each emitter finger of the common base device is connected to only a single collector finger of the common emitter device. In this thermally-stable Cascode configuration [5,6], stability against current-hogging by a single emitter finger is ensured with less emitter ballasting than is required for a common-emitter HBT operating at the same collector bias voltage. Emitter ballast resistance nevertheless significantly reduces gain. Gain degradation due to parasitic layout impedance of the base bypass capacitor is a major difficulty in Cascode amplifier design. Even a very small parasitic inductance in the bypass capacitor results in significantly reduced gain. The emitter finger spacing is 7 um, with results in negligible thermal coupling between fingers [7].

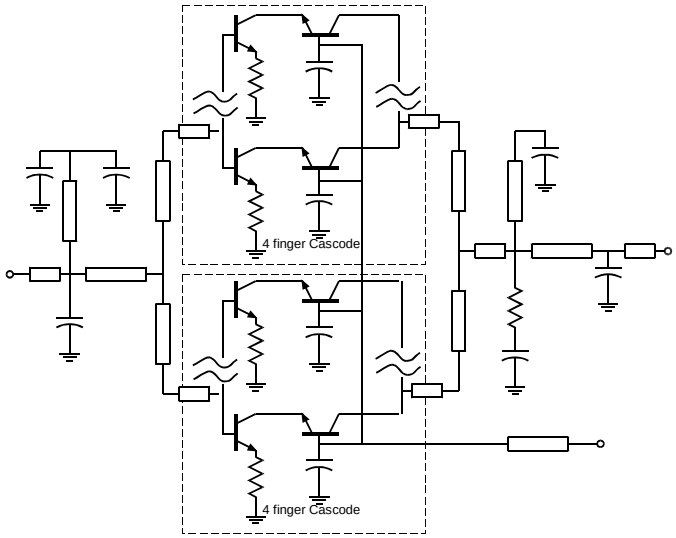

Fig.1: Cascode power amplifier circuit schematic

The 40 GHz power amplifier employs two parallel multi-finger Cascodes. Each multi-finger Cascode consists of 4 emitter/collector fingers. Each emitter finger has a contact size of 1um x 16um and the corresponding collector area is 2um x 20um. The two parallel 4-finger Cascode topology is chosen for two reasons: First, the low input and output impedances of each Cascode are pre-matched through their interconnecting microstrip lines. This eases design of the amplifier's matching networks. Second, by reducing the size of the multi-finger transistor from 4 to 8 fingers, reduced lengths are obtained for the wires interconnecting emitter and

collector fingers within the multi-finger cell. This is a key advantage in computer-aided design, as layout parasitics within the multi-finger cell are electrically significant yet difficult to model with finite-element CAD tools. The longer wires connecting the two 4-finger cells into an 8 finger transistor are microstrip lines with negligible line coupling, and are readily and accurately modeled.

The input network matches the transistor to 50 Ohms using an inductive microstrip line and MIM radial stub capacitors. A large shunt AC-grounded resistor connected to the Cascode output provides unconditional stability. In the output matching network, a shunt AC–grounded inductive microstrip line compensates the HBT output parasitic susceptance arising from the base-collector capacitance, and a low-impedance quarter-wave transformer transforms the 50 Ohm load to the HBT maximum-saturated load impedance:

$$R_L = (V_{CE,\max} - V_{CE,sat}) / I_{C,\max}$$

The maximum DHBT current is $I_{C,max}$ =128 mA with $V_{CE,sat}$=1.2 V, while a maximum collector emitter voltage $V_{CE,max}$=6.5 V< $V_{CE,breakdown}$ is selected as the dynamic operating range to avoid risk of device destruction.
The expected class-A saturated output power is approximately:

$$P_{\max} = I_{\max}(V_{CE,\max} - V_{CE,sat})/8 = 80\,\mathrm{mW}$$

The IC employs two types of MIM capacitors, with higher-capacitance devices using 0.4 μm Si_3N_4 dielectric and lower-capacitance capacitors to ground using the 5 μm BCB microstrip wiring dielectric. The SiN capacitors have much larger capacitance per unit die area, but have substantially larger processing variability due to variations in the thickness of the deposited dielectric film. Parallel combinations of the two, with capacitances appropriately partitioned between the SiN and BCB elements, result in a compact IC layout with reduced processing variability.

III. Measurement and results

Small signal measurements were performed on-wafer on an HP8150 network analyzer with on-wafer TRL calibration. Saturated power measurements were also performed on-wafer using micro-coaxial wafer probes. Reported power measurements include corrections for the known attenuation of bias tees, probes, and cables.

The amplifier die (Fig.2) is 0.7 mm ×0.6 mm. The circuit is biased at I_C =80 mA with 3.5 Volts V_{CE} applied to the common-base device and 1.5 Volts V_{CE} to the common emitter. The power supply is thus 5 V. Fig. 3 shows the small-signal S-parameter measurements. The small-signal power gain is 6.8 dB, the input return loss is better than –20 dB and the output return loss is better than -6 dB. Low S_{22} is not expected in power amplifiers, unless the balanced configuration is employed. The 3 dB bandwidth of S_{21} is 16 GHz. Fig. 4 shows 40 GHz saturated power measurements. The output power at 1 dB gain compression is 14 dBm, while the saturated output power is 17 dBm with a corresponding 4 dB gain. The peak power added efficiency is 12.5% when the amplifier is operating close to full power saturation.

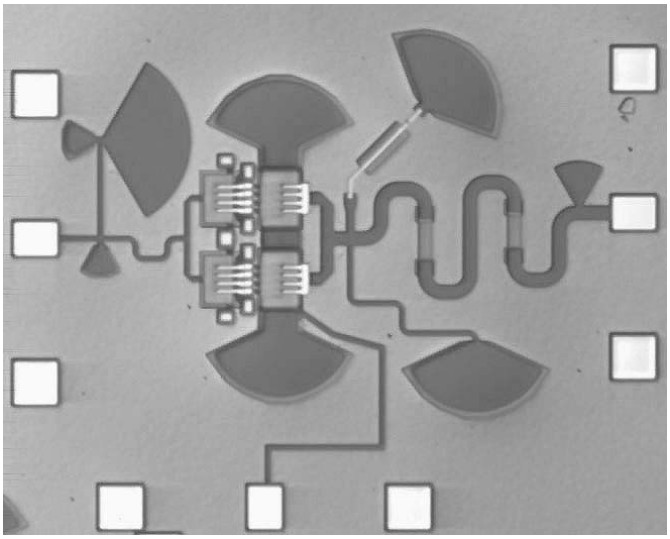

Fig.2: Amplifier die photograph

IV. Conclusion

We report a 40 GHz MMIC power amplifier in InP DHBT technology that exhibits 6.8 dB power gain and 14 dBm output power at 1 dB compression. The saturation output power is 17 dBm (50 mW) while the peak power added efficiency is 12.5%. Future work will seek to extend these results to higher power levels at higher frequencies.

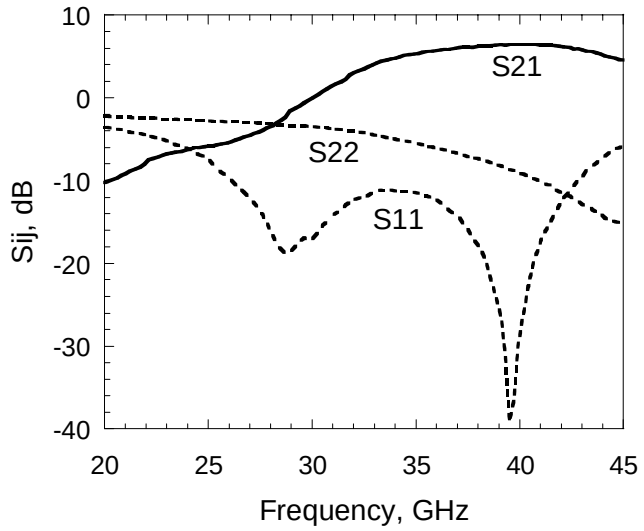

Fig.3: Amplifier small-signal gain-frequency characteristics

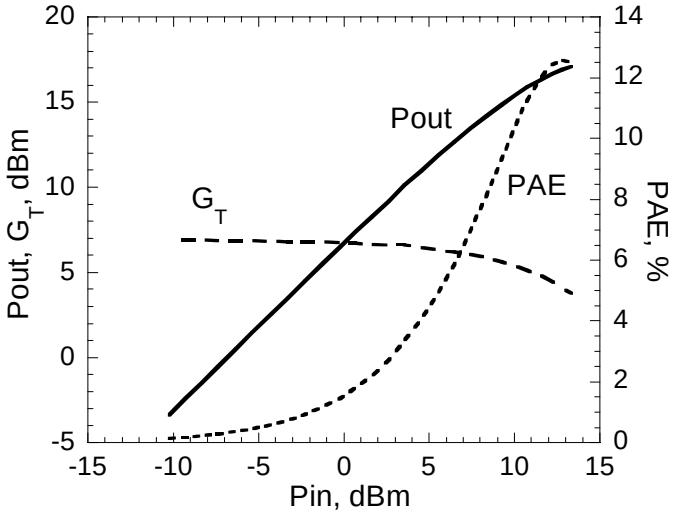

Fig.4: Amplifier saturated power characteristics

References

[1] Rodwell, M.; Lee, Q.; Mensa, D.; Guthrie, J.; Betser, Y.; Martin, S.C.; Smith, R.P.; Jaganathan, S.; Mathew, T.; Krishnan, P.; Serhan, C.; Long, S. “Transferred-substrate heterojunction bipolar transistor integrated circuit technology”. Conference

Proceedings. Eleventh International Conference on Indium Phosphide and Related Materials (IPRM'99) Piscataway, NJ, USA: IEEE, 1999. p.169-74.

[2] Lee, S.; Kim, H.J.; Urteaga, M.; Krishnan, S.; Wei, Y.; Dahlstrom, M.; Rodwell, M. "Transferred-substrate InP/InGaAs/InP double hetero-junction bipolar transistors with f_{max}=425 GHz." *Electronics Letters*, vol.37, 16 Aug. 2001. pp.1096-1098

[3] Guthrie, J.R.; Urteaga, M.; Scott, D.; Mensa, D.; Mathew, T.; Lee, Q.; Krishnan, S.; Jaganathan, S.; Betser, Y.; Rodwell, M.J.W. "HBT MMIC 75 GHz and 78 GHz power amplifiers". Conference Proceedings. 2000 International Conference on Indium Phosphide and Related Materials Piscataway, NJ, USA: IEEE, 2000. p.246-9.

[4] Wei, Y; Lee, Sangmin; Sundararajan, S; Dahlstrom, M; Urteaga, M; Rodwell, M; "High current (100mA) InP/InGaAs/InP DHBTs with 330 GHz f_{max}". Conference Proceedings. 2002 Indium Phosphide and Related Materials Conference, May 12-16, 2002, Stockholm, Sweden: IEEE, 2002. p.47-50.

[5] R. Ramachandran and A.F. Podell, "Segmented cascode HBT for microwave-frequency power amplifiers", U.S. Patent 5066926, November 1991, Filed Jun. 26, 1990.

[6] B. Bayraktaroglu and M. Salib, "Unconditionally Thermally stable Cascode GaAs HBT's for Microwave Applications", IEEE Microwave and Guidewd Wave Lett., vol.7, No. 7, pp.187-189, 1997.

[7] Liu, William., Hin-Fai Chau; Beam, E., III 'Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors'. IEEE Transactions on Electron Devices, vol.43, (no.3), IEEE, March 1996. p.388-95

Acknowledgement

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