40 Gb/s TDM System Using InP HBT IC Technology

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***Abstract* — A 40 Gb/s time-division-multiplexing (TDM) system transmitter and receiver with 4-channel 10 Gb/s interface is presented. InP DHBT IC technology is used to implement the complete chipset (4:1 multiplexer with VCO /clock multiplication unit, modulator driver, transimpedance amplifier, limiting amplifier and 1:4 demultiplexer with clock and data recovery). A 2.26 km long transmission experiment was performed using the system with 40 Gb/s, 2^{31}-1, NRZ PRBS. The transmit eye exhibits a high extinction ratio >12.5 dB with 1 ps added RMS jitter and 4 dbm output power. Receive sensitivity is better than –7.8 dBm with 0.22 dB dispersion penalty.**

I. INTRODUCTION

With the 40 Gb/s systems reaching commercial deployment, there is a great demand for low cost integrated solutions that enable transponder manufacturers to meet performance, power and size constraints. Various device technologies including SiGe HBT, InP HEMT / HBT and GaAs PHEMT [1]-[2] have been competing to realize some or all of the circuits for these applications. Among them, InP DHBT technology exhibits excellent high-speed performance, high break-down voltage, large-scale integration, good uniformity and reliability. This makes it suitable for realizing broadband analog amplifiers as well as large scale digital circuits required for the front-end components in a 40 Gb/s system.

In this paper we present a complete chipset (Table. I) for a 40 Gb/s TDM system with 4-channel 10 Gb/s interface. System test for a 2.26km link using a CW laser and EO modulator are presented.

TABLE I. SUMMARY OF CIRCUIT PERFORMANCE

Circuit	Gain	Bandwidth / Speed	Power
4:1 Mux. / CMU		36-45 Gb/s	2.7 W
EA Mod. Driver	31 dB	43 GHz	1.8 W
EO Mod. Driver	30 dB	41 GHz	2.8 W
Transimpedance Amp.	56 dBΩ	36 GHz	0.4 W
Limiting Amp.	24 dB	35 GHz	0.7 W
1:4 Demux. / CDR		38-42 GHz	3.5 W

II. SYSTEM OVERVIEW

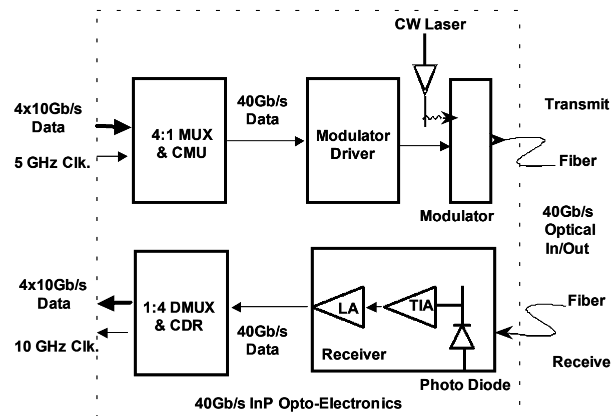

Fig. 1. Block diagram of the 40 Gb/s TDM system.

Fig. 1 shows the functional block diagram for a 40 Gb/s TDM system prototype using the transmitter and receiver circuits presented in this paper. The input and output interface consists of 4-channels of 10 Gb/s signals.

At the transmit end, four 10 Gb/s parallel CML level inputs are multiplexed to a 40 Gb/s serial bit stream by the 4:1 MUX. A 20 GHz VCO is divided down and locked to the 5 GHz input clock. Two modulator drivers used to drive an electro-absorption modulator (EAM) or a differential electro-optic modulator (EO) are presented. The EAM/EO modulates a CW laser.

At the receive end, a receiver with a p-i-n photo-diode, transimpedance amplifier and a limiting amplifier is integrated in one package. A 1:4 demultiplexer with integrated clock and data recovery circuit is used to synchronize the on-chip 40 GHz VCO to the phase of the incoming data. A 10 GHz clock in phase with the demultiplexed output data is made available.

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III. TECHNOLOGY

InAlAs/InGaAs/InP DHBT technology with 140 GHz f_t and 160 GHz f_{max} was used to realize the circuits. 4 inch wafers with standard GaAs HBT process techniques and a carbon doped base for improved reliability at high current density were used. The smallest device sizes were 1x3 μm^2 emitter area with typical current gain of 40. Various device sizes, two layers of interconnect metal with polyimide as the dielectric, Si_3N_4 MIM capacitors with 0.36 fF/μm^2 capacitance and NiCr resistors with 50 Ω/sq resistivity were available. CPW transmission lines were implemented on the two metal layers wherever required. All IC's were packaged in a high speed ceramic package and tested.

IV. TRANSMIT

Transmit side consists of a 4:1 multiplexer and a modulator driver driving an EA or EO modulator that modulates a CW laser.

A. 4:1 Multiplexer and Clock Multiplication Unit

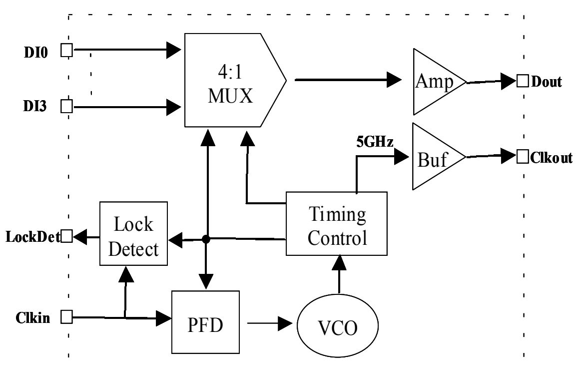

Fig. 2. Block diagram of the 4:1 multiplexer and clock multiplication unit.

The 4:1 multiplexer (Fig. 2) is based on cascaded 2:1 selector architecture. Each 2:1 selector uses ECL latches with additional buffers to regenerate the data. An on-chip 20 GHz VCO (similar to [3]) is phase frequency locked to the 5 GHz reference input clock via static dividers and an internal loop filter. A clock distribution circuit delivers clock signals with proper phase and frequency for all the latches. I/O's are differential CML levels with 50 Ω terminations. Operating from a –4.2 V supply the IC (Fig. 3) dissipates 2.7 W and has a locking range of 36-45 GHz.

Fig. 4 shows the 40 Gb/s eye pattern from the multiplexer, on driving it with 4 channels of de-correlated 10 Gb/s 2^{31}-1 PRBS. 260 mV single-ended output with 20-80% rise/fall times of 9.3 ps / 7.1 ps and 1.1 ps rms jitter was observed using a 50 GHz sampling module (Tektronix 80E01).

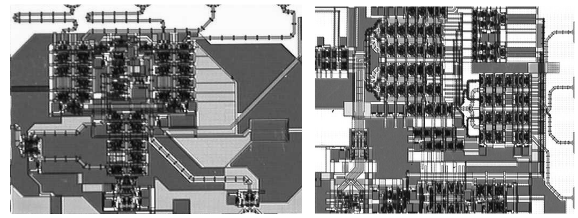

Fig. 3. Micrograph of the 40 Gb/s 4:1 multiplexer and 1:4 demultiplexer (3.3 mm x 3.3 mm each).

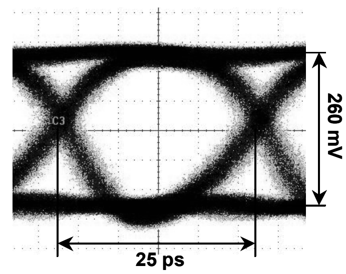

Fig. 4. 40 Gb/s output from the 4:1 multiplexer

B. Modulator Driver

Two versions of the modulator driver one with 3Vp-p single-ended output for driving EAMs and one with 6Vp-p differential output (Fig. 5) for driving differential Lithium Niobate (EO) modulators were designed [4].

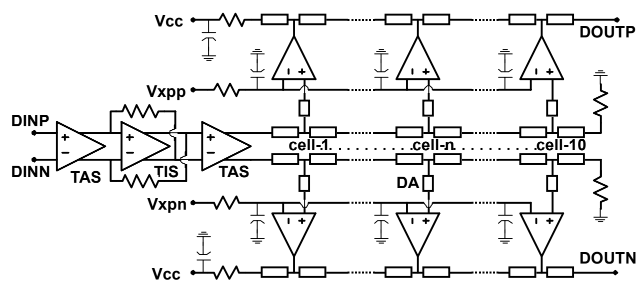

Fig. 5. Schematic of the 40 Gb/s differential modulator driver.

Small signal gain >30 dB and and broad bandwidth of 41 GHz were obtained from a single chip using lumped input stages and a distributed output stage (Fig. 6). A 500 mVp-p differential drive from the multiplexer is sufficient to provide full output swing from the driver. Additional features like modulation current control to adjust the output swing, cross-point control to change the zero crossing from 40% to 75%, output power down option, modulation current monitor pin for external closed-loop automatic power control are also available.

When driven with the multiplexer, the differential driver provides (Fig. 7) 3 Vp-p swing at each end with rise/fall times of 8.6 ps / 7.5 ps and an rms jitter of 1.23 ps (added rms jitter of 0.55 ps).

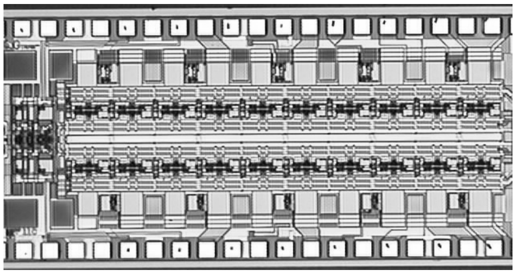

Fig. 6. Micrograph of the 40 Gb/s differential modulator driver (3.3 mm x 1.5 mm)

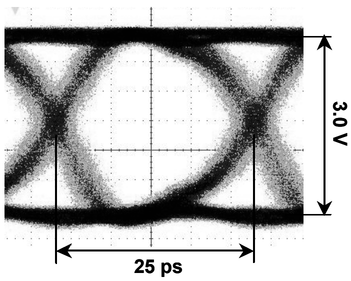

Fig. 7. 40 Gb/s single-ended output from the differential modulator driver.

C. Modulator and Laser

A 1550 nm CW laser source with 13 dBm output power was used. The differential driver output was used to drive a differential Lithium Niobate modulator. 4.1 dBm of optical power with 12.8 dB extinction ratio and 1.62 ps rms jitter (1 ps of added rms jitter) was observed (Fig. 8). After 2.2 km of SMF fiber the extinction ratio dropped to 9.9 dB, with 1.8 ps rms jitter and 40% crossing (Fig. 9).

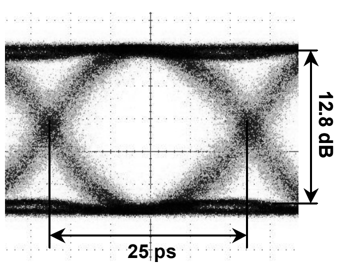

Fig. 8. 40 Gb/s optical output from the lithium niobate modulator after 0 km

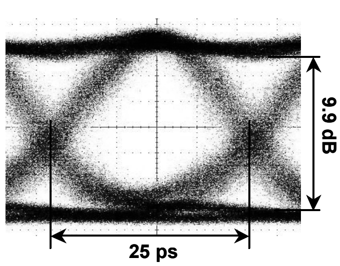

Fig. 9. 40 Gb/s optical output from the lithium niobate modulator after 2.25 km

The single-ended driver was used to drive an EA modulator. Because of the non-linearity in the optical insertion loss vs. applied voltage for EAMs, a driving voltage with 75% duty-cycle ratio was required to maximize the optical eye opening. About 2.9 dBm of optical power with 10.4 dB extinction ratio and 1.5 ps rms jitter was observed (Fig. 10).

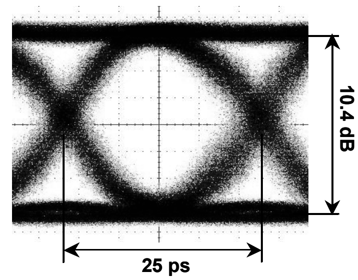

Fig. 10. 40 Gb/s optical output from the EAM after 0 km.

V. RECEIVE

The receive end consists of a receiver module followed by a 1:4 demultiplexer.

A. Receiver

The receiver module incorporates a InP based p-i-n photo-diode, a trasimpedance amplifier and a limiting amplifier (Fig. 11).

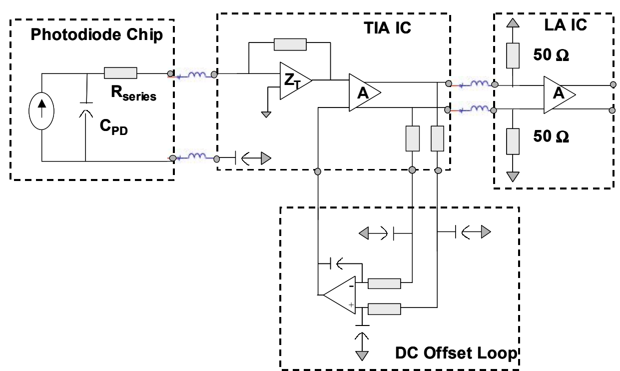

Fig. 11. Schematic of the 40 Gb/s receiver.

The transimpedance amplifier includes a transimpedance stage followed by a single-ended to differential gain stage with a DC offset restore loop [5]. The chip dissipated 0.4 W and provides an overall differential transimpedance of 650 Ω with 36 GHz bandwidth and +10 to -5 ps group delay variation.

The differential four stage limiting amplifier has a 20 mV input sensitivity, 24 dB gain, and 35 GHz bandwidth. Operating from a -5V supply, the IC provides 1 Vp-p differential output with 0.7 W power dissipation.

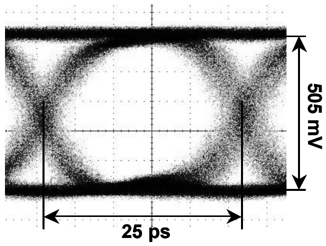

Fig. 12. 40 Gb/s single-ended output from the receiver module

The receiver was tested with a 40 Gb/s 2^{31}-1 PRBS eye pattern from the EO modulator. Fig. 12 shows 505 mV single-ended output with rise/fall times of 7.9 ps / 6.1 ps and 1.3 ps rms jitter for a 0 dBm input optical power. The output was demultiplexed into 4 channels of 10 Gb/s data and the bit error rate was tested. The receiver exhibits -7.8 dBm sensitivity at a BER of 10^{-12} with 3.5 dBm overload, 8000 V/W differential gain, and 0.22 dB dispersion penalty after transmission over 2.26 km of SMF (Fig. 13).

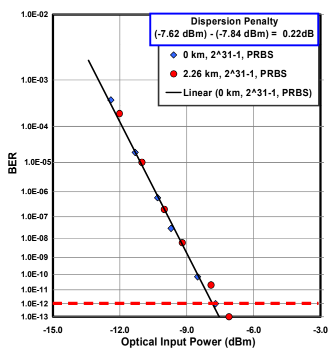

Fig. 13. BER performance at 40 Gb/s for the TDM system after 0 km and 2.25 km.

B. 1:4 Demultiplexer and CDR

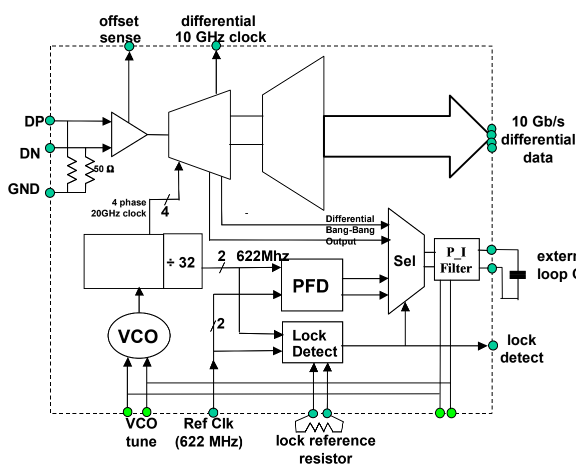

Fig. 14. Block diagram of the 1:4 demultiplexer with clock and data recovery.

The 1:4 demultiplexer (Fig. 14) incorporates an Alexander phase detector for clock and data recovery. On-chip 40 GHz VCO [3] is synchronized to the incoming data using a phase-locked loop locked consisting of a phase-frequency detector and a proportional-integral filter. The IC (Fig. 3) operates of a -4.2 V supply and dissipates 3.5 W. Fig. 15 shows the recovered 10 GHz clock and data from a 40 GB/s bit pattern.

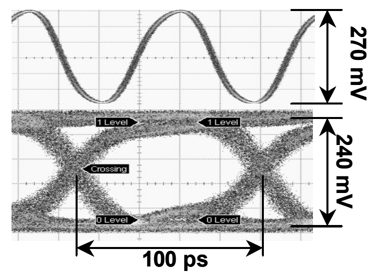

Fig. 15. Recovered 10 GHz clock and 10 Gb/s data from the 1:4 demultiplexer.

V. Conclusion

A complete 40 Gb/s InP DHBT chipset for 40 Gb/s TDM system has been developed. The performance of these ICs have been evaluated in a 2.26 km transmission link. The transmitter provides better than 12.5 dB extinction ratio with 1 ps added RMS jitter and up to 4dbm output power. The receiver sensitivity is better than –7.8 dBm with 0.22 dB dispersion penalty. These IC's would meet the requirements for commercial deployment.

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