InAs/AlSb HFETs WITH f_T AND f_{max} ABOVE 150 GHz FOR LOW-POWER MMICs

J. Bergman, G. Nagy, G. Sullivan, and B. Brar
Rockwell Scientific Company
Thousand Oaks, CA 91360, U.S.A

C. Kadow, H.-K. Lin, A. Gossard, and M. Rodwell
University of California, Santa Barbara
Santa Barbara, CA 93106, U.S.A.

Abstract

Very low-power InAs/AlSb HFETs with excellent RF performance are reported. These metamorphic HFETs on GaAs substrates combine high microwave g_m of at least 1.1 S/mm with low parasitic resistances to offer simultaneous measured f_T and f_{max} values of 160 GHz for both figures of merit. This performance is obtained at a drain bias voltage of only 0.35 V for an HFET with a 0.25-μm gate length. The high current gain (f_T) is attributable to the improved charge control due to scaling of the barrier thickness to 180 Å. The maximum power gain (f_{max}) depends on both g_m and the HFET output conductance, which is fundamentally limited by the low breakdown voltage gap of the InAs channel (E_g = 0.36 eV).

I. Introduction

InAs/AlSb HFETs are promising for high-speed applications on account of the high electron mobility (>25,000 cm^2/Vs) and saturation velocity (4×10^7 cm/s) (1). In addition, the large conduction band offset of 1.35 eV between InAs and AlSb results in excellent electron confinement and allows for very high electron densities relative to other lattice-matched III-V materials (2). The combination of high electron mobility and concentration in the 2DEG has motivated research into developing the InAs/AlSb HFET (3)-(5) into a high-speed integrated circuit technology with unparalleled speed-power performance.

The major inherent drawback of the InAs/AlSb HFET is the low breakdown voltage associated with the narrow 0.36 eV band gap of the InAs channel. The low output resistance of the InAs/AlSb HFET has limited its RF power gain in earlier work. The best-reported results to date indicate simultaneous measured f_t / f_{max} values of 180 / 80 GHz for a 0.1-μm HEMT (6), and 120/100 GHz for a 0.25-μm device (4). Approaches to improve the breakdown voltage in an InAs/AlSb HFET include the use of a back gate to collect impact-generated holes (7), and a composite sub-channel design (3). The back gate was shown to be very effective in increasing breakdown, but the high frequency performance was degraded by the high shunt capacitance between the channel and back-gate. The sub-channel can improve breakdown slightly by shifting electron transport to the narrow InAs sub-channel, but reported results typically show reduced mobility compared to single channel InAs/AlSb HFETs. In addition, the need to engineer the device band structure profile so that the majority of electrons are confined in the sub-channel in the high-field region complicates HFET epitaxial design.

Alternatively, we focus on low voltage operation, with V_{ds} below 0.5 V, and do not modify our baseline high quality InAs/AlSb HFET to improve breakdown. In the present work we report on the RF characteristics of vertically scaled 0.25-μm InAs/AlSb HEMTs with best-to-date simultaneous measured f_t / f_{max} values of up to 160 / 160 GHz at drain biases below 0.5 volts.

II. Epitaxial Growth and Fabrication

The HFET material was grown by solid-source MBE on a semi-insulating GaAs substrate, using a 2 μm AlSb metamorphic buffer to accommodate the large (~7%) relative lattice mismatch. The HFET active layers were grown at 500 °C over an $Al_{0.8}Ga_{0.2}Sb$ stabilizing buffer. The 125 Å InAs channel was followed by a 130 Å AlSb upper barrier, with approximately 4×10^{12} cm^{-2} tellurium modulation doping. The upper barrier was scaled down from 200 Å in order to improve the HFET transconductance. The earlier HFET exhibited peak f_t / f_{max} values of 120 / 100 GHz for a nominally 0.25-μm gate HFET (4). Finally, the HFET was capped by a 50 Å strained $In_{0.5}Al_{0.5}As$ cap, which serves to provide a chemically stable surface layer, as well as lower the gate leakage current relative

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to HFETs with GaSb caps (8). The epitaxial layer structure is illustrated in Figure 1. Hall measurements determined the sheet carrier concentration and mobility of the initial material to be 3.7×10^{12} cm^{-2} and 19,000 cm^2/Vs at 295 K, respectively. The corresponding values at 77 K were 3.4×10^{12} cm^{-2} and 65,000 cm^2/Vs, which indicate excellent material quality for an InAs/AlSb HFET with AlSb buffers at this doping level.

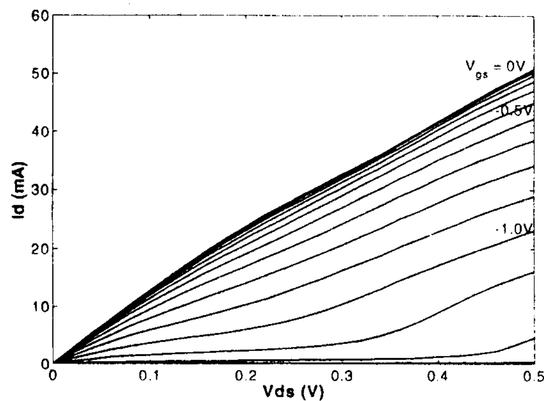
Layer	Thickness
InAlAs	50 Å
AlSb	130 Å ← Te: 4e12
InAs:	125 Å
AlSb:	80 Å
$Al_{0.8}Ga_{0.2}Sb$:	2000 Å
AlSb:	2 μm
GaAs substrate	

Figure 1. The epitaxial layer structure of the InAs/AlSb metamorphic HFET. Te delta-doping provides charge to the channel.

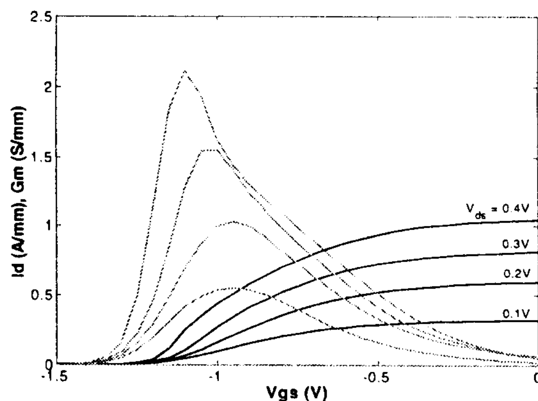
The HFET was fabricated using a conventional mesa isolation process, by wet chemical etching to the $Al_{0.8}Ga_{0.2}Sb$ buffer layer. Diffused Pd-Au source and drain contacts were employed (9). Four-wire transfer length measurements yielded a contact resistance of 0.07 Ω-mm with a sheet resistance of 100 Ω/square. Nominally 0.25-μm gates were patterned with electron-beam lithography.

III. DC Results

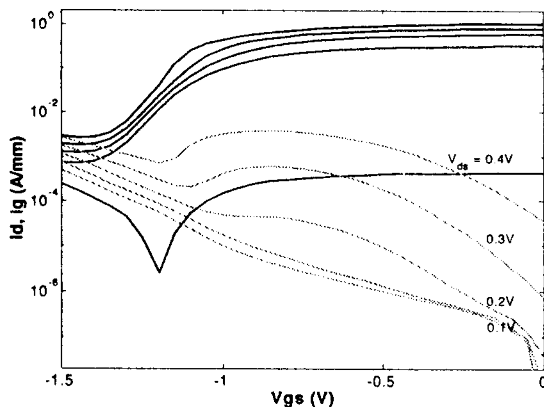
The device has typical DC characteristics for a doped InAs/AlSb HFET. Gating by impact-generated holes increases the drain conductance at high drain bias, seen in Figure 2a for a 2 × 20 μm device. For a 2 μm source-to-drain spacing, the zero-bias source-drain access resistance is 0.30 Ω-mm, a value that needs to be kept low to achieve high performance at low voltage. Impact generated holes also enhance the DC transconductance, as indicated by a peak g_m of 1.5 S/mm and 2.0 S/mm at V_{ds} of 0.3 V and 0.4 V, respectively (Figure 2b). As explained in (4), the onset of impact-ionization increases the output current, which increases the peak DC g_m at high drain bias. This is strictly a low frequency effect, so the RF transconductance is expected to be lower. The rise in the gate leakage current as the gate voltage is lowered at $V_{ds} \geq 0.3$ V is also attributable to the impact-generated holes. Finally, it should be noted that the very low gate leakage of this vertically scaled HFET (180 Å barrier), shown in Figure 2c, reproduces the very low gate leakage of the earlier device with a 250Å reported in (4).



(a)



(b)



(c)

Figure 2. (a) The DC output characteristics for the 2 × 20 μm InAs/AlSb HFET. (b) The DC input characteristics show high current density and transconductance, but that latter is enhanced by impact-ionization at $V_{ds} \geq 0.3$ V. (c) The sub-threshold plot shows low gate leakage for an InAs/AlSb HFET. The excess gate current at high drain bias is caused by the collection of impact-generated holes at the gate.

IV. RF Results

On-wafer s-parameter measurements were conducted from 0.05–50 GHz over a range of DC bias conditions, and contour maps of the RF figures of merit were generated. Figure 3 shows the –20 dB/decade extrapolated f_T and f_{max} mapped as a function of the bias. Pad parasitics are not de-embedded. We observe that f_T increases with drain bias, achieving a maximum value of 172 GHz at V_{ds} = 0.45 V. The increase of f_T with the drain voltage is likely correlated to a rise in the RF g_m. The rise is not as dramatic as that of the DC transconductance in Figure 2b, however, indicating that only fraction of enhancement of DC g_m with increasing V_{ds} is caused by faster electron transport in the InAs channel. The peak f_{max} occurs between V_{ds} = 0.35 and 0.40 V, and at slightly lower gate voltage and drain current. The extrapolated f_T and f_{max} at this point, shown in Figure 4, are both 162 GHz.

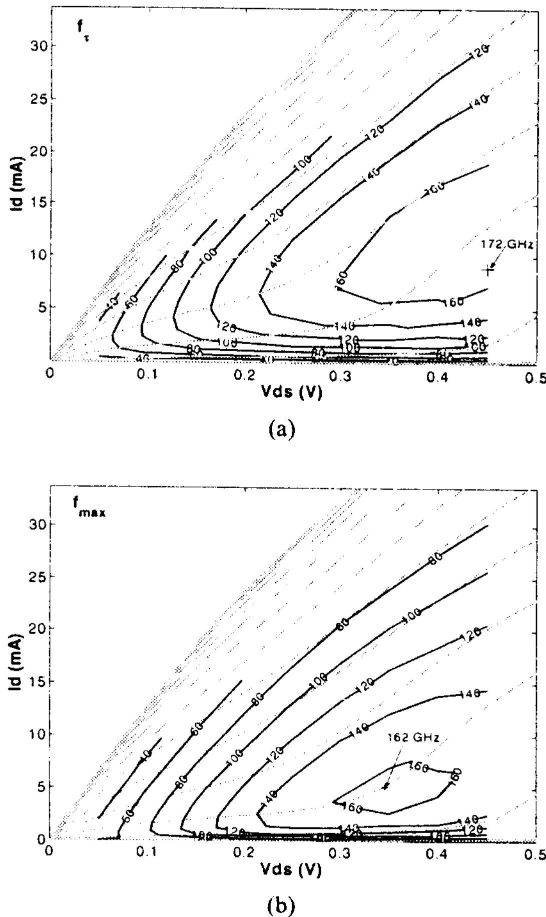


Figure 3. (a) The f_T contour plot shows f_T steadily rising with drain voltage bias, although not nearly as dramatically as the DC g_m. (b) The corresponding f_{max} contour plot. The pad parasitics have not been de-embedded. The high figures of merit at drain voltages below 0.2 V highlight the low-power potential of the InAs/AlSb HFET.

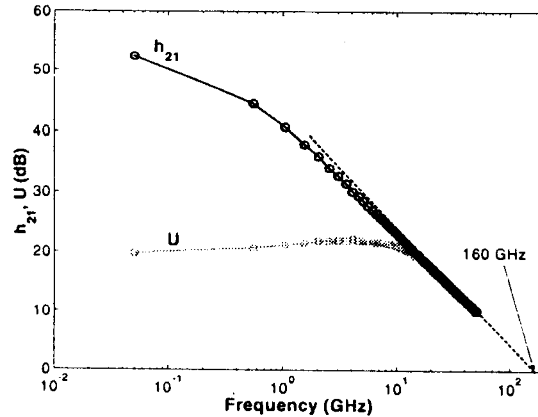


Figure 4. The HFET's short-circuit current gain, h_{21}, and the maximum unilateral gain, U. The DC operating conditions are V_{gs} = –1.1 V, V_{ds} = 0.35 V, with I_d = 6.08 mA and I_g = -20.9 μA.

In order to better understand the underlying device physics, we extract the extrinsic transconductance from the measured RF data. As mentioned previously, the DC g_m is artificially high due to impact ionization effects in the high field region near the drain, specifically gating by impact-generated holes and the high HFET output conductance. It is expected that the effects of impact-generated holes on the HFET electrical properties are confined to low frequency HFET parameters, because of the slow response times of the holes relative to the majority electrons. This is the reason that the measured S_{22} appears inductive at low frequencies at high drain voltages; the collection of impact-generated holes lags the voltage at the drain. We observe that the AC g_m agrees with the DC g_m at very low frequencies. For example, for a fixed V_{ds} and V_{gs} of 0.4 V and –1.1 V, the DC g_m was 2.11 S/mm. At 50 MHz, the lowest frequency measured, the AC transconductance is 1.87 S/mm. The AC g_m drops rapidly with frequency, falling to 1.26 S/mm at 1 GHz, and settling to its steady-state value of 1.13 above 4 GHz. On the other hand, when the drain voltage is lowered to 0.2V, the steady-state RF transconductance of 0.68 S/mm barely changes from the DC value of 0.70 S/mm, confirming that the large, sharply peaked DC g_m for drain voltages ≥ 0.3 V is attributable primarily to impact-ionization effects. These observations indicate that any microwave FET model used for MMIC design should give special attention to impact-ionization.

It should be noted that the extrinsic RF g_m does in fact increase with drain voltage, but much more gradually than the DC g_m. Figure 5 shows the corresponding contour plot of the extrinsic RF g_m, showing a steady increasing trend with drain bias, leveling out to a maximum of about 1.15 S/mm at V_{ds} = 0.45 V. The improvement in RF transconductance at higher drain voltage is expected to be a result of faster electron transit from source to drain. As expected, since the FET f_T typically is proportional to g_m, the f_T and g_m contour maps have excellent agreement.

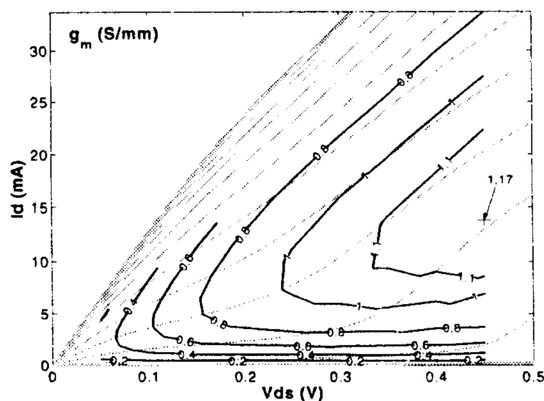


Figure 5. The contour map of the extrinsic RF g_m.

V. Conclusion

An InAs/AlSb with 0.25-μm gate length exhibits a simultaneous f_T and f_{max} of at least 160 GHz, achieved by vertically scaling a previous HFET design. By reducing the barrier thickness from 250 Å to 180 Å and slightly lowering the doping, we increased the figures of merit from 120 / 100 GHz to 160 / 160 GHz. In addition, the gate leakage current remained low, indicating that further scaling of the HFET barrier thickness may be possible. While the InAs/AlSb HFET's RF power gain is still limited by an inherently low output resistance, the improvement in g_m from additional vertical scaling may help to further enhance high frequency performance.

VI. References

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