THERMAL LIMITATIONS OF InP HBT'S IN 80 AND 160 Gbits^{-1} IC's

I.Harrison†, M. Dahlstrom, S. Krishnan, Z. Griffith, Y.M Kim, M.J.W. Rodwell

†School of Electrical and Electronic Engineering, University of Nottingham, Nottingham, NG7 2RD, UK
Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA

A 3D thermal model based on finite elements has been developed for the analysis of the thermal resistance of InP heterojunction bipolar transistors. The model was verified by comparing simulated and experimental results. The simulations also show that the maximum temperature in the device can be significantly higher than the experimentally determined base-emitter junction temperature. By applying scaling laws, a road map for 80Gbit/s and 160Gbit/s devices is presented. Simulations show that devices suitable for 160Gbit/s circuits will be thermally possible if the InGaAs etch stop or contacting layer is removed from the sub collector.

I Introduction

40Gbit/s integrated circuits (ICs) are becoming commercially available. Two major competing technologies are SiGe heterojunction bipolar transistors (HBTs) and InP HBTs. While very high mm wave power gains have been obtained with single heterojunction devices (SHBT), they suffer from low breakdown voltages and high thermal resistance because of the narrow band gap InGaAs collector. To overcome these inherent problems, a double heterostructure bipolar transistor (DHBTs), which has an InP collector, can be used. Devices of this kind have been reported with a f_{max} in excess of 450GHz [2,3]. These results indicate that DHBTs have potential applications in 80Gbit/s and 160Gbit/s ICs. This is reinforced by recent observations of frequency dividers operating above 80GHz [4,5]. As device design is modified for 80-160Gbits/s applications, the current density within the device will greatly increase resulting in higher device temperatures and so accurate thermal design is critical for accurate circuit simulation and reliability studies.

Thermal modeling of HBTs has, to date, centered on power amplifiers [6]. These studies have concentrated on modeling the heat flow in the substrate using a semi-analytical approach developed for Si BJT's [7]. The method does not account for (1) the temperature gradients within the device which are significant in sub-micron HBT's or (2) heat flow through the emitter metalisation which can be high as 20% of the total heat dissipated.

Before circuits can be marketed, the device reliability must be assessed and this has driven an interest in the thermal resistance of InP HBTs. [9,10] For 80 and 160 and probably 40Gbit/s applications, DHBTs will be used because of their lower thermal resistance. This paper examines the thermal performance of devices for the 80 and 160 Gbit/s applications by modeling the heat flow in 3D.

II. Device Scaling

To achieve high-speed performance, an increase in the current density (J) will allow a device with a smaller collector-base junction area to be used in the circuit, so reducing C_{bc}. However, J cannot be increased indefinitely because of the Kirk Effect.

If the collector doping N_D is chosen so that the collector is fully depleted at zero bias current and the applied V_{CE} the maximum current density through the emitter junction is approximately given by

$$J_{max} = 4\varepsilon v_{sat} V_{CE} / T_C^2 , \qquad (1)$$

where ε is the dielectric constant of the collector, T_C is the collector thickness, and v_{sat} the saturated electron velocity in the collector [1]. The minimum time required (τ) by the transistor to switch the output voltage by ΔV can be approximated by;[1]

$$\tau \approx \frac{C_{cb}\Delta V_L}{I_0} = \frac{A_c}{A_e}\frac{\Delta V_L T_C}{4 v_{sat} V_{CE}} , \qquad (2)$$

where I_0 is the switched current and is the product of J_{max}, given by (1) and the area of the emitter (A_E). To obtain the last term of (2), the collector-base junction area is assumed to be A_C. Although the performance of digital circuits requires additional terms [1] and depends significantly on the layout of the circuit, (2) is the dominant term in InP HBT digital circuits. By reducing the collector thickness the switching time can be decreased.

III.Thermal Model

The temperature distribution within a device has been determined by using a commercial finite element solver (ANSYS) to solve 3D the heat diffusion equation. In 3D problems, there is a requirement to use symmetry to reduce the number of nodes so that storage limitations are not exceeded and the computational times are acceptable. There is a natural plane of symmetry along the length of the emitter and if the base contact pad is ignored there is another orthogonal plane of symmetry. The collector of a DHBT normally consists of an InGaAs set back layer, and a grading layer, followed by InP collector. As the electrons leave the base they experience a large electric field that accelerates them. In this region close to the base, the electrons move quasi-ballistically with little scattering and so there will be little dissipation of heat. In this model, the ballistic transport region is assumed to extend over the whole of the setback and grading layer.

Thermal conductivity (k) of semiconductors decreases when the temperature is increased and can be modeled using the equation:

$$k_T = k_{300}(300/T)^n . \qquad (3)$$

The values of the room temperature k and the exponential term (n), used in this work are shown in table I.

In GaAs, k reduces with heavy doping and a similar effect will also occur in InP and InGaAs. Unfortunately there is no experimental data for InP to incorporate into the model so k of

0-7803-7704-4/03/$17.00©2003 IEEE

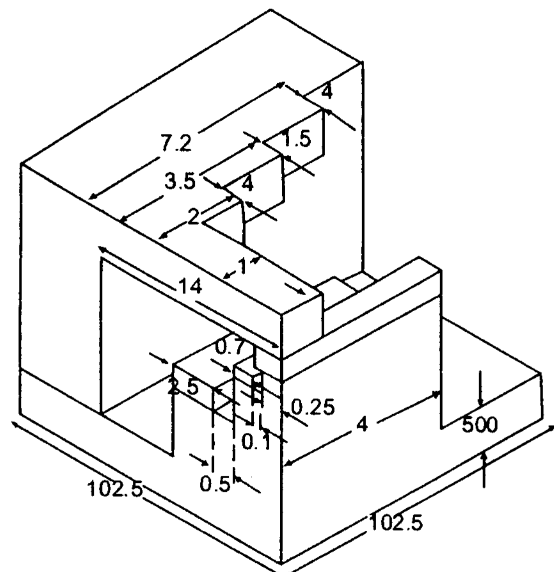

Fig 1. The simulated device structure used for the verification of the thermal model. (Symmetry allows quarter of the device to be used). All measurements are in μm. In order to show the detail, the diagram is not drawn to scale. The thickness of the collector, base and emitter metalisation are 0.3μm, 0.1μm and 0.4μm. The layer structure is given in the table II.

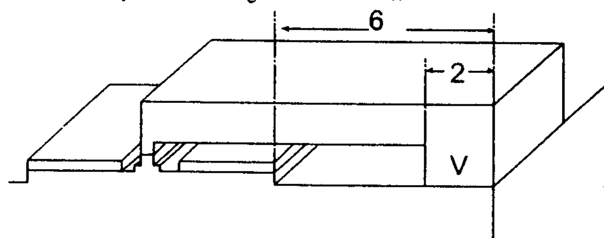

Fig 2. The physical device structure used in the assessment of the thermal performance of a current switch. Two lines of symmetry are assumed: one midway between the devices and the second through the middle of the devices so that only half of the emitter is simulated. V marks a thermal via connecting the emitter interconnects with the InP substrate. All dimensions are in μm.

TABLE I

THERMAL CONDUCTIVITIES OF THE MATERIALS USED IN THIS SIMULATION

Material	Values used ($Wcm^{-1}K^{-1}$)	n	Experimental Range ($Wcm^{-1}K^{-1}$)	Refs
InP	0.68	1.42	0.68-0.877	[11]
InGaAs	0.048	1.375	0.048-0.061	[12]
Au	3.17	-	3.17	[13]

k of gold was assumed to be temperature independent.

TABLE II

LAYER DIMENSIONS

Label in fig .4	Length (μm)	Sub-layer length (μm)	Description
Sub	500		Substrate
SC	0.20		InP sub collector
ES	0.05		Etch stop layer
		0.156	InP Collector
		0.024	InGaAs/InAlAs Grade
		0.020	InGaAs setback layer
C	0.2		Total Collector thickness
B	0.03		InGaAs Base
		0.12	InP Emitter
		0.04	InGaAs Emitter Cap
E	0.16		Total Emitter length

heavily doped material is assumed to be 65% of the undoped

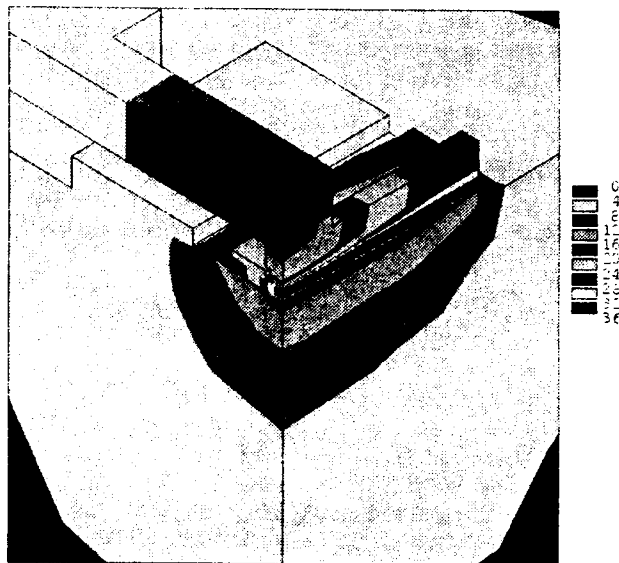

Fig.3 Temperature profile inside the simulated device when the power dissipation was 10mW. The lower surface of the substrate was fixed at 300K. The contours are shown as alternating light and dark gray. The collector is the hottest part of the device.

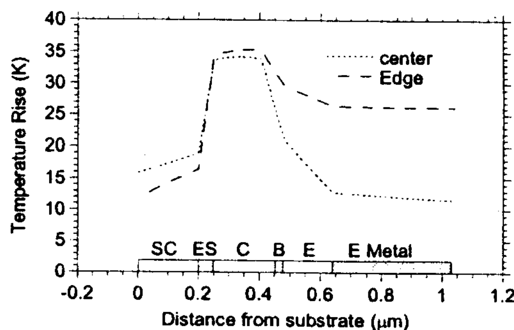

Fig 4.Temperature profile through the center and edge of the device. The different parts of the device are shown at the bottom of the figure and the labels are given in table II

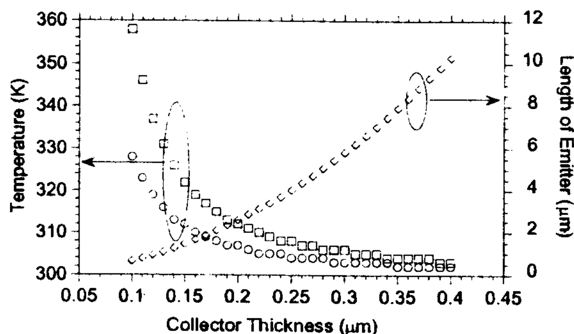

Fig. 5 The variation of junction temperature (circles) , maximum device temperature (squares) and emitter length (diamonds) with the collector thickness.

material. (This is the measured reduction in GaAs).

The heat flow in the emitter and emitter metalisation will be vertical before flowing in a horizontal direction in the emitter interconnect. Rather than model the layers making up the emitter and emitter metalisation separately a composite *k* was used. This can be founded by summing the thermal resistances of each layer. The collector and base metalisations

were also multilayer, however the heat flow in these layers is not significant and so these were modeled using k of gold.

Two different device structures have been simulated. The first, shown in fig 1, represents the test transistors used in our laboratory and allows the verification of the simulation results with experiments. The layer structure and the device dimensions are shown in table II. The device is passivated using a polyimide, which has a very low k, and so heat flow through the polyimide is assumed to be zero.

High-speed digital circuits have either emitter coupled or current mode topology. In both of these a bias current is switched between two transistors of a differential pair. These transistors need to be in close proximity to each other for high speed. The second structure models one of the devices in such a differential pair. Under normal operating conditions the heat dissipation in each device is the same and so there is a line of symmetry, modeled using an adiabatic plane midway between the devices. The simulated structure is shown in fig 2.

IV.Verification

The thermal model was verified by comparing the measured and simulated thermal resistance of devices. The temperature profile through the device is shown in fig 3. To obtain this plot the input power was set to 10mW, which was the same power used in the experimental determination of the thermal resistance and so a direct comparison between the two can be made. As expected, there is significant temperature variation through the device. In the center of the device the emitter-base junction temperature rise is 21.0K but at the edge of the emitter the increase in junction temperature rise is higher (29.5K). This temperature difference is caused by the limited size of the emitter interconnect. The average temperature rise of the junction is 26.2K, which corresponds to a thermal resistance of 2620K/W. This is in good agreement with experimental value (2600K/W). The collector is the hottest part of the device with a temperature 60% higher than the average temperature of the emitter-base junction. The temperature rise will increase the transit time of the electrons traveling through the collector because of the reduction in the saturated velocity (v_{sat}). (For a 50K temperature rise, v_{sat} will reduce by 10%. [14]). From (1), this change in v_{sat} will also reduce the Kirk current density limit by the same amount.

In fig 4, the temperature through the center of the device and at the edge is shown. There is a large temperature gradient on both sides of the collector caused by the poor k of the InGaAs used in the base and the sub collector etch stop layers. Reduction of the thickness of the InGaAs etch stop layers will significantly reduce the temperature of the collector. This will be discussed in section V.

As the device speed increases the thickness of the base decreases and the control of the base metalisation diffusion becomes important both during manufacture (yield) and during operation (reliability). Diffusion rate increases with temperature. Therefore if the temperature of the base metalisation is higher than expected, this may cause the lifetime of the devices to be below the expected value.

In some parts of the device, especially near the ends, the temperature of the base metalisation is higher than the average emitter –base junction temperature. For reasons given above this will have an adverse effect on reliability. Improving the heat sinking of the emitter at the edge of the device by increasing the width of the emitter interconnects will reduce the maximum temperature of the base metalisation and so improve the reliability.

In fig 5, the junction and maximum temperatures of the simulated device are presented. The structure of the device was the similar to that shown in fig 1 with the exception of the width of the emitter interconnection. To generate a ΔV of 300mV across a 50Ω load impedance requires a 6mA bias current. In generating fig 6, the current flowing through the device is assumed to be 6mA with a 50% switching duty cycle. Furthermore, when the device was conducting, V_{CE} was assumed to be 1V. This equates to an average power dissipation of 3mW. The length of the emitter was chosen so that the device was operating at the Kirk limit given by (1), and the emitter junction width (fig 1) remains constant at 0.5 μm. The length is also given in fig 5. The difference between the junction temperature and the maximum temperature also increases. At a collector thickness of 1000A the maximum temperature rise is nearly 60K. For a 100% duty cycle the temperature rise would be approximately 120K. Clearly this temperature rise is unacceptable. The increase in the width of emitter interconnect also reduces the temperature variation across the device.

TABLE III ROAD MAP OF KEY DEVICE PARAMETERS FOR 80GBIT/S AND 160GBIT/S INP HBT CIRCUITS.

Speed	(Gbit/s)	40	80	160
Collector Thickness	(Å)	3000	2000	1000
Base doping	(cm^{-3})	$4\ 10^{19}$	$6\ 10^{19}$	$8\ 10^{19}$
Base Sheet resistance	($\Omega_\square$)	750	700	700
Base contact resistance	(Ω-μm^2)	150	20	10
Base Thickness	(Å)	400	300	250
Base Mesa width	(μm)	3	1.6	0.4
Current Density	(mA/μm^2)	1	2.3	9.8
Emitter. Junction Width	(μm)	1	0.8	0.2
Emitter Parasitic resistivity	(Ω-μm^2)	50	20	5
Emitter Length	(μm)	6	3.3	3.2
Predicted MS-DFF	(GHz)	62	125	237
f_t	(GHz)	170	260	500
f_{max}	(GHz)	170	440	1000

Table IV Predicted temperature rise.

Speed	(Gbit/s)		40	80	160
Predicted MS-DFF	(GHz)		62	125	237
Temperature Rise (Etch Stop)	(K)	Junction	7.5	14.0	28.0
		Maximum	10.0	20.0	49.0
Temperature Rise (No sub collector etch stop)	(K)	Junction	5.5	13.0	12.5
		Maximum	7.5	9.0	20.5

V. Devices for 80 and 160Gbit/s applications

Results of the previous section show that the operating temperature of the device rapidly increases as the collector thickness is reduced, given that the device is operated at Kirk-effect-limited current density. It is therefore important to consider the thermal performance of devices suitably scaled for use in 80 and 160Gbit/s applications. Before these simulation can be performed the key physical parameters for 80 and 160 Gbit/s IC's need to be examined. Master-slave latch speed is an important figure of merit because these circuits are heavily used in fiber transceivers. In conservative system-level designs the maximum clock rate is 1.5 times the operating bit rate. To determine the physical parameters of the devices, stated in table III, the methodology of [1] was used. The base contact resistance and base sheet resistivity are all consistent with values obtained in our laboratory [3]. The 160 Gbit/s devices have a very small base–emitter separation as well as a small base mesa. Devices with dimensions similar to the proposed devices have already been manufactured in the GaAs system. (e.g. [15]). Note that the current densities are 1, 2.3 and 9.8 mA/μm^2 at the three bit rates and this drives the

thermal design.

Table IV gives the temperatures at the base-emitter junction and the maximum temperature with and without the collector etch stop layer. In calculating the device temperatures, the same assumptions as in the previous section were used and so the total power dissipated in the device was set to 3mW. The temperature rise for the 40 and 80 Gbit/s devices is clearly within acceptable bounds even when the etch stop layer was used. The 80Gbit/s device would benefit thermally by a reduction in the thickness of the etch stop layer. With the etch stop layer the temperature rise in the 160Gbit/s device is 49K and 23% of the heat flows through the emitter. Under idle conditions the dissipated power will be doubled and to the first approximation the temperature rise will be 98K. This value is too high for long-term operation of the device. With no etch stop layer the maximum temperature rise within the device is significantly lower (20.5K). Under these conditions the flow of heat out of the emitter is reduced to only 0.3mW (i.e. 10% of the total). Under idle conditions, the temperature rise becomes 41K, which is acceptable. Note, the etch stop layer is used to control the base mesa process and so to get a device operating at these low temperatures will require the development of an alternative base mesa process or etch stop layer. The InGaAs etch stop layer also provides an additional benefit. The resistance of contacts on n+ InGaAs is smaller than on n+ InP. Therefore, the removal of the etch stop layer will increase the collector resistance and the effect of this on circuit performance needs to be considered.

VI.Conclusions

An experimentally validated thermal model of InP HBT has been presented and has been used to demonstrate that operation of devices for 80 and 160Gbit/s applications are thermally possible. To achieve this, the etch stop layer in the sub-collector needs to be removed.

The model also shows that the maximum temperature within the device is higher than the measured value at the emitter-base junction. This observation needs to be taken into account when the reliability of devices is considered.

Acknowledgements

The authors would like to acknowledge Walsin Corp. and the University of California CORE program for part funding this work. I.Harrison would also like to thank the Royal Academy of Engineering for an Engineering Foresight Award.

References

1. M.J.W.Rodwell, M.Urteaga, Y.Betser, T.Methew, P.Krishnan,D.Scott, S.Jaganathan, D.Mensa, J.Guthrie, P Pullela, Q.Lee, B.Agarwal, U.Bhattacharya, S.Long and S.C. Martin and R.P. Smith, "Scaling of InGaAs/InAlAl HBTs for high speed mixed-signal and ,mm-wave IC's". International Journal of High Speed Electronics and systems, 11 (2001) pp159-215
2. S.Lee H.J.Kim, M.Urteaga, S. Krishman, Y.Wei, M.Dahlström, and M. Rodwell, "Transferred Substrate InP/InGaAs/InP double heterojunction bipolar transistors with fmax =425GHz." Electronic Letters 27 (2001) pp1096-1098
3. M. Dahlström , M. Urteaga, S. Krishnan, N. Parthasarathy, M.J.W. Rodwell, X.-M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau and W.K. Liu ," Ultra-Wideband DHBTs using a Graded Carbon-Doped InGaAs Base ", presented at IPRM 2002, Stockholm, Sweden
4. S. Tsunashima, H. Nakajima, E Sano, M Ida, K.Kurishima, N. Wananabe, T.Enoki and H. Sugahara. " 90-GHz operation of a novel dynamic frequency divider using InP/.InGaAs HBTs" Proceeding of the 14th Indium Phosphide and related materials conference. (2002) pp43-46
5. S Krishnan,Z,Griffith, M.Urteaga, Y Wei, D.Scott, M.Dahlström, N. Parthasarathy, and M.J.W.Rodwell. "87GHz Frequency dividers in an InP-based Mesa DHBT technology", to be presented at IEEE GaAs IC symposium 2002.
6. R.Anholt. "Thermal impedances of multi-finger heterojunction bipolar transistors." Solid State Electronics 42 (1998) pp865-869
7. R.D.Lindsted and R.J.Surty, "Steady state junction temperature of semiconductor chips", IEEE Trans Electron.Devices 40 (1972) pp41-44
8. W Liu , H.F.Chau and E.Beam, "Thermal properties and thermal instabilities of InP Based heterojunction bipolar transistors", ", IEEE Trans Electron.Devices 43 (1996) pp338-395
9. C.H.Fields, J.Foschaar and S Thomas III," Thermal characterization of 200GHz Ft InGaAs/InAlAs HBT's". Proceeding of the 14th Indium Phosphide and related materials conference. (2002) pp79-82
10. P.C.Grossman, A Gutierrez-Aitken, E. Kaneshiro, D Sawdai and K Sata. "Characterization and Measurement of Non-Linear Temperature Rise and Thermal Resistance in InP Heterojunction Bipolar Transistors", Proceeding of the 14th Indium Phosphide and related materials conference. (2002) pp83-86
11. J.C.Brice in "Properties of Indium phosphide" eds
12. S Adachi and J.Brice pubs INSPEC London p20-21 S Adachi in "Properties of Latticed –Matched and strained Indium Gallium Arsenide" ed P Bhattacharya pubs INSPEC London p34-39
13. "CRC Materials science and engineering handbook", 2nd edition ,eds J.F Shackelford,A.Alexander, and J.S Park, pubs CRC press, Boca Raton, p270
14. R. Quay, C. Moglestue, V. Palankovski, and S. Selberherr, ``A Temperature Dependent Model for the Saturation Velocity in Semiconductor Materials, " Materials Science in Semiconductor Processing, 3 (2000) ,pp149-155
15. T Oku, K.Hirata, H.Suzuki, K. Ouchi, H. Uchiyama, T.Taniguchi, K.Mochizuki and T.Nakamura. "Small scale InGaP/GaAs heterojunction bipolar transistors for high speed and low power integrated circuit applications", ". International Journal of High Speed Electronics and systems, 11 (2001) pp115-136