HIGH CURRENT DENSITY AND HIGH POWER DENSITY OPERATION OF ULTRA HIGH SPEED InP DHBTs

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Abstract

We report thermal design and characterization of high-current-density InP double heterojunction bipolar transistors (DHBT) designed for 150 GHz logic operation. Low thermal resistance DHBTs were obtained through use of InP collectors and composite InGaAs/InP subcollectors containing as little as 12.5 nm InGaAs for ohmic contacts. When biased at J_e = 8 mA/μm^2 and V_{ce} = 1.45 V (11.6 mW/μm^2 dissipation), producing 370 GHz f_τ and 459 GHz f_{max} [1], the devices exhibit only 69 °C emitter junction heating. The DHBTs operate without destruction at 10 mA/μm^2 at V_{ce} = 2 V, a 20 mW/μm^2 dissipation. We also report on the improvements obtained through reducing the InGaAs subcollector ohmic contact layer thickness for improved device heat-sinking into the substrate.

I. Introduction

To minimize $\Delta V_{logic} C_{cb}/I_c$ charging times in ~ 150 GHz logic ICs, InP DHBTs must operate at a current density of 5-10 mA/μm^2 [2], at 1.5 Volt V_{ce}, hence 7.5-15 mW/μm^2 power dissipation. The maximum current density is limited by the Kirk effect and by thermal failure through device heating. A high Kirk threshold is achieved by thinning the collector, appropriate choice of collector doping, and correct base-collector grade design, but is ultimately set by the transport properties of the collector material [2-6]. Low thermal resistance is achieved through the use of double heterojunction bipolar transistors using a high-thermal-conductivity InP collector, as opposed to SHBTs, where the collector is low-thermal-conductivity InGaAs. The subcollector and any underlying layers must contain only minimal thicknesses of low thermal conductivity InGaAs or InAlAs layers. Through employing these improvements, InP DHBTs can be operated at power densities exceeding 20 mW/μm^2.

II. Theory

HBTs generate heat primarily in the collector depletion region [3], and the upper portions of the subcollector, where energetic electrons undergo scattering. Thermal resistance between the collector and substrate must be minimized, hence low-thermal resistance collector and subcollector materials are necessary for effective heat transfer. InP, $In_{0.53}Ga_{0.47}As$, and InAlAs have respectively 65, ~5, and ~10 Watt/(K-meter) thermal conductivities at room temperature [5]. These room-temperature thermal conductivities decrease with lattice temperature and are ~20% poorer at 80 °C. Other ternary or quaternary materials have similarly poor thermal conductivily due to phonon Rayleigh scattering from the alloy disorder. Thermal conductivity also decreases with increased doping and defect density, but available data is limited [3,5]. Additionally, in HBTs configured for microwave probe testing, the large emitter metal contact pads provide significant additional heat removal, an effect much less significant for HBTs within an IC with its complex wiring environment [7]. If the collector thermal resistance is high and heat removal through the emitter metal is significant, then vertical heat flow through the high-thermal-resistance InGaAs base will result in an emitter junction substantially cooler than the collector junction. In that case, thermal resistance measured by the standard V_{be} technique [8-13] – which provides the temperature rise in the base-emitter junction - seriously underestimates the collector temperature [7].

Thickness (nm)	Material	Doping cm^{-3}	Description
40	$In_{0.53}Ga_{0.47}$ As	3E19 : Si	Emitter Cap
8	InP	3E19 : Si	Emitter
10	InP	8E17 : Si	Emitter
30	InP	3E17 : Si	Emitter
30	$In_{0.53}Ga_{0.47}$ As	8-5E19 : C	Base
20	$In_{0.53}Ga_{0.47}$ As	3E16 : Si	Setback
24	InGaAlAs	3E16 : Si	Base-Col Grade
3	InP	3E18 : Si	Delta doping
103	InP	3E16 : Si	Collector
12.5	$In_{0.53}Ga_{0.47}$ As	1.5E19 : Si	Sub Collector
300	InP	2E19 : Si	Sub Collector
Substrate	SI : InP		

Table 1: Layer composition for DHBT-19b [1]. Main differences in layer composition between samples are described in Table 2.

An InP collector is clearly superior to an InGaAs collector from a device self-heating perspective due to the higher

thermal conductivity of InP. HBTs incorporating a collector pedestal implant [16] also offers superior thermal resistance compared to mesa-etched collectors due to the confined heat flow in the latter case, especially if the base-collector junction is strongly undercut. The transferred substrate process, in which the main heat-flow is through the emitter, suffers from high thermal resistance due to the small base-emitter junction area [10].

Subcollector design faces several demands. The InGaAs subcollector layer serves as an etch-stop layer for the base-collector mesa etch and provides a lower collector contact resistance (10 Ω–μm^2) compared to contacts to N$^+$ InP (150 Ω–μm^2) [14]. Even at 25 nm thickness, such layers contribute substantially to DHBT thermal resistance. Below 5 nm thickness, the InGaAs layer does not provide a low contact resistance layer due to limited selectivity of the base-collector etch and to nonzero ohmic contact alloy depth. The overall thickness of the subcollector is limited by planarity considerations, while increased dislocation density is observed for doping above $3\cdot10^{19}$ cm^{-3}. Our recent DHBTs consequently use a subcollector having 300 nm InP and 12.5 nm InGaAs, doped at $1.5\cdot10^{19}$ and at $2\cdot10^{19}$ cm^{-3}. For metamorphic InP DHBTs grown on GaAs, thermal resistance is also strongly dependent on the thermal conductivity of the buffer layer, as reported by Kim *et al* [10-13], who showed low thermal resistance InP buffers provided superior heat conduction compared to alternative ternary buffers.

Device	Buffer (μm)	Tc (nm)	Tsc InGaAs (nm)	Tsc InP (nm)	θ_{JA} K/mW
DHBT-M1	-	200	25	125	2.5
DHBT-19b	-	150	12.5	300	1.8
DHBT-23	-	150	12.5	300	1.4
M-HBT-1	InAlP 1.5	200	50	125	7.6
M-HBT-2	InP 1.5	200	50	125	3.3
M-HBT-11	InP 1.5	200	25	300	3.1

Table 2: Thermal characteristics. M-HBTs are metamorphic devices; others are lattice matched. T_c is the collector depletion thickness, and T_{sc} the subcollector layer thicknesses. The emitter junction areas are 0.5 by 7 μm= 3.5μm^2 .

III. Experiment and Measurements

InP DHBTs [1,4,6,10-14] were fabricated in an all wet-etch mesa process with self-aligned base contacts. Passivation and planarization was done by using either polyimide or benzocyclobutene (BCB). Emitter contact widths vary 0.4-2 μm with a fixed emitter length of 8 μm. The base contact extends 0.5 μm on each side of the emitter metal. A 1 μm thick gold interconnect layer contacts device terminals. The interconnect contact to the emitter was 5.5 μm long for an 8 μm contact, providing significant heat removal through the emitter contact. In earlier designs [4] the interconnect contact was 2.5 μm long, but it was shown [7] that a wider contact provided superior heat removal at a negligible increase in parasitic capacitance. β varies from 12-41 and B_{VCEO} from 3.5-7.5 V depending on collector thickness, base design, and passivation.

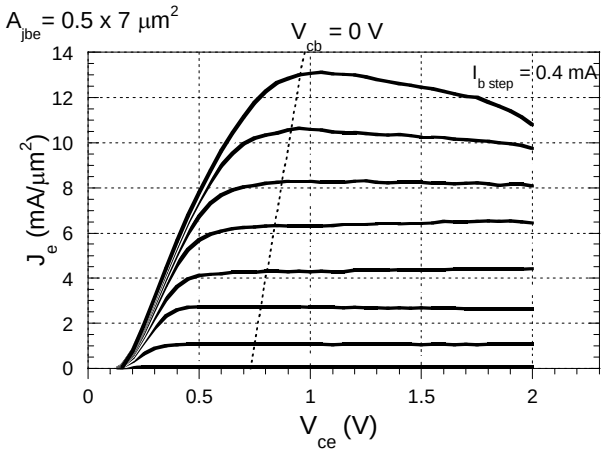

Figure 1: DHBT-19b DC characteristics. Note the thermally induced negative output conductance is only observed above 8 mA/μm^2. The subcollector was composed of 12.5 nm $In_{47}Ga_{53}As$ and 300 nm InP.

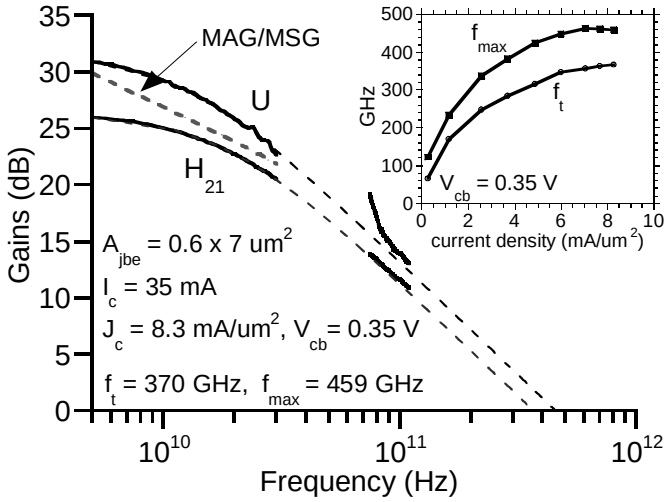

Figure 2: DHBT-19b peak RF characteristics [1]. Measurements were done in the 5-30 GHz and 75-110 GHz range.

The thermal resistance θ_{JA} (R_{th}) at the base-emitter junction was measured by observing the change in V_{be} at fixed I_c while varying the applied V_{ce} (1), [3,8-13].

$$\left.\frac{\partial V_{be}}{\partial V_{ce}}\right|_{\text{fixed } I_c} = \frac{\partial T}{\partial P}\frac{\partial P}{\partial V_{CE}}\left.\frac{\partial V_{be}}{\partial T}\right|_{\text{fixed } I_c} \cong \theta_{JA}\cdot I_C\phi \qquad (1)$$

ϕ is the thermoelectric feedback coefficient. The value of ϕ, which varies from 1.0 to 0.9 mV/K at the current densities used here, was referenced from Liu [8-9]. ϕ is a weakly material dependent parameter that changes little with emitter-base composition. ϕ measured for the InP/InGaAs HBTs reported here varies by as little as 4 % compared to AlGaAs/GaAs HBTs [8].

Thermal characteristics were measured on DHBTs grown on both InP and GaAs substrates, the latter using InP and InAlP metamorphic buffer layers [10-13]. For the

measurements, I_c was fixed at 5 mA and V_{ce} was spanned from 1.0-1.8 Volts. Table 2 and figures 3 and 4 summarize the thermal measurements. Thermal resistance is plotted as a function of base-collector junction area.

Reducing the InGaAs subcollector thickness from 25 nm to 12.5 nm reduced θ_{JA} from 2.5 to 1.4-1.8 K/mW for lattice-matched DHBTs with a 0.6 x 8 um^2 emitter junction area. For metamorphic DHBTs, reducing the InGaAs contribution of the subcollector from 50 to 25 nm reduces θ_{JA} from 3.3 to 3.1 K/mW for similar emitter dimensions. The two lattice matched DHBTs with 12.5 nm InGaAs subcollector contact thickness showed significantly different thermal resistance, with the BCB passivated device showing the highest gain as well as the lowest thermal resistance. Given the low thermal conductivity of both polyimide and BCB, this difference must be explained by other factors.

The thermal resistance for a 0.6 x 8 μm^2 DHBT exhibiting a 370 GHz f_τ and 459 GHz f_{max} (fig. 1-2) was 1.5 K/mW, indicating 69 °C temperature rise at J_c = 8 mA/μm^2 and V_{ce} = 1.45 V (11.6 mW/μm^2 dissipation) [1]. This particular DHBT is biased just below the Kirk current threshold. The device has a 150 nm collector and functions at 10 mA/μm^2 with V_{ce} = 2.0 V without destruction (fig. 1). While the low-current B_{VCEO} is 5.6 Volts, at higher current densities DHBTs on the same wafer exhibit thermally-driven failure at ~18 mW/μm^2 power density. The typical operating area used for an emitter coupled logic (ECL) digital circuit is shown in figure 5, illustrating a significant device operating safety margin. A static frequency divider was constructed using the same epitaxial layer structure and device layout—demonstrating a maximum operation to 118.7 GHz [15].

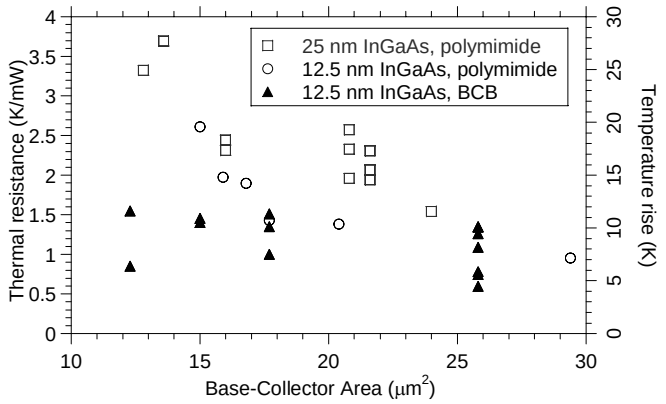

Figure 3: Measured thermal resistances for lattice matched HBTs. I_c= 5 mA, V_{ce}=1.5 V, P=7.5 mW

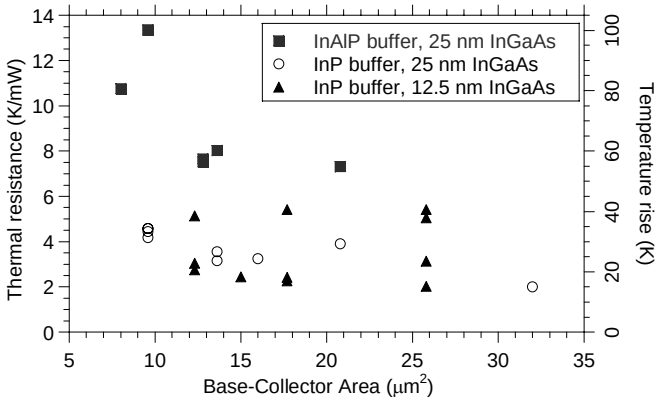

Figure 4: Measured thermal resistances for metamorphic HBTs. I_c= 5 mA, V_{ce}=1.5 V, P=7.5 mW.

V. Conclusion

InP DHBTs must operate at high current densities for both high f_t and f_{max}, and to minimize gate delay for high speed digital logic. At high current densities associated with high device speed, thermally-driven failure restricts allowable applied voltage to well below B_{VCEO}. The DC safe operating area (SOA) is a key device parameter. Using DHBTs with minimal InGaAs in the subcollector, we demonstrate DHBTs whose SOA well exceeds the bias conditions required for high transistor bandwidth.

Reducing the InGaAs subcollector thickness from 25 nm to 12.5 nm decreased the thermal resistance by 28-44 % for lattice matched DHBTs. For metamorphic DHBTs, reducing the subcollector thickness from 50 nm to 25 nm reduced the thermal resistance by 6 %. This trend illustrates the importance of eliminating or reducing the thickness of those epitaxial layers within a DHBT structure that would prevent next generation InGaAs/InP based HBT device operation from being Kirk effect limited (higher operating current and power density) as opposed to operating in a prematurely limited thermal regime.

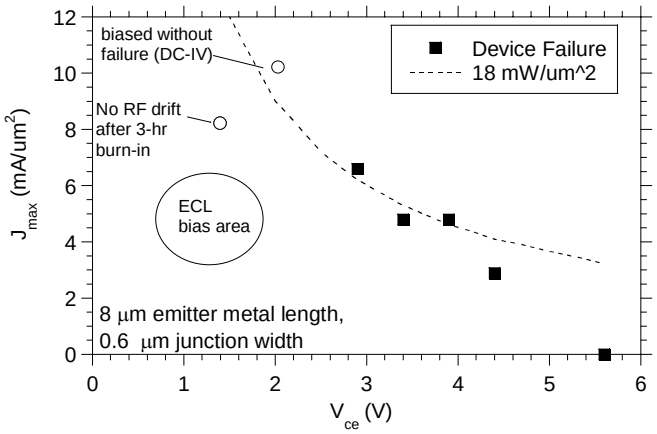

Figure 5: Measured bias range for device failure, as well as ECL bias area for a UCSB designed static frequency divider.

Acknowledgement

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