# A High IIP3, 50-GSamples/s Track and Hold Amplifier in $0.25\,\mu\mathrm{m}$ InP HBT Technology

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***Abstract*—A 50-GSamples/s track and hold amplifier (THA) is designed and fabricated in a $0.25\,\mu\mathrm{m}$ InP HBT technology. High speed switching functionality in the amplifier is achieved using Base-Collector diodes rather than switched-emitter-followers (SEF). Operating with $-5\,\mathrm{V}$ and $-2.5\,\mathrm{V}$ supplies, it achieves IIP3 more than $+16\,\mathrm{dBm}$ up to $22\,\mathrm{GHz}$. An $HD3$ of $-30.3\,\mathrm{dB}$ is measured at $+7.5\,\mathrm{dBm}$ input power which is P1dB point of THA at $15\,\mathrm{GHz}$. Time domain measurement verifies the sampling rate of 50-GSamples/s in the THA.**

***Index Terms*—Mixed analog digital integrated circuits, Indium Phosphide, Analog-digital conversion, Sampled data circuits.**

## I. Introduction

The usage of digital receivers in optical transceivers and millimeter-wave radios is growing rapidly which is consequently requiring high speed Analog-to-digital converters (ADCs) [1]. The overall performance of these systems is strongly dependent to the performance of ADCs in terms of bandwidth, sampling rate, resolution and linearity. Therefore, these ADCs needs to be designed carefully. Design of high speed Track and Hold amplifier (THA) is one of the challenging bottlenecks in the design of high sampling-rate ADCs.

Recently reported high sampling-rate THAs which are either SiGe-based [1]-[3] or InP-based [4],[5] are designed using the switched emitter followers. The THA presented in this paper is using a Base-Collector diode rather than a switched emitter follower stage. Here we present a THA that operates at 50 GSamples/s and shows an IIP3 greater than $+16\,\mathrm{dBm}$ up to $22\,\mathrm{GHz}$. This THA has the fastest sampling rate in InP HBT technology. We briefly describe the circuit diagram and operation of the circuit in Sec III. Then, the measurement results are presented in Sec.IV.

## II. $0.25\,\mu\mathrm{m}$ Indium Phosphide HBT Process

The THA IC reported in this paper uses the $0.25\,\mu\mathrm{m}$ InP HBT technology with a $\sim 4.5\,\mathrm{V}$ breakdown voltage. A single HBT has a peak bandwidth of $f_{max} = 700\,\mathrm{GHz}$ and $f_T = 400\,\mathrm{GHz}$ at the amplifiers quiescent bias of $J_e = 5.5\,\mathrm{mA}/\mu\mathrm{m}^2$.

A four-metal interconnect stack is used in the fabrication of THA. Compact, stacked interconnect vias provide access from the top layer of metal interconnect for signal ($3\,\mu\mathrm{m}$ thick) to the three lower layers (each $1\,\mu\mathrm{m}$ thick). Interconnects are separated by $1\,\mu\mathrm{m}$ BCB interlayer dielectric layers.

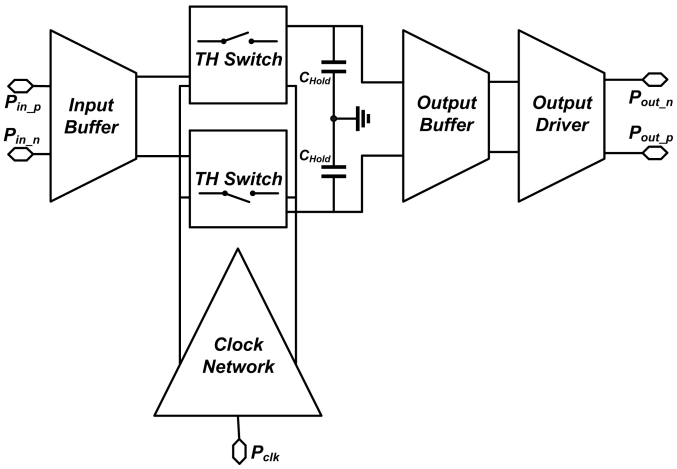


Fig. 1. Conceptual block diagram of the presented THA.

MIM capacitors are $0.3\,\mathrm{fF}/\mu\mathrm{m}^2$ and thin-film resistors are $50\,\Omega/\mathrm{square}$.

## III. Track and Hold Amplifier Design

The conceptual block diagram of the THA presented in this paper is shown Fig. 1 where the track and hold switches are operating with the sampling rate defined by the clock network. $50\,\Omega$ match in the input and output is provided by input buffer and output driver stages. The input buffer is also designed to provide the high linearity in the input (IIP3) of the amplifier.

Figure 2 represents the schematic of the input buffer, two track and hold switches and the output buffer. The main core of the input buffer ($Q_{1\text{-}6}$) is consisted of two degenerated differential pairs where the linearity error caused by $V_{BE}$ modulation of $Q_{1,2}$ is compensated by the one of $Q_{5,6}$ and results a high linearity buffer.

The design of track and hold switches is benefited of using high speed Base-Collector (BC) diodes rather than switched emitter follower stages which does not suffer from instability issues of emitter followers and consequently reduces the excessive peaking in the AC response of the circuit. The operation of the track and hold switches is explained as follows:

1) In the track mode, transistor $Q_9$ is conducting and its $6\,\mathrm{mA}$ current is drawn from the BC diode which cause the input signal to appear across the hold capacitance

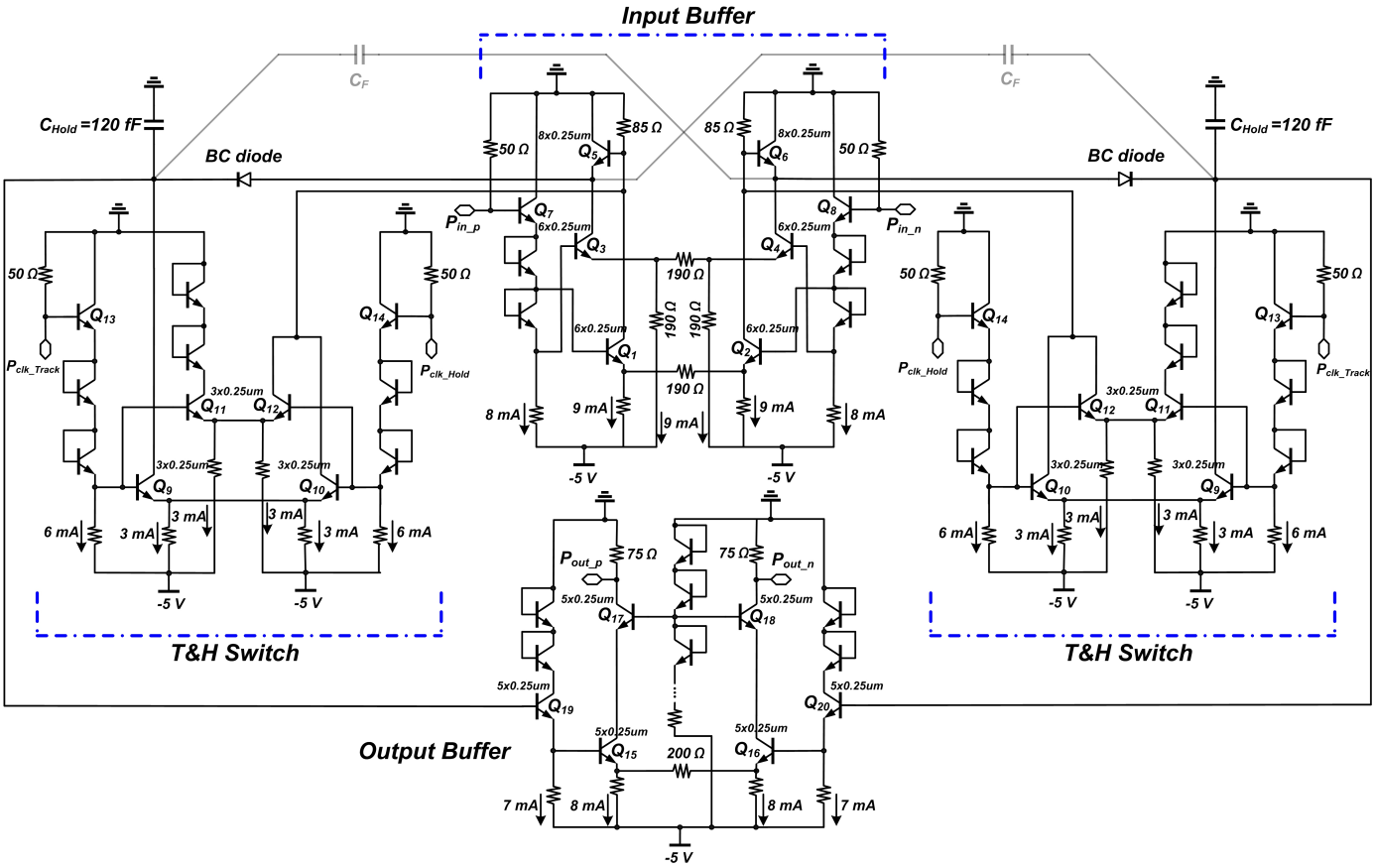


Fig. 2. Circuit schematic of the input buffer cascaded with two T&H switches and the output buffer.

$(C_{hold})$. The value of MIM hold capacitance is selected as 120 fF based on the design methodology reported in [2].

2) In the hold mode, $Q_{10}$ and $Q_{12}$ are conducting and a total current of 12 mA is drawn from the 85 Ω load resistor of the input buffer and provides a voltage drop of 1 V across that. This voltage drop completely turns off the BC diode whose $V_{BE\text{-}on}$ is 0.8 V. Large swings of the input signal in the output of input buffer turns on the BC diode if it is partially turned off. The feedthrough cancellation capacitors $(C_F)$ are selected at the same amount of the BC diode capacitance in this design.

The output buffer of THA is designed to be always in on state which has the drawback of signal droop during the hold mode. However, as the target of this work was to design a Sample & Hold circuit where two THA are cascaded and work in opposite states, by turning off the output buffer in the hold mode, the valid data in the output of the first THA which should be read by the second THA, becomes inaccessible.

The core of the output driver [shown in Fig.1] is a degenerated differential pair with 50 Ω loads and 120 Ω degeneration resistor with the tail current of 35 mA while another differential pair with 35 mA current is preceding that.

The clock network of THA is consisted of cascaded Cherry-Hooper amplifier with differential common emitter stages

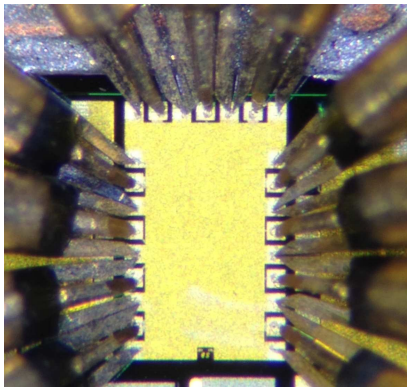

Fig. 3. Die-photo of the THA ($0.675 \times 1.075\,\mathrm{mm}^2$)

where it converts the single-ended $150\,\mathrm{mV_{p\text{-}p}}$ clock signal to a differential signal with amplitude of $300\,\mathrm{mV_{p\text{-}p}}$ applied to the track and hold switches. The wide bandwidth of the Cherry-Hooper amplifier achieves a high speed clock network of 50 GSamples/s.

## IV. Measurement Results

The THA chip shown in Fig. 3, consumes 130 mA and 220 mA from power supplies of −5 V and −2.5 V, respectively. The clock network and the output driver are drawing

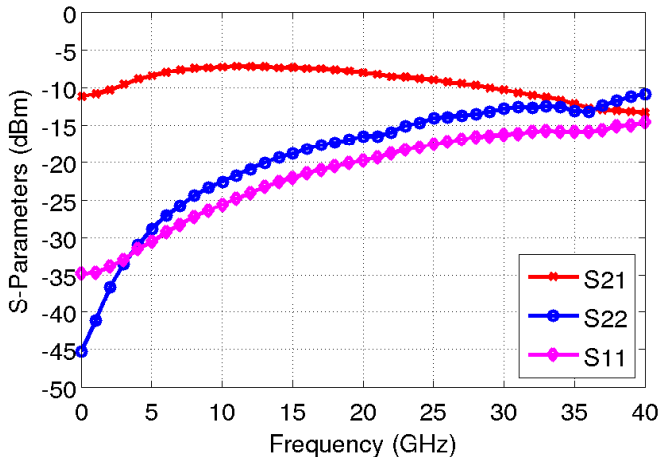


Fig. 4. Measured single-ended THA input return loss ($S_{11}$), output return loss ($S_{22}$) and transmission ($S_{21}$)

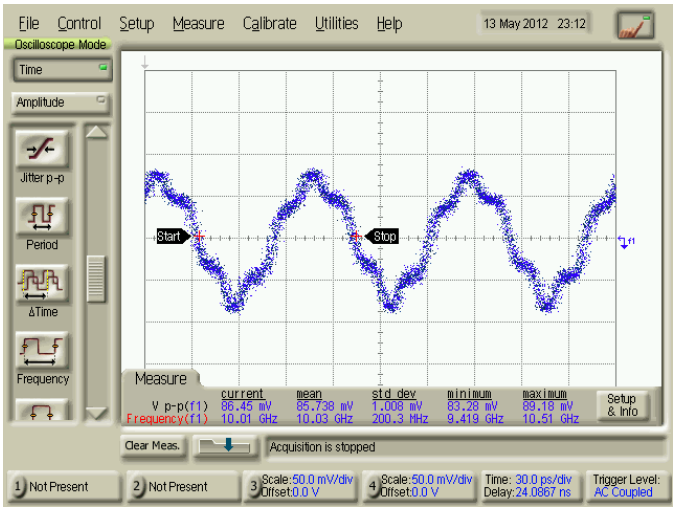


Fig. 5. Measured differential output of a 10 GHz input signal sampled with a 50 GSample/sec sampling rate

150 mA and 70 mA respectively, from the −2.5 V supply.

2-port RF measurements of the THA were performed from 100 MHz to 40 GHz using an Agilent PNA-X N5245 network analyzer after LRRM calibration. The non-stimulated input and output ports were terminated by a 50-Ohm termination. The single-ended S-parameters in the track mode are shown in Fig. 4.

Time-domain measurements were conducted using Rohde & Schwarz SMF 100A signal generator for the input signal and Agilent E8257D-M50 50 GHz signal generator for the clock source. Figure 5 which has been captured by an Agilent 86100A wide-band Oscilloscope, shows a differential output signal at 10 GHz which is being sampled by 50 GSample/s sampling rate.

Figure 6 shows the spectral content of a two tone test at 18 GHz. Using a Rohde & Schwarz FSU 20 Hz-46 GHz spectrum analyzer, the fundamental signal powers and their

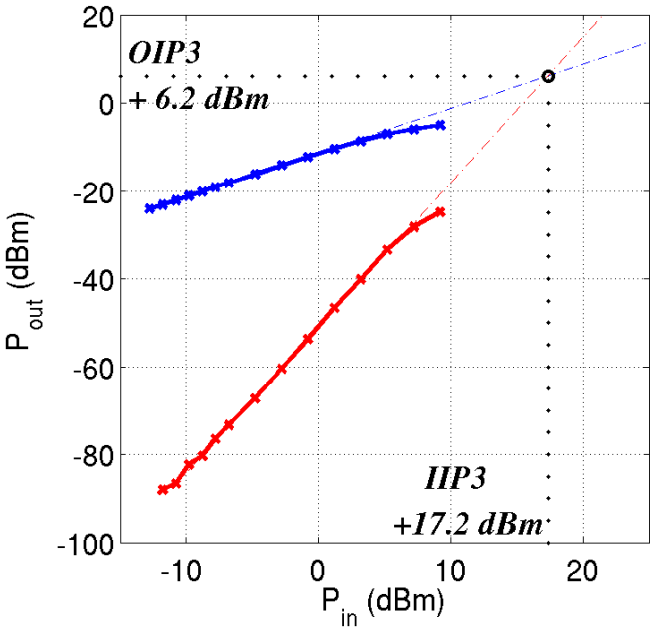


Fig. 6. IP3 measurement by applying two frequency tones at 18 GHz and 18.100 GHz. The output power ($P_{out}$) is measured from the Spectrum Analyzer under the condition of Res. BW = V. BW = 10 kHz and RF Attn = 0 dB.

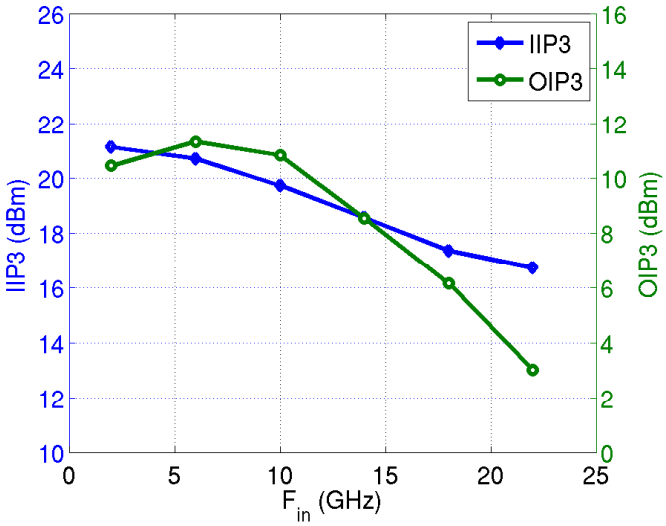


Fig. 7. Measured IP3 versus input frequency.

corresponding third-order intermodulation products were captured by sweeping the input power over the range of −10 to +10 dBm. The extrapolated IIP3 and OIP3 are +17.2 dBm and +6.2 dBm, respectively. Using the same measurement method, IIP3 and OIP3 of the THA has been extracted and shown in Fig. 7 over the input frequency range of 2 to 22 GHz.

The harmonic distortion of THA has been investigated by measuring the spectral content of the single-ended output for a 15 GHz input signal by sweeping its input power up to the P1dB of THA at this frequency. Figure 8 shows an $HD2$ and an $HD3$ of −15.5 dB and −30.3 dB, respectively at the input

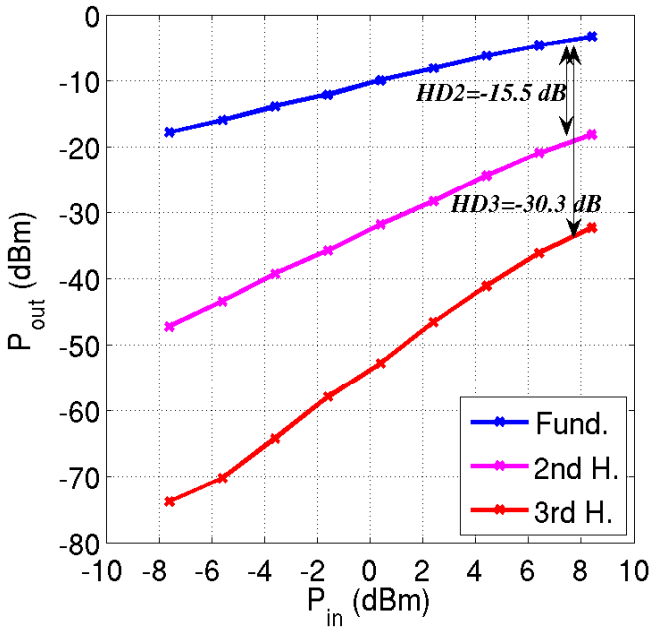


Fig. 8. Single-ended spectral characterization at input signal frequency of 15 GHz.

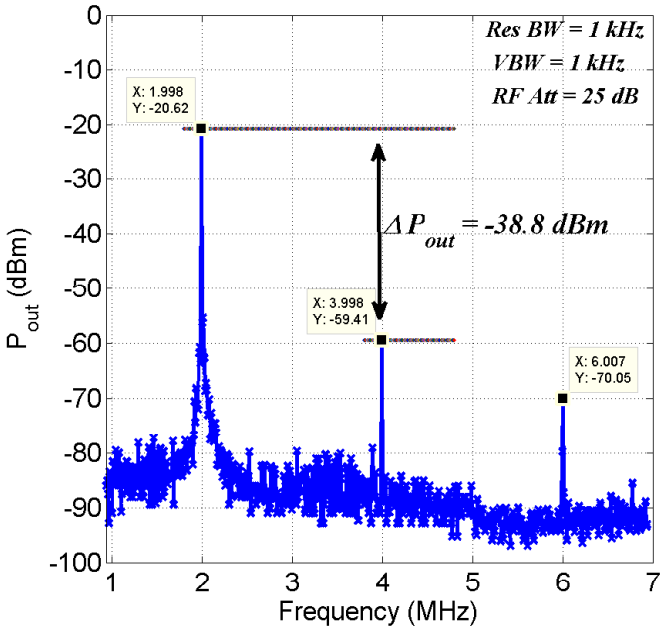


Fig. 9. Single-ended spectral characterization at input signal frequency of 15 GHz.

power of $+7.5\,\mathrm{dBm}$ which is the P1dB compression point of THA at $15\,\mathrm{GHz}$.

Figure 9 presents the spectral characteristics of a beat frequency test with $f_{in} = f_s + \Delta f$ where $f_s = 40\,\mathrm{GHz}$ and $\Delta f = 2\,\mathrm{MHz}$ at an input power of $+3\,\mathrm{dBm}$ with the $3^{rd}$-order harmonic distortion of $-38.8\,\mathrm{dB}$.

## V. Conclusion

A $50$ GSample/s THA has been designed using fast Base-Collector diodes and fabricated in $0.25\,\mu\mathrm{m}$ InP HBT technology. The reported THA has the highest sampling rate in the InP HBT technology. Time-domain measurement at $50$ GSample/s sampling rate is presented for a $10\,\mathrm{GHz}$ signal. The THA achieves IIP3 more than $+16\,\mathrm{dBm}$ up to $22\,\mathrm{GHz}$ of the input signal frequency which makes it a proper choice for high speed ADC applications. An example of spectral characterization at $15\,\mathrm{GHz}$ shows an $HD3$ of $-30.3\,\mathrm{dB}$ at the P1dB input power of THA which is $+7.5\,\mathrm{dBm}$. Finally, the beat frequency test at $40\,\mathrm{GHz}$ with $\Delta f = 2\,\mathrm{MHz}$ exhibits an $HD3$ of $-38.8\,\mathrm{dB}$.

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