Ultra High Frequency Static Dividers > 150 GHz in a Narrow Mesa InGaAs/InP DHBT Technology

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Abstract--A static frequency divider with a maximum clock frequency > 150 GHz was designed and fabricated in a narrow mesa InP/$In_{0.53}Ga_{0.47}As$/InP DHBT technology. The divider operation is fully static, operating from f_{clk} = 3 GHz to 152.0 GHz while dissipating 594.7 mW of power in the circuit core from a -4.07 Volt supply. The circuit employs single-buffered emitter coupled logic (ECL) and inductive peaking. The transistors have an emitter junction width of 0.5 mm and a 3.0 collector-to-emitter area ratio. A microstrip wiring environment is employed for high interconnect density, and to minimize resonances and impedance mismatch at frequencies > 100 GHz.

INTRODUCTION

InP based double heterojunction bipolar transistors (DHBT) have been aggressively pursued because of their superior material transport properties over SiGe [1]. This is demonstrated by the increased value of small-signal unity current gain f_t and unity power gain f_{max} that InP devices possess over SiGe at a given scaling generation [2,3]. The minimum gate delay of a digital IC in contrast is not determined by an algebraic function of f_t and f_{max}, but instead by a set of time constants of which $C_{cb}DV_{logic}/I_c$ is a major contributor. As Si based processing technologies are much more advanced than InP, SiGe HBTs have been scaled to dimensions where the reduction in base-collector capacitance C_{cb} and increased operating current density J_e are such that the speed of digital circuits in both material systems have been comparable.

Over the past year techniques to aggressively scale InP devices to submicron features vertically and laterally [4] has resulted in record performance for f_t and f_{max} [3,5]. Applications for these devices include mixed signal ICs for digital radar and advanced communication systems--with circuit transistor counts approaching 10,000 devices [6]. Efforts to simultaneously produce submicron InP HBTs and have high circuit device yield > 10,000 are underway. The first step in the realization of such a process has lead to the design and fabrication of static frequency dividers—a digital performance benchmark for a given device technology. Prior to this work, the highest reported value for a static frequency divider in an InP HBT technology was 118.7 GHz [7]. For a SiGe based HBT technology the highest reported value for a static frequency divider is 96 GHz [8]. Here we report a static frequency divider in a divide by 2 topology, with a maximum operating clock frequency of 152.0 GHz.

DEVICE AND CIRCUIT DESIGN

When designing an HBT for use in emitter coupled logic (ECL), it should be done with emphasis on minimizing the major delay term $C_{cb}DV_{logic}/I_c$, where $DV_{logic} \approx 300$ mV for ECL. If device operation can be maintained at the Kirk threshold current density J_{Kirk} (current density at which the electric field at the base-collector junction becomes zero), the delay $C_{cb}DV_{logic}/I_c$ scales proportionally to the collector thickness, T_c. To increase digital circuit speed, the collector must be thinned, but as $J_{Kirk} \propto T_c^{-2}$, the collector should not be thinned to where the voltage drop $I_e \times R_{ex} \cong$

$J_{Kirk} \times r_c \propto T_c^{-2}$ on the emitter parasitic resistance becomes a significant portion of DV_{logic} [9]. By simultaneously thinning the collector and reducing the emitter contact resistance r_c, circuit speed will improve.

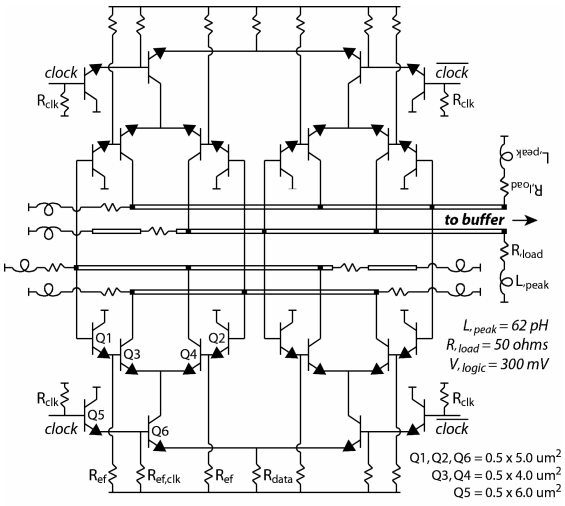

Fig 1: Schematic of static frequency divider

The circuit is a master-slave flip-flop with the output cross-coupled to the input to generate $f_{clk}/2$ frequency division of the clock source (fig. 1). Unlike the divider reported in [8], this circuit employs single-buffered emitter coupled logic (ECL) which consumes less power than E^2CL. Bias currents are established using pull-down resistors, not current mirrors, to reduce the number of active devices and reduce capacitive loading. The HBTs in the divider operate at $J_e \cong J_{Kirk}$ for their respective base-collector bias voltage V_{cb}. As explained by [9], if the devices in the circuit can be operated at J_{Kirk} for a given collector thickness T_c, then the major contributor to the gate delay $C_{cb}\Delta V_{logic}/I_c$ is minimized. To decrease the interconnect delays, the switching signal path is kept short—doubly-terminated with 50 Ω in a transmission-line bus with peaking inductance, located at the center of the IC. The output of the divider drives a differential-pair that serves as an output buffer to minimize loading to the divider signal bus. The total divider area is 493 x 473 μm^2 and contains 24 transistors.

CIRCUIT FABRICATION

The transistors in the circuit are formed from an MBE layer structure grown by commercial vendor IQE Inc., with a highly doped 40 nm InGaAs base and 150 nm collector [3] and are fabricated in a triple-mesa process with both active junctions defined by selective wet and dry etch chemistry. Details of the base and collector layer design can be found in [10]. Benzocyclobutene (BCB) passivates devices and planarizes the wafer after device formation. The ensuing level of metal deposition is used for circuit interconnects and making electrical contacts to the transistors and resistors. Thin-film-dielectric microstrip wiring is employed for its predictable characteristics, controlled impedance, and ability to maintain signal integrity at very high frequencies within dense mixed-signal ICs. The associated ground plane also eliminates signal coupling through on-wafer ground-return inductance. This is realized by placing 3 μm of BCB above the signal interconnects (M1) and using the top-most interconnect layer (M3) as a large ground plane (fig. 2).

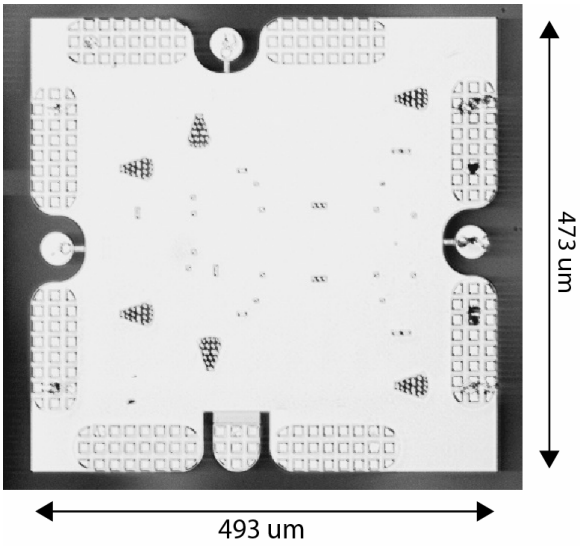

Fig 2: IC micrograph of the divide by 2

CIRCUIT AND DEVICE MEASUREMENTS

	units	Q3, Q4	Q1, Q2	Q6	Q5
size	μm^2	0.5 x 4	0.5 x 5	0.5 x 5	0.5 x 6
J_e	$mA/\mu m^2$	6.0	4.0	4.8	3.3
C_{cb}/I_c	ps / V	0.59	0.99	0.59	0.86
V_{cb}	V	0.6	0	0.6	1.7
f_t	GHz	301	260	301	280
f_{max}	GHz	358	268	358	280

Table 1: Bias conditions and discrete device operation for HBTs within the divider

RF device measurements were performed on HBTs like those in the circuit (fig 1) and the results are summarized in table 1--listing the respective operating J_e, C_{cb}/I_c, V_{cb}, f_t, and f_{max} for these devices. To minimize divider gate delay, the HBTs in the circuit are biased at or slightly higher than $J_{Kirk} \cong J_{design}$ for minimum C_{cb}/I_c ratio [9].

Divide by 2 measurements for clock frequencies ranging from 3 to 152.0 GHz were performed without the use of an input clock driver to the divider core. Because of this, an offset voltage V_{offset} = -0.6 V at all clock input devices is required to maintain their V_{cb} reversed biased while the clock signal is applied. All measurements took place with the wafer chuck at room temperature, 25°C. At low frequencies, a DC-40 GHz frequency synthesizer directly drives the clock input. The divider was clocked as low as 3 GHz to demonstrate that it is fully static (fig 3). For V-band measurements, the synthesizer drives a

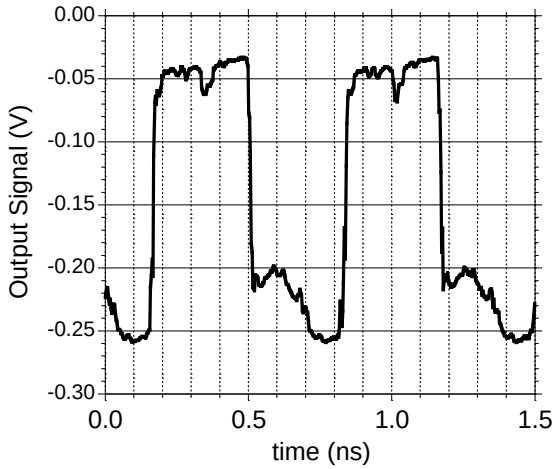

Fig 3: Output waveform @ 1.5 GHz, f_{clk} = 3 GHz
This measurement confirms the divider is fully static

frequency tripler for testing between 50-75 GHz using a WR-15 wafer-probe. For W-band measurements, the synthesizer drives a 20-40 GHz amplifier, whose output drives a frequency tripler for testing between 75-110 GHz using a WR-10 wafer-probe. For 130-156 GHz measurements, the synthesizer signal is quadrupled using a Virginia Diode (VDI) doubler chain with the output delivered on-wafer with a waveguide-coupled G-band wafer probe. The output spectrum of the divide by 2 operating at 150 GHz and 152 GHz is shown in figures 4 and 5. The measured signal drive power at the probe tip is ≈ 11 dBm. At higher frequencies, the divider failed.

While testing at 150 GHz and 152 GHz, the output power was split in order to monitor the

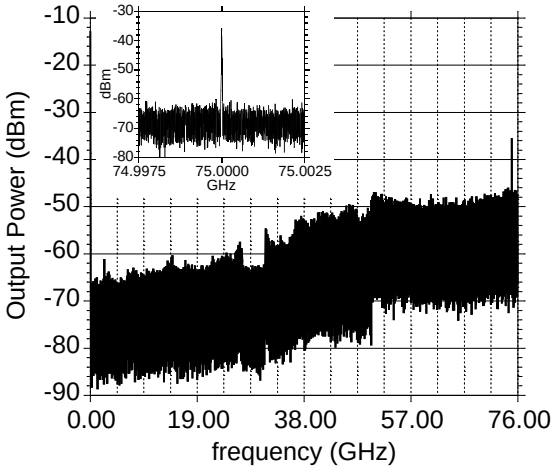

Fig 4: Output signal @ 75 GHz, f_{clk} = 150.0 GHz

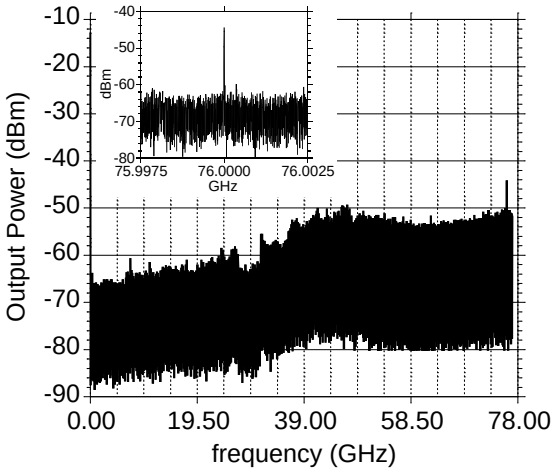

Fig 5: Output signal @ 76 GHz, f_{clk} = 152.0 GHz

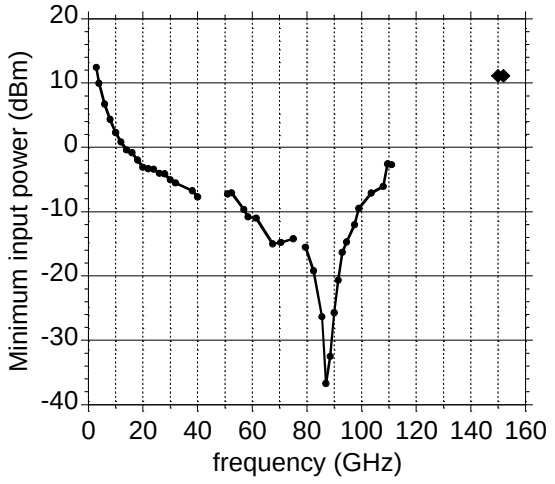

Fig 6: Variation of input sensitivity with frequency

output spectrum from DC-50 GHz and 50-75 GHz simultaneously. The estimated attenuation from the divider output to the spectrum analyzer is approximately 22 dB at 75 GHz. Correcting for these losses, the *approximate* output power is -13 dBm with a 150 GHz input and -21 dBm with a 152 GHz input.

Sensitivity measurements were performed from 3 to 152 GHz on the divide by 2 circuit (fig. 6). The self-oscillation frequency of the divider is ≈ 87 GHz.

CONCLUSION

Fully static divide by 2 circuits have been designed and fabricated having a 152 GHz maximum clock frequency in a narrow mesa InP/$In_{0.53}Ga_{0.47}As$/InP DHBT technology. The circuit transistors operate at $J_e \cong J_{Kirk}$ for their respective V_{cb} bias to minimize gate delays associated with $C_{cb}\Delta V_{logic}/I_c$, and the total power dissipation of the divider with and without the output buffer is 659.8 mW and 594.7 mW respectively.

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