# InGaAs–InP DHBTs for Increased Digital IC Bandwidth Having a 391-GHz $f_T$ and 505-GHz $f_{\max}$

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***Abstract*—InP–In$_{0.53}$Ga$_{0.47}$As–InP double heterojunction bipolar transistors (DHBT) have been designed for use in high bandwidth digital and analog circuits, and fabricated using a conventional mesa structure. These devices exhibit a maximum 391-GHz $f_\tau$ and 505-GHz $f_{\max}$, which is the highest $f_\tau$ reported for an InP DHBT—as well as the highest simultaneous $f_\tau$ and $f_{\max}$ for any mesa HBT. The devices have been aggressively scaled laterally for reduced base–collector capacitance $C_{\rm cb}$. In addition, the base sheet resistance $\rho_s$ along with the base and emitter contact resistivities $\rho_c$ have been lowered. The dc current gain $\beta$ is ≈36 and $V_{\rm BR,CEO} = 5.1$ V. The devices reported here employ a 30-nm highly doped InGaAs base, and a 150-nm collector containing an InGaAs–InAlAs superlattice grade at the base–collector junction. From this device design we also report a 142-GHz static frequency divider (a digital figure of merit for a device technology) fabricated on the same wafer. The divider operation is fully static, operating from $f_{\rm clk} = 3$ to $142.0$ GHz while dissipating ≈ 800 mW of power in the circuit core. The circuit employs single-buffered emitter coupled logic (ECL) and inductive peaking. A microstrip wiring environment is employed for high interconnect density, and to minimize loss and impedance mismatch at frequencies >100 GHz.**

***Index Terms*—Heterojunction bipolar transistor (HBT).**

## I. Introduction

DEVELOPMENT of digital logic and mixed-signal systems operating at higher clock speeds and bandwidth require continued improvement in transistor performance [1], [2]. Target heterojunction bipolar transistor (HBT) specifications for 160 Gb/s systems include an $f_\tau$ and $f_{\max}$ higher than 440 GHz, a breakdown voltage exceeding 3 V, operating current density greater than 10 mA/$\mu$m$^2$ at a base–collector voltage $V_{\rm cb} = 0.0$ V, and low base–collector capacitance ($C_{\rm cb}/I_c < 0.5$ ps/V) [3]. When designing an HBT for use in emitter coupled logic (ECL), it should be done with emphasis on minimizing the major delay term $\tau = C_{\rm cb}\Delta V_{\rm logic}/I_c$, where $\Delta V_{\rm logic} \approx 300$ mV for ECL. If the operating point for these devices can be maintained at the Kirk threshold current density $J_{\rm Kirk}$ for the respective $V_{\rm cb}$ (the bias for which the electric field at the base–collector junction becomes zero), the delay $C_{\rm cb}\Delta V_{\rm logic}/I_c$ scales proportionally to the collector thickness, $T_c$. To increase digital circuit speed, the collector must be thinned, but as $J_{\rm Kirk} \propto T_c^{-2}$, the collector should not be thinned to where the voltage drop on the emitter parasitic resistance $\Delta V_{\rm parasitic} = I_e \cdot R_{\rm ex} \cong J_{\rm Kirk} \cdot \rho_c \propto T_c^{-2}$ becomes a significant portion of $\Delta V_{\rm logic}$. Recently fabricated state-of-the-art InP DHBTs with a 150-nm collector used in digital benchmark circuits [4] have an emitter $\rho_c \approx 20\ \Omega \cdot \mu$m$^2$ and operate at $J_e \approx 6$ mA/$\mu$m$^2$—producing a $\Delta V_{\rm parasitic} \approx 120$ mV. As the collector is thinned to 100 nm, $J_{\rm Kirk}$ will increase to >10 mA/$\mu$m$^2$ and without reductions to $\rho_c$, $\Delta V_{\rm parasitic}$ will be >200 mV—a considerable fraction of $\Delta V_{\rm logic}$, and circuit bandwidth will suffer. By simultaneously thinning the collector *and* reducing the emitter contact resistance $\rho_c$, device and circuit bandwidth will increase.

In addition to vertical scaling of the collector thickness, lateral scaling of the base and collector junctions is necessary to reduce delays associated with $R_{\rm bb}$ and $C_{\rm cb}$. For our mesa HBT process, this scaling is limited by alignment registration tolerance and by the ohmic transfer length $L_T$ of the base contact. The minimum base contact width $W_B$ feasible in our laboratory is 0.3 $\mu$m based on typical base contact resistivity and collector undercut. Scaling $W_B$ any further than this will increase $R_{\rm bb,cont} \propto \coth(W_B/L_T)$ at a rate greater than the reduction of $C_{\rm cb} \propto W_B$, and the device and circuit performance overall will be poorer.

Prior to this letter, the highest $f_\tau$ reported for an InP DHBT was 370 GHz with an $f_{\max}$ of 459 GHz [5], having a 30-nm base and 150-nm collector. The highest reported $f_{\max}$ for a mesa HBT is 519 GHz, with a 252 GHz $f_\tau$ [6], having a 40-nm base and 150-nm collector. Here we report a 391-GHz $f_\tau$ and 505-GHz $f_{\max}$ InP DHBT—the highest $f_\tau$ reported for such a device.

## II. Design, Growth, and Fabrication

The epitaxial material was grown by commercial vendor IQE Inc. on a 3-in SI-InP wafer and the HBTs were fabricated in an all wet etch, standard triple mesa process. The device layer structure is similar to that reported in [7] and details of the base and collector design are given in [8]. The improvements in the device design here compared to [5] include the use of an indium rich InGaAs emitter cap doped at $3 \cdot 10^{19}$ cm$^{-3}$ for reduced emitter contact resistance, and slightly reduced base doping

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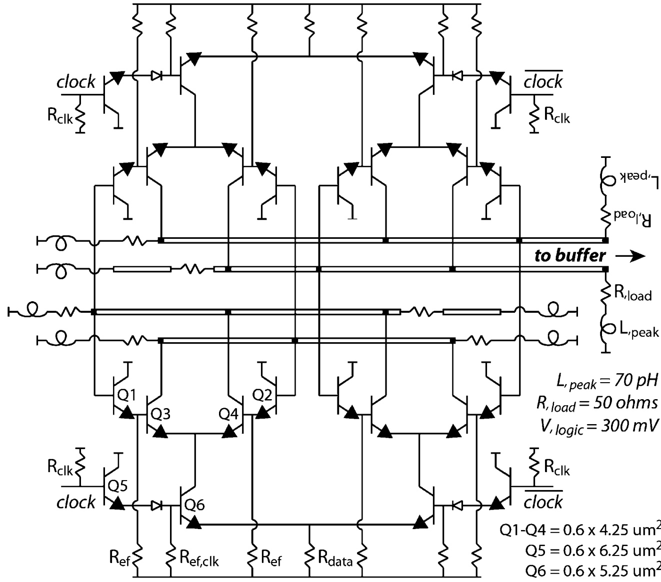


Fig. 1. Schematic of static frequency divider with design details—including the values of circuit load resistance $R_L$, peaking inductance $L_{\rm peak}$, and the emitter junction areas $A_{\rm je}$.

combined with the use of benzocyclobutene (compared to polyimide for [5], [8]) for device passivation to increase dc current gain $\beta$. This lighter doping also brings with it an increased hole mobility $\mu_p$, producing an overall increased doping-mobility product and, hence, lower base sheet resistance—$\mu_p \approx 52$ and 61 cm$^2$/V· s for a $8 \cdot 10^{19} - 5 \cdot 10^{19}$ cm$^{-3}$ [5], [8] and $7 \cdot 10^{19} - 4 \cdot 10^{19}$ cm$^{-3}$ doping grade, respectively.

The static frequency divider is a master-slave flip-flop with the output cross-coupled to the input to generate $f_{\rm clk}/2$ frequency division of the clock source (Fig. 1). The divider design techniques are similar to those reported in [4], with details provided in Fig. 1. Thin-film dielectric microstrip wiring is employed by the RF device test structures and circuit interconnects for its predictable characteristics, controlled impedance, and reduced line coupling at very high frequencies within dense mixed-signal ICs. This is realized by placing 3.5 $\mu$m of benzocyclobutene (BCB) above the signal interconnects (M1) and using the top-most interconnect layer (M3) as a large ground plane.

## III. Results

Standard transmission line measurements (TLM) show the base $\rho_s \approx 564\ \Omega$ and $\rho_c \approx 9.6\ \Omega \cdot \mu\mathrm{m}^2$, and the collector $\rho_s \approx 11.9\ \Omega$ and $\rho_c \approx 5.4\ \Omega \cdot \mu\mathrm{m}^2$. Scanning electron microscope images of the TLMs were taken to account for variance between the photomask and fabricated spacings to ensure accurate extraction of $\rho_s$ and $\rho_c$. The emitter $\rho_c$ was determined from RF parameter extraction $(\mathrm{Re}(Y_{12})^{-1} = R_{\rm ex} + R_{\rm bb}/\beta + (NkT)/(qI_c)$ and $\approx 10.1\ \Omega \cdot \mu\mathrm{m}^2$. This emitter $\rho_c$ is consistent with other devices on the wafer with varying emitter dimensions. The HBTs have $\beta \approx 36$, a common-emitter breakdown voltage $V_{\rm BR,CEO} = 5.1$ V (at $I_c = 50\ \mu$A), and a collector leakage current $I_{\rm cbo} = 108$ pA (at $V_{\rm cb,\,offset} = 0.3$ V). A plot of the common-emitter current–voltage (*I–V*) and Gummel characteristics are shown

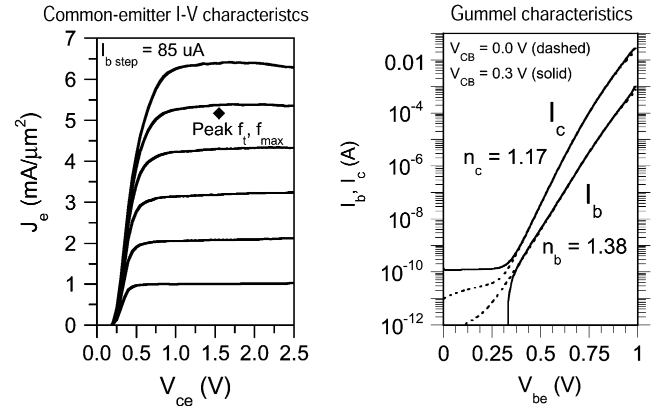


Fig. 2. Common-emitter *I–V* characteristics and Gummel characteristics. Device junction dimensions $A_{\rm je} = 0.6 \times 4.25\ \mu\mathrm{m}^2, A_{\rm jc} = 1.3 \times 6.5\ \mu\mathrm{m}^2$.

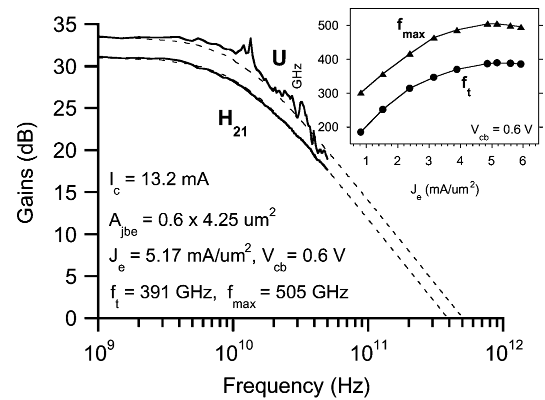


Fig. 3. Measured microwave gains.

in Fig. 2. DC-50 GHz RF measurements were carried out after performing an off wafer line-reflect-reflect-match calibration on an Agilent 8510 XF network analyzer. An on-wafer open circuit pad structure identical to the one used by the devices was measured after calibration in order to de-embed this associated capacitance from the device measurements. A maximum 391-GHz $f_\tau$ and 505-GHz $f_{\max}$ (Fig. 3) at $I_c = 13.1$ mA and $V_{\rm ce} = 1.54$ V ($V_{\rm cb} = 0.60$ V, $J_e = 5.17$ mA/$\mu$m$^2$, $C_{\rm cb}/I_c = 0.51$ ps/V) was determined from $|H_{21}|$ and Mason's unilateral gain $|U|$—extrapolated at $-20$ dB/dec using a single-pole fit to the small-signal hybrid-$\pi$ equivalent circuit (Fig. 4) for the device. This device has a $0.6 \times 4.25\ \mu\mathrm{m}^2$ emitter semiconductor junction area $A_{\rm je}$ and a 0.3 $\mu$m wide base contact width $-1.3\ \mu$m base mesa width, and collector to emitter mesa width ratio $W_c/W_e = 2.17$. Note that the $C_{\rm cbi}/C_{\rm cbx}$ ratio of the model is smaller than expected from geometry [9], [3] an effect which may be due in part to capacitance cancellation [10], [11], [3]. Peak $f_\tau$ and $f_{\max}$ is between $J_e = 5.0$–$5.5$ mA/$\mu$m$^2$ at $V_{\rm cb} = 0.6$ V for different HBTs on the wafer.

Divide by two measurements for clock frequencies ranging from 3 to 142.0 GHz were performed without the use of an input clock driver to the divider core. Because of this, an offset voltage $V_{\rm offset} = -0.6$ V at all clock input devices is required to maintain their $V_{\rm cb}$ reverse biased while the clock signal is applied. All measurements took place without any surface cooling and with the wafer chuck temperature at 25 °C. The divider was clocked as low as 3 GHz ($P_{\rm clk} \approx 13$ dBm) to demonstrate that

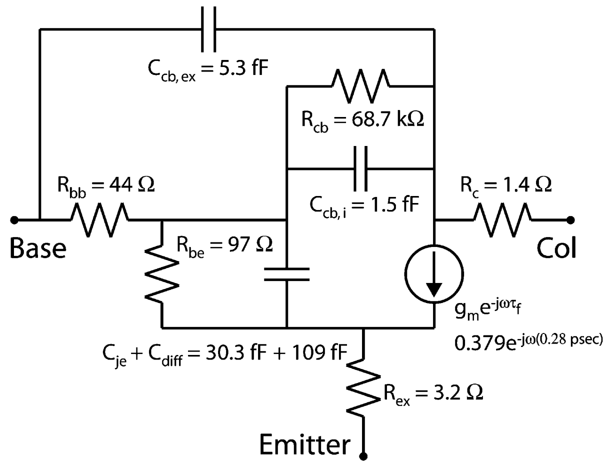


Fig. 4. Small-signal hybrid-$\pi$ equivalent circuit model.

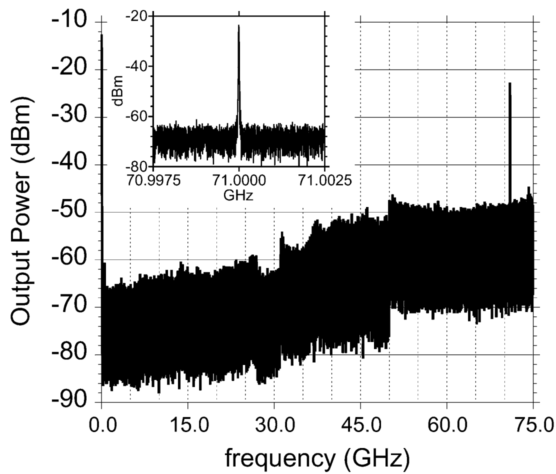


Fig. 5. Divider output spectrum at 71 GHz, $f_{\text{clk}} = 142$ GHz. The measurement includes 17 dB of attenuation; not corrected in the output spectrum.

it is fully static. For measurements at 142 GHz, the synthesizer signal is quadrupled using a Virginia Diode (VDI) doubler chain with the output amplified and delivered on-wafer with a WR-05 wafer probe. The output spectrum of the divide by two operating at 142 GHz is shown in Fig. 5, and the signal drive power at the probe tip is ≈12 dBm. Sensitivity measurements were performed and the self-oscillation frequency is $\approx 84$ GHz. Most HBTs in the circuit are biased closely to $J_{\text{Kirk}} \cong J_{\text{design}}$ for a minimum $C_{\text{cb}}/I_c$ ratio [3], however, because the devices at the data level (Fig. 1, Q1, Q2) are biased at $I_{\text{bias}} >> I_{\text{Kirk}}$ due to a lower fabricated sheet resistance than designed for the biasing resistors ($\rho_{\text{sheet, fab}} = 40\ \Omega$ versus $\rho_{\text{sheet, design}} = 50\ \Omega$), circuit performance suffers compared to [4] and [12].

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