ULTRA HIGH FREQUENCY STATIC DIVIDERS IN A NARROW MESA InGaAs/InP DHBT TECHNOLOGY

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Abstract

A static frequency divider with a maximum clock frequency > 111 GHz was designed and fabricated in a narrow mesa InP/$In_{0.53}Ga_{0.47}As$/InP DHBT technology. The divider operation is fully static, operating from f_{clk} = 4 GHz to 118.70 GHz and dissipating 686.4 mW of power from a -4.2 Volt supply. The circuit employs single-buffered emitter coupled logic (ECL) and inductive peaking. The transistors have an emitter junction width of 0.5 μm and a collector-to-emitter area ratio of 3.0. A microstrip wiring environment is employed for high interconnect density, and to minimize loss and impedance mismatch at frequencies > 100 GHz.

I. Introduction

InP based double heterojunction bipolar transistors (DHBT) have been aggressively pursued because of their superior material properties over SiGe [1]. This is demonstrated by the increased value of small signal unity current gain f_τ and unity power gain f_{max} that InP devices possess over SiGe at a given scaling generation [2,3]. The minimum gate delay of a digital IC in contrast is not determined by an algebraic function of f_τ and f_{max}, but instead by a set of time constants of which $C_{cb} \cdot \Delta V_{logic}/I_c$ is a major contributor. As Si based processing technologies are much more advanced than InP, SiGe devices have been scaled to dimensions where the reduction in base-collector capacitance C_{cb} and increased operating current density J_e are such that the speed of digital circuits in both material systems have been relatively the same. Over the past year, techniques to aggressively scale InP devices vertically and laterally have resulted in record performance for f_τ and f_{max} [3,4], as well as the design and fabrication of static frequency dividers—the digital performance benchmark for a given device technology. Prior to this work, the highest reported value for a static frequency divider in an InP technology was 100 GHz [5]. For a SiGe based technology the highest reported value for a static frequency divider is 96 GHz [6]. Here we report a static frequency divider in a divide by 2 and divide by 4 topology with a maximum operating clock frequency of 118.70 GHz and 115.72 GHz, respectively.

II. Technology

The transistors in the circuit are formed from an MBE layer structure with a highly doped 40 nm InGaAs base and 150 nm collector [3] and are fabricated in a triple-mesa process with both active junctions defined by selective wet and dry etch chemistry. The layer structure is given in table 1. Benzocyclobutene (BCB) passivates devices and planarizes the wafer after device formation. The ensuing level of metal deposition is used for circuit interconnects and making electrical contacts to the transistors and resistors. Thin-film dielectric microstrip wiring is employed for its predictable characteristics, controlled impedance, and ability to maintain signal integrity at very high frequencies within dense mixed-signal ICs. The associated ground plane also eliminates signal

Thickness (nm)	Material	Doping cm^{-3}	Description
40	InGaAs	8E19-5E19:C	Base
20	$In_{0.53}Ga_{0.47}$ As	2E16:Si	Setback
24	InGaAlAs	2E16 : Si	Base-Collector Grade
3	InP	3.0E18 : Si	Delta doping
100	InP	2E16 : Si	Collector
25	InP	1.5E19:Si	Sub Collector
5	$In_{0.53}Ga_{0.47}$ As	2E19 : Si	Sub Collector
300	InP	2E19 : Si	Sub Collector
Substrate	SI : InP		

Table 1: DHBT layer structure

coupling through on-wafer ground-return inductance. This is realized by placing 3 μm of BCB above the signal interconnects (M1) and using the top-most interconnect layer (M3) as a large ground plane (fig. 1).

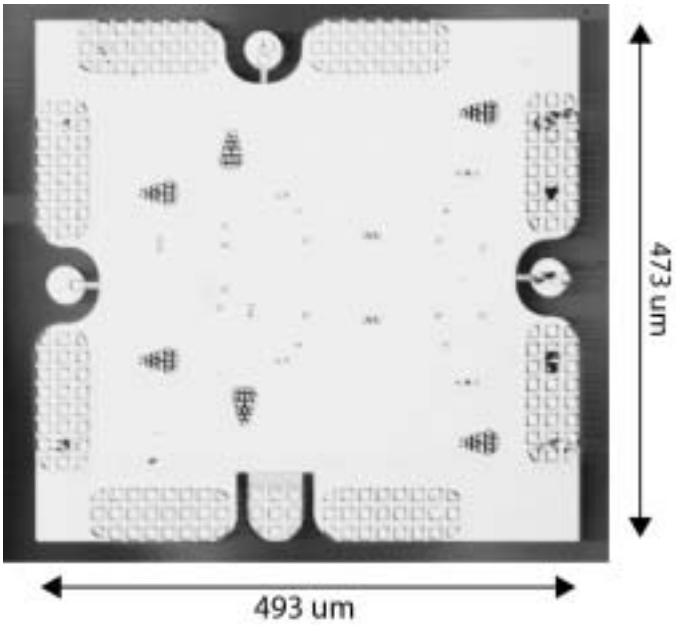

Fig 1: IC micrograph of the divide by 2

III. Circuit Design

The divide by 2 circuit is a master-slave latch with the output cross-coupled to the input to generate $f_{clk}/2$ frequency division of the clock source (fig. 2). The divide by 4 circuit is similar—two divide by 2 circuits are placed in series to generate $f_{clk}/4$ frequency division of the clock source. Unlike the dividers reported in [5,6], these circuits employ single-buffered emitter coupled logic (ECL) which consumes less power than E^2CL. Bias currents are established using pull-down resistors, not current mirrors, to reduce the number of active devices and reduce capacitive loading. The HBTs in the divider operate at $J_e \cong J_{Kirk}$ for their respective V_{cb} bias. As explained by [7], if the devices in the circuit can be operated at J_{Kirk} for a given collector thickness T_c, then the major contributor to the gate delay $C_{cb} \cdot \Delta V_{logic}/I_c$ is minimized and proportional T_c. To decrease the interconnect delays, the switching signal path is kept short—doubly-terminated with 50 Ω in a transmission-line bus with peaking inductance, located at the center of the IC. The output of each divider drives a differential-pair that serves as an output buffer to minimize loading to the divider signal bus. The divide by 2 area is 493 x 473 μm^2 and contains 28 transistors. The divide by 4 area is 575 x 813 μm^2 and contains 56 transistors.

IV. Circuit measurements and results

RF device measurements were performed on HBTs like those in the circuit. Data steering devices had a 235 GHz f_τ and 265 GHz f_{max}. Emitter followers at the data level had a 220 GHz f_τ and 150 GHz f_{max}. All clock level devices had a

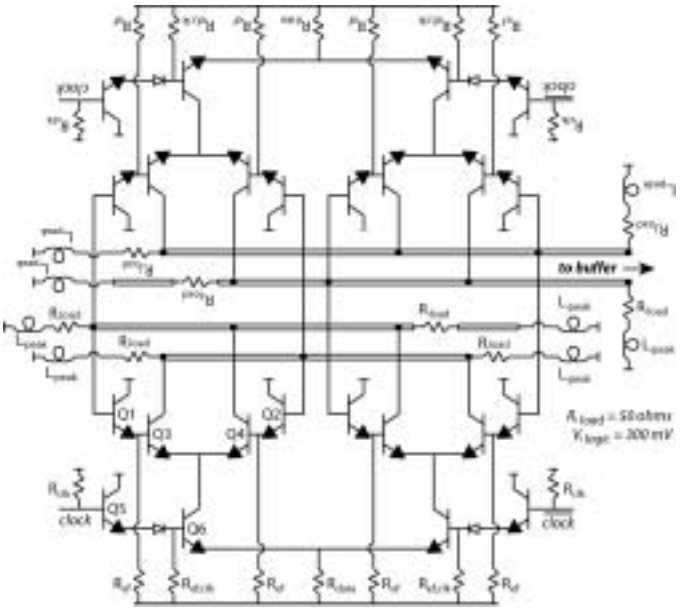

Fig 2: Schematic of static frequency divider

255 GHz f_τ and 260 GHz f_{max}. To minimize divider gate delay, the HBTs in the circuit are biased at or slightly higher than $J_{Kirk} \cong J_{design}$ for minimum C_{cb}/I_c ratio [7].

Divide by 2 and 4 measurements for clock frequencies ranging from 4 to 111.36 GHz were performed. At low frequencies, a DC-40 GHz frequency synthesizer directly drives the clock input. The dividers were clocked as low as 4 GHz to demonstrate that they are fully static (fig 3). An input clock driver is not used in this circuit—for this reason, a dependence on the output waveform from the slew-rate of the incoming clock signal is observed. For 50-75 GHz (V-band) measurements, the synthesizer drives a frequency tripler whose output is delivered on-wafer with a V-band waveguide-coupled wafer probe.

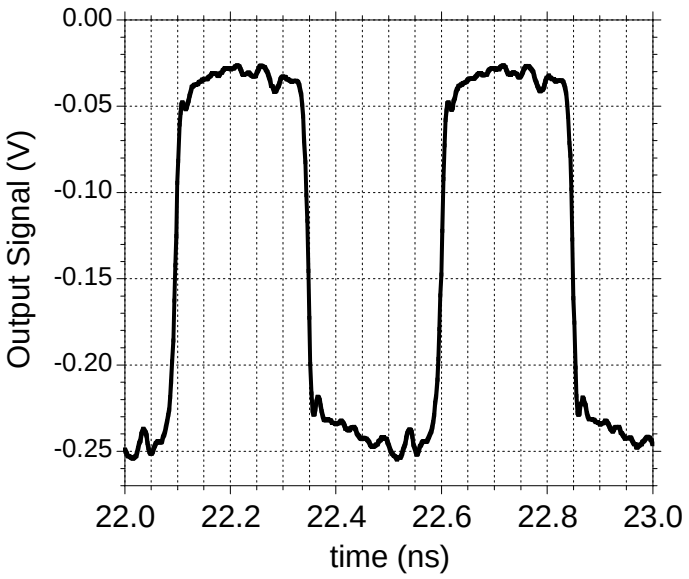

Fig 3: Output waveform @ 2 GHz, f_{clk} = 4 GHz

This measurement confirms the divider is fully static

For 75-110 GHz (W-band) measurements, the synthesizer drives a 20-40 GHz amplifier, whose output drives a frequency tripler for W-band frequencies. The clock signal is then amplified and delivered on-wafer with a waveguide-coupled W-band wafer probe. The output waveform at 55.68 GHz for a 111.36 GHz clock signal of a divide by 2 is shown in fig. 4, where the drive power at the probe tip was measured to be 9.8 dBm at this frequency. Measurements beyond 111.36 GHz with this W-band setup were not possible because of the sharp power roll-off at higher frequencies—at 112 and 113 GHz, P_{out} = 7.28 and 2.80 dBm respectively.

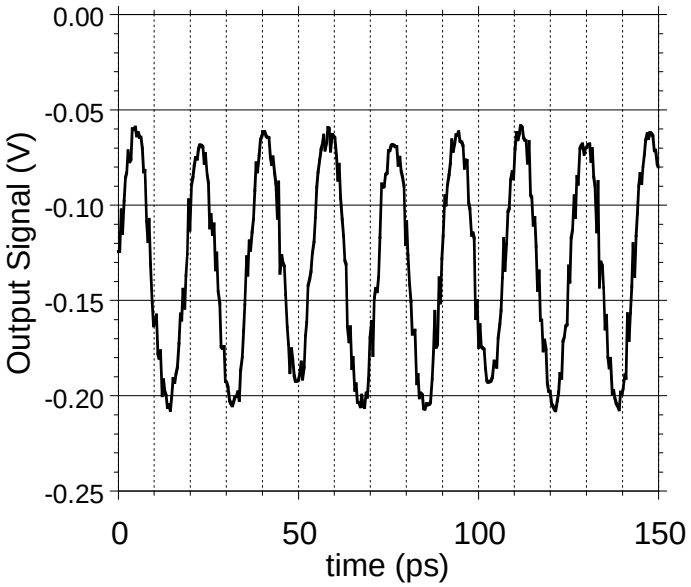

Fig 4: Output waveform @ 55.68 GHz, f_{clk} = 111.36 GHz
Amplitude modulation from setup at f_{clk} / 6 GHz on output waveform

For testing beyond 110 GHz, a backwards wave oscillator (BWO) was used. The output of the BWO directly feeds a variable attenuator and the signal is delivered on wafer with a waveguide-coupled wafer probe. The output spectrum at 59.35 GHz for a 118.70 GHz clock signal of a divide by 2 is shown in fig. 5, where the drive power at the probe tip was measured to xxx dBm at this frequency. The output spectrum at 57.8 GHz for a 115.6 GHz clock signal of a divide by 4 is shown in fig 6. At frequencies > 118.7 GHz, the divide by 2 stopped working properly. At frequencies > 115.6, the divide by 4 stopped working properly.

Sensitivity measurements were performed from 2 to 118.70 GHz on a divide by 2 circuit (fig. 7). The self-oscillation frequency of the divider is ≈ 75 GHz. The discontinuity between V-band and W-band testing is due to the minimum input power requirements of the frequency tripler for W-band testing.

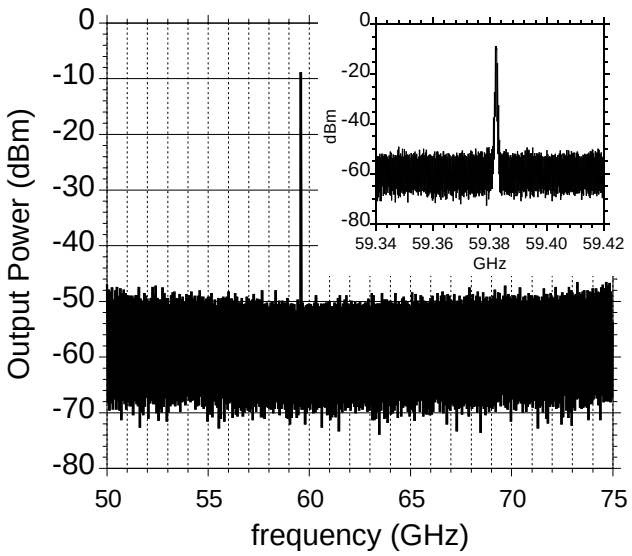

Fig 5: Output spectrum @ 59.35 GHz, f_{clk} = 118.70 GHz

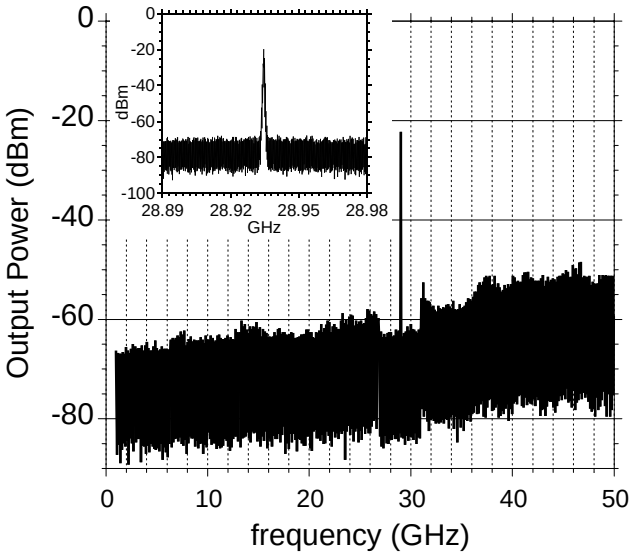

Fig 6: Output spectrum @ 57.8 GHz, f_{clk} = 115.6 GHz

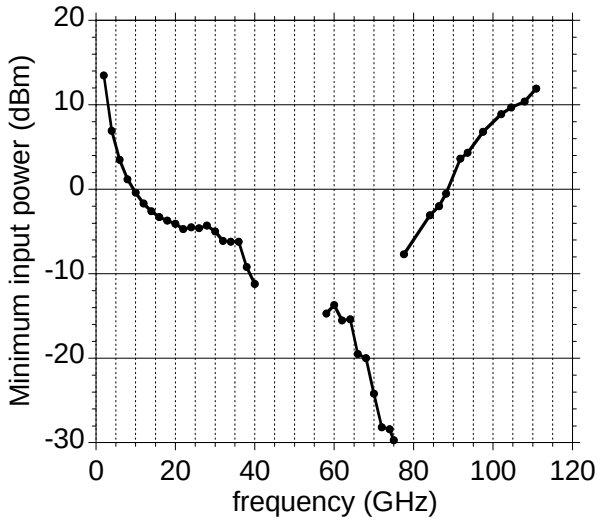

Fig 7: Variation of input sensitivity with frequency

V. Conclusion

Fully static divide by 2 and divide by 4 circuits have been designed and fabricated having a maximum clock frequency of > 115 GHz in a narrow mesa InP/$In_{0.53}Ga_{0.47}As$/InP DHBT technology. The circuit transistors operate at $J_e \cong J_{Kirk}$ for their respective V_{cb} bias to minimize gate delays associated with $C_{cb} \cdot \Delta V_{logic}/I_c$. The total power dissipation of the divide by 2 and output buffer is 686 mW. The total power dissipation of the divide by 4 and output buffer is 1.21 W.

Acknowledgement

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