Transistor and Circuit Design for 100–200-GHz ICs

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***Abstract*—Compared to SiGe, InP HBTs offer superior electron transport properties but inferior scaling and parasitic reduction. Figures of merit for mixed-signal ICs are developed and HBT scaling laws introduced. Device and circuit results are summarized, including a simultaneous 450 GHz f_τ and 490 GHz $f_{\max}$ DHBT, 172-GHz amplifiers with 8.3-dBm output power and 4.5-dB associated power gain, and 150-GHz static frequency dividers (a digital circuit figure-of-merit for a device technology). To compete with advanced 100-nm SiGe processes, InP HBTs must be similarly scaled and high process yields are imperative. Described are several process modules in development: these include an emitter-base dielectric sidewall spacer for increased yield, a collector pedestal implant for reduced extrinsic $C_{\rm cb}$, and emitter junction regrowth for reduced base and emitter resistances.**

***Index Terms*—InP heterojunction bipolar transistor, static frequency divider, millimeter-wave amplifier, dielectric sidewall-spacer, collector pedestal, emitter regrowth.**

I. Introduction

DESPITE formidable progress in CMOS, bipolar transistors remain competitive due to the larger breakdown voltages obtainable and the larger lithographic feature sizes required for a transistor at a given bandwidth. Compared to SiGe, InP heterojunction bipolar transistors (HBTs) have $\approx$ 3.5:1 higher collector electron velocity and $\approx$ 10:1 higher base electron diffusivity. Consequently, at the same scaling generation InP HBTs would have $\approx$ 3:1 greater bandwidth than SiGe HBTs. Today the maturity of advanced silicon processes has enabled SiGe HBTs to be fabricated with 100-nm emitter junctions with minimal extrinsic parasitics, while efforts to similarly scale InP HBTs have just begun. With that, SiGe HBTs have demonstrated simultaneous 300 GHz f_τ and 350 GHz $f_{\max}$ [1] and 102 GHz static frequency dividers [2], while InP DHBTs have obtained simultaneous 450 GHz f_τ and 490 GHz $f_{\max}$ [3], 176 GHz power amplifiers with 5-dB power gain [4], and $>$150 GHz static frequency dividers [5]–[8]. Consequently, the two technologies today have comparable bandwidth, with SiGe offering much higher levels of integration. Improved bandwidth and integration of InP HBTs therefore requires great consideration be given to scaling laws and limits, and the requirements placed upon transistor design for wide-band circuits must be clearly understood, where the ensuing fabrication processes must provide high yield at 100-nm scaling [9].

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II. HBT Performance Metrics

Although readily measured and widely reported in the device literature, transistor asymptotic unity current gain f_τ and unity power gain $f_{\max}$ cutoff frequencies are of limited value in predicting the speed of logic, mixed-signal, or optical transmission ICs, and transistors designed exclusively for high values of these parameters may perform poorly in circuits. For HBTs, an emitter-coupled logic (ECL) master–slave (M-S) latch is a representative small-scale mixed-signal circuit. Such latches serve as decision circuits in optical receivers, as latched comparators in ADCs, and as timing control elements in larger ICs. An M-S latch with inverting feedback (Fig. 1) forms a 2:1 static frequency divider, the maximum clock frequency $f_{\rm clk,max}$ of which serves as a convenient and popular speed benchmark of a mixed-signal IC technology. From charge control analysis, [10], [12], $T_{\rm gate} = 1/(2f_{\rm clk,max})$ is approximately a sum of RC delays $T_{\rm gate} = \Sigma a_{ij} R_i C_j$. Table I lists the delay coefficients a_{ij} and Table II the components of $T_{\rm gate}$ for an HBT design with target 260 GHz $f_{\rm clk,max}$ [10], [11]. $\Delta V_L = R_{\rm load} I_c$ is the logic voltage swing, $R_{\rm load}$ the load resistance, I_c the collector current, $R_{\rm ex}$ and R_{bb} the emitter and base parasitic series resistances, $C_{\rm je}$ the emitter depletion capacitance, $C_{{\rm cb}x}$ and $C_{{\rm cb}i}$ the components of the collector depletion capacitance $C_{\rm cb}$ external to and internal to R_{bb}, τ_f the sum of base τ_b and collector τ_c transit times, and τ_w the propagation delay on the signal wiring bus (Fig. 1).

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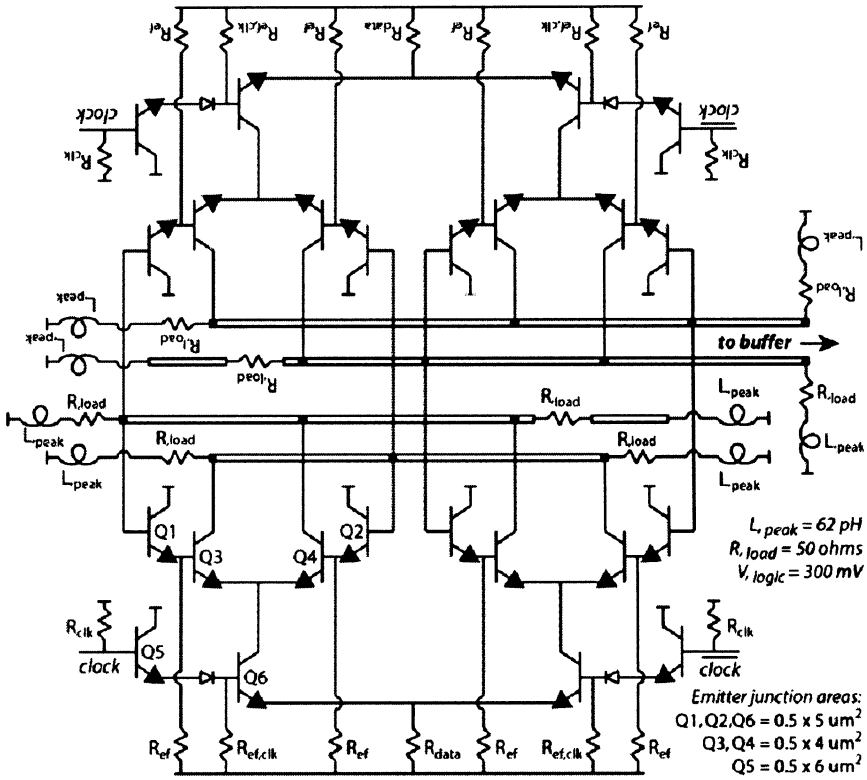


Fig. 1. Circuit schematic; 2:1 static frequency divider.

TABLE I
TOP—DELAY COEFFICIENTS a_{ij} FOR AN ECL M-S LATCH, WHERE $T_{\rm gate} = (2f_{\rm clk,max})^{-1} = \Sigma a_{ij} R_i C_j$. **BOTTOM**—PROPORTION OF $T_{\rm gate}$ DELAY FOR A 300-nm SCALING-GENERATION HBT, WITH TARGET 260 GHz CLOCK RATE

	C_{je}	C_{cbx}	C_{cbi}	$\tau_f I_c/\Delta V_L$	$\tau_w I_c$ / ΔV_L
$\Delta V_L/I_c$	1	6	6	1	1
kT/qI_c	0.5	1	1	0.5	0
R_{ex}	-0.3	0.5	0.5	0.5	0
R_{bb}	0.5	0	1	0.5	0

	C_{je}	C_{cbx}	C_{cbi}	$\tau_f I_c/\Delta V_L$	$\tau_w I_c/\Delta V_L$	sum
$\Delta V_L/I_c$	11%	16%	22%			49%
$\Delta V_L/I_c$				15%	18%	33%
kT/qI_c				1%		1%
R_{ex}	-1%			1%		0%
R_{bb}	5%		3%	7%		15%
sum	16%	16%	25%	24%	18%	100%
		42%				

TABLE II
TECHNOLOGY ROADMAPS FOR 40, 80, 160 Gb/s ICs, ASSUMING AN MS D-LATCH MAXIMUM CLOCK FREQUENCY 1.5:1 HIGHER THAN THE DATA RATE. MASTER-SLAVE LATCH DELAY INCLUDES 10% INTERCONNECT DELAY

Parameter	Gen. 1	Gen. 2	Gen. 3
MS D-latch speed	60 GHz	121 GHz	260 GHz
Emitter width (μm)	1.0	0.8	0.3
Parasitic resistivity ρ_{ex}, ($\Omega\cdot\mu$m^2)	50	20	5
Base thickness (nm)	40	40	30
Doping (cm^{-3})	$5\cdot10^{19}$	$7\cdot10^{19}$	$7\cdot10^{19}$
Sheet resistance (Ω/sq)	750	700	700
Contact resistance $\rho_{v,b}$ ($\Omega\cdot\mu$m^2)	150	20	20
Collector width (μm)	3	1.6	0.7
Collector thickness (nm)	300	200	100
Current density (mA/μm^2)	1	2.3	12
$A_{collector}$ / $A_{emitter}$	4.55	2.6	2.9
f_τ (GHz)	170	248	570
f_{max} (GHz)	170	411	680
I_c / L_e (mA/μm)	1	1.9	3.7
τ_f (ps)	0.67	0.50	0.22
C_{cb} / I_c (ps/V)	1.7	0.62	0.26
$C_{cb}\cdot\Delta V_l$ / I_c (ps)	0.5	0.19	0.09
R_{bb} / (ΔV_l / I_c)	0.8	0.68	0.99
$C_{je}\cdot\Delta V_l$ / I_c (ps)	1.7	0.72	0.15
R_{ex} / (ΔV_l / I_c)	0.1	0.15	0.17

The base and collector transit times play a relatively minor role in logic speed, with only 24% of $T_{\rm gate}$ arising from τ_f for the HBT of Table II. This is in contrast to the much stronger relative contribution of transit times to f_τ, with τ_f typically contributing 80% of $\tau_{ec} = 1/2\pi f_\tau$. Depletion capacitance charging times $C\Delta V_L/I_c$ dominate over transit delays in digital circuits because $\Delta V_L \gg kT/q$, as is required for digital noise margin. Examining the total delay $\Sigma a_{ij} R_i C_j$ in terms of resistances, 49% of $T_{\rm gate}$ is associated with the load resistance $\Delta V_L/I_c$. High current density is thus essential. For adequate logic noise margin, ΔV_L must be at least $\sim 4(kT/q + R_{\rm ex} I_e)$, hence increased current density must be accompanied by

reduced emitter resistance, so as to maintain a small ΔV_L. Although not evident in Table I, $R_{\rm ex}$ thus has a large indirect effect on $f_{\rm clk,max}$, as increased $R_{\rm ex}$ forces increased ΔV_L. Examined in terms of capacitances, 58% of $T_{\rm gate}$ arises from the depletion capacitances $C_{\rm cb}+C_{\rm je}$, even given the assumed HBT design having small C/I ratios. For logic and mixed-signal ICs, low $C_{\rm cb}\cdot\Delta V_L/I_c$ charging time is critical, necessitating very high current density, minimal excess collector junction area, and very low emitter access resistance.

For reactively-tuned amplifiers [13] in radio transceivers, $f_{\rm max}$ defines the highest frequency at which power gain can be obtained, and is therefore directly relevant. f_τ has significant but secondary importance; when tuned for maximum power gain, a transistor with a high $f_{\rm max}/f_\tau$ ratio requires a high ratio of load resistance to transistor input resistance. The required high impedance tuning ratio aggravates matching-network resistive losses—already considerable in >100 GHz ICs—and thereby reduces gain. In receivers, amplifiers are tuned not for maximum gain but for minimum noise figure, while in transmitters, amplifiers are tuned for maximum efficiency and for maximum saturated power output. Gain expressions under such constraints are complex.

At a given scaling generation, the HBT base and collector layers can be thinned for highest feasible f_τ while sacrificing both $f_{\rm max}$ and logic speed, but such transistors are of limited value in circuits. Of greater value are balanced and proportional reductions of all transistor parasitics, such that all circuits employing the transistor exhibit a proportional increase in bandwidth.

III. Scaling: Laws, Limitations, and Roadmaps

Approximate HBT scaling laws derived in [11] are here summarized. For a $\gamma:1$ bandwidth increase in an arbitrary circuit using the transistor, all transistor capacitances and transit delays must be reduced $\gamma:1$ while maintaining constant all parasitic resistances, all bias and signal voltages, the transconductance g_m, and the operating current I_c. Reducing the collector depletion layer thickness T_c by $\gamma:1$ and base thickness T_b by $\gamma^{1/2}:1$ reduces τ_f by the required proportion but would *increase* $C_{\rm cb}$ if junction areas were held constant. Reducing the emitter and collector junction areas in proportion to $\gamma^2:1$ then results in the desired $\gamma:1$ reduction in $C_{\rm cb}$. Because the total base resistance is only weakly dependent upon the emitter junction width (contact and link resistance dominate over spreading resistance) but varies as the inverse of the emitter junction stripe length, reducing the emitter and collector junction widths in proportion to $\gamma^2:1$ will maintain constant R_{bb} while effecting the needed $\gamma^2:1$ reduction in emitter junction area. With constant I_c, but with the emitter junction area reduced in proportion to $\gamma^2:1$, the emitter current density increases: $J_e\propto\gamma^2$. This is feasible within the limits imposed by the Kirk effect, as $J_{\rm Kirk}\propto 1/T_c^2\propto\gamma^2$. Because the emitter parasitic resistance $R_{\rm ex}$ must remain constant in the presence of a $\gamma^2:1$ reduction in emitter junction area A_e, the normalized emitter contact resistivity $\rho_{\rm ex}=R_{\rm ex}A_e$ must be reduced rapidly, with $\rho_{\rm ex}\propto 1/\gamma^2$. Because operating J_e increases in proportion to the bandwidth squared, the maximum reliable power density $P/A_e=J_eV_{\rm ce}\propto\gamma^2V_{\rm ce}$ is a more significant applied voltage limit than the low-current breakdown voltages $\rm BV_{CEO}$ or $\rm BV_{CBO}$.

TABLE III
Summary of Simultaneous Parameter Scaling for a $\gamma:1$ Increase in HBT and Circuit Bandwidth

key device parameter	required change
collector depletion layer thickness	decrease γ:1
base thickness	decrease $\sqrt{\gamma}$:1
emitter junction width	decrease γ^2:1
collector junction width	decrease γ^2:1
emitter contact resistivity, ρ_{ex}	decrease γ^2:1
current density	increase γ^2:1
base contact resistivity – if contacts lie above B-C junction	decrease $\sim\gamma^2$:1
base contact resistivity – if contacts do not lie above B-C junction	unchanged

Scaling requirements for the base contact resistivity and for the emitter depletion thickness are not easily summarized here [11]. The emitter depletion layer thickness need not be scaled as rapidly as that of the collector, hence $C_{\rm je}$ becomes progressively less significant with scaling. If the base Ohmic contacts lie above the collector-base junction, then their width must reduced $\gamma:1$ to obtain the requisite reduction in $C_{\rm cb}$; this necessitates a $\sim\gamma^2:1$ reduction in the base contact resistivity $\rho_{v,b}$. It the contacts do not lie above the junction, their resistivity can remain unchanged. These scaling laws are summarized in Table III.

Consider specifically the impact of this scaling on ECL logic speed. With a $\gamma:1$ scaling, the collector thickness T_c is reduced $\gamma:1$, the current density increased $\gamma^2:1$, and the dominant delay $C_{\rm cb}\cdot\Delta V_L/I_c$ reduced $\gamma:1$. The parasitic voltage drop $R_{\rm ex}I_c=\rho_{\rm ex}J_e$ remains constant only because $\rho_{\rm ex}$ is reduced rapidly, being proportional to $1/\gamma^2$

Base $\rho_{v,b}$ and emitter $\rho_{\rm ex}$ contact resistivity, thermal resistance $\theta_{\rm JA}$, and fabrication yield of submicron features are the key barriers to further scaling [11], [14]. Current density must increase, and emitter and base contact resistivities must decrease in proportion to the *square* of circuit bandwidth. Thermal resistance normalized to the emitter junction area $\theta_{\rm JA}A_e$, must also be reduced in proportion to the square of circuit bandwidth. Table II shows a prospective HBT scaling roadmap for increased digital logic speed; note in particular that at ~260 GHz target clock rate, the emitter contact resistivity must be $\sim5\ \Omega\cdot\mu{\rm m}^2$, the current density 12 mA/$\mu{\rm m}^2$, and the normalized thermal resistance $\sim5\ {\rm K}\cdot\mu{\rm m}^2$/mW.

Consider a future HBT having 1 THz f_τ and $f_{\rm max}$. Its emitter width would be ~75 nm, feasible with present lithographic tools. But, to be properly scaled so as to enable, e.g., ~500 GHz digital clock rates $\sim1\ {\rm K}\cdot\mu{\rm m}^2$/mW thermal resistance and $\sim1\ \Omega\cdot\mu{\rm m}^2$ emitter contact resistivity would be required. It is not yet clear how to obtain such parameters.

IV. Transistor and IC Results for Mesa HBTs

At a given scaling generation, defined by the minimum emitter feature size, different transistor layer structures are

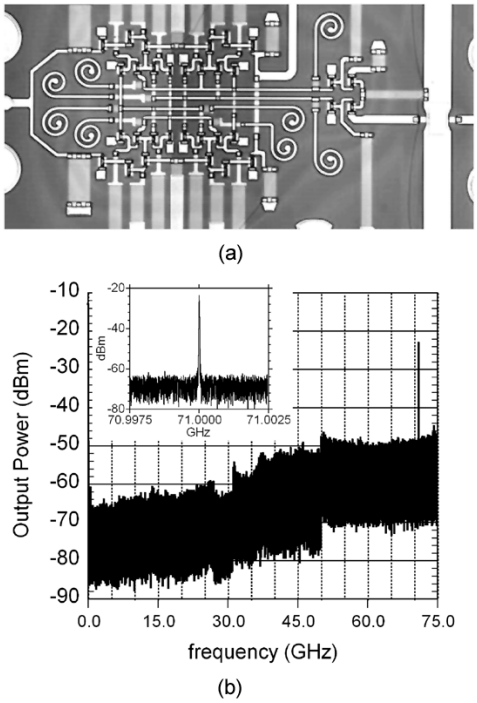


Fig. 2. Fabricated and measured results of UCSB static frequency divider. (a) Circuit photograph of static divider signal bus, (b) Output spectum of divide-by-2 circuit at 71 GHz, $f_{\rm clock} = 142$ GHz.

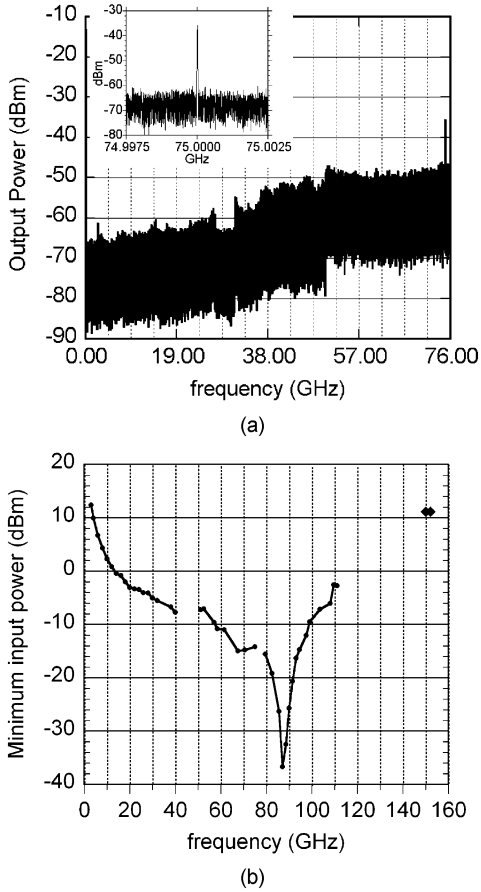


Fig. 3. Measured results of 150 GHz static frequency divider—UCSB design, GCS fabrication. (a) Output spectum of divide-by-2 circuit at 75 GHz, $f_{\rm clock} = 150$ GHz, (b) Input signal sensitivity plot.

preferred so as to obtain a differing balance of device parasitics that are more suited for the particular application—i.e., mm-wave tuned amplifiers benefit from high $f_{\max}$ and can tolerate moderately lower f_τ, whereas digital IC speed benefits from devices having simultaneously high values of f_τ and $f_{\max}$, and demands low $C_{\rm cb} \cdot \Delta V_L / I_c$ and low $R_{\rm ex} \cdot I_c / \Delta V_L$. Amongst different HBT designs, numerous device and circuit results have recently been reported.

Two device designs intended for use in high-speed logic have been investigated at the University of California at Santa Barbara (UCSB) with 150-nm and 120-nm drift-collector thickness T_c. The HBT having 150-nm T_c obtained a simultaneous 391 GHz f_τ, 505 GHz $f_{\max}$, and $C_{\rm cb}/I_c = 0.51$ ps/V when biased at $J_e = 5.17$ mA/μm^2 and $V_{\rm cb} = 0.6$ V. The common-emitter breakdown voltage $\rm BV_{CEO}$ was 5.1 V [15]. From this device design, ECL static frequency dividers were designed and fabricated at UCSB and at GCS (Fig. 1). Divide-by-2 circuits fabricated at UCSB produced an $f_{\rm clk,max} = 142$ GHz (Fig. 2), [15], and utilizing the same collector structure an $f_{\rm clk} \geq 150$ GHz static divider (Fig. 3) was demonstrated from GCS [5]. For the 150 GHz divider, the key device parameters of the HBTs within the circuit at their respective bias conditions are given in Table IV.

From the 120-nm T_c design, 450 GHz f_τ, 490 GHz $f_{\max}$, and $C_{\rm cb}/I_c = 0.36$ ps/V were obtained at a bias of $J_e = 8.7$ mA/μm^2 and $V_{\rm cb} = 0.6$ V. $\rm BV_{CEO}$ was 3.9 V [3]. The DC common-emitter IV characteristics and measured microwave gains are shown in Fig. 4.

Devices with a collector $T_c = 100$ nm were explored to investigate the effectiveness of the InGaAs/InAlAs chirped-superlattice base-collector grade [16] at higher current densities. 491 GHz f_τ, 415 GHz $f_{\max}$, and $C_{\rm cb}/I_c = 0.57$ ps/V was measured at $J_e = 10.3$ mA/μm^2 and $V_{\rm cb} = 0.4$ V, while $\rm BV_{CEO} = 3.1$ V [17]. $J_{\rm Kirk} \approx 15$ mA/μm^2, at $V_{\rm ce} = 1.0$ V. Thermal failure is at 25–30 mW/μm^2, hence the devices can be biased at $V_{\rm ce} = 2$ V while carrying 13 mA/μm^2. The devices thus far discussed have a 0.6×4.3 μm^2 emitter junction area $A_{\rm je}$, a collector to emitter width ratio $= 2.2$, and employ an evaporated self-aligned base contact. The reduced $f_{\max}/f_\tau$ ratio of the HBTs with $T_c = 100$ nm reflects insufficient lateral scaling of the emitter and collector junctions.

Devices intended for power amplifiers employing a 210-nm collector T_c obtained a simultaneous 276 GHz f_τ, 451 GHz

TABLE IV
KEY DEVICE PARAMETERS (FIG. 1) OF THE 150-GHz STATIC DIVIDER

	units	Q1, Q2	Q3, Q4	Q5	Q6
A_e	μm^2	0.5 × 5	0.5 × 4	0.5 × 6	0.5 × 5
J_e	mA/μm^2	4.0	6.0	3.3	4.8
C_{cb}/I_c	ps/V	0.99	0.59	0.86	0.59
V_{cb}	V	0.0	0.6	1.7	0.6
f_τ	GHz	260	301	280	301
f_{max}	GHz	268	358	280	358

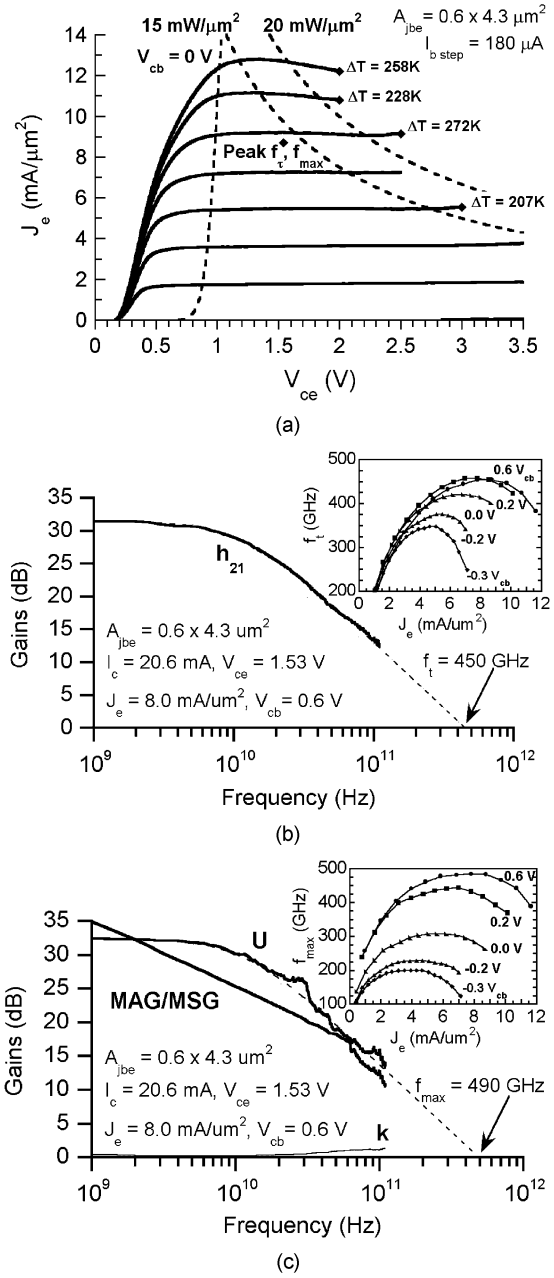


Fig. 4. DC and RF performance of a narrow-mesa InP-DHBT—120-nm collector, 30-nm base. (a) Common-emitter I-V characteristics at high power density, (b) Measured microwave gains at peak f_τ, DC-110 GHz, (c) Measured microwave gains at peak $f_{\max}$, DC-110 GHz.

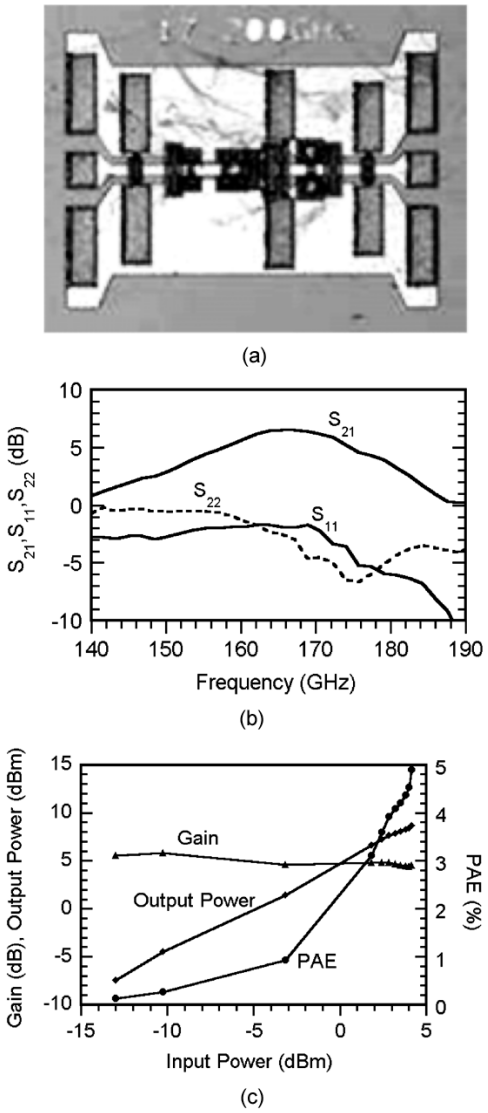


Fig. 5. Fabricated and measured results of InP-DHBT power amplifiers. (a) Circuit photograph of 172-GHz one-stage MMIC amplifier. (b) Small-signal S-parameters, 140–220 GHz. (c) Amplifier power gain at 172 GHz.

$f_{\max}$, and $C_{\rm cb}/I_c = 0.65$ ps/V, with $\mathrm{BV_{CEO}} = 6.9$ V. An ensemble of different medium power amplifiers were fabricated from this collector structure and have been reported [4]—among them include a 176-GHz common-base amplifier with 8.3-dBm output power and 4.5-dB associated power gain, shown in Fig. 5. The common-base configuration is employed because it has higher maximum stable gain (MSG) than common-emitter. This MSG is further increased by minimizing the base feed inductance and collector-emitter overlap capacitance $C_{\rm ce}$. Stage gain was limited on this amplifier due to $f_{\max}$ decreasing ($\approx$ 300 GHz) to below design values (450 GHz) on the wafer carrying amplifiers.

V. Advanced InP HBT Process Modules

A. Dielectric Sidewall Spacers—LSI Level Device Yield

The mesa HBTs described above suffer limited yield from the self-aligned emitter-base etch/liftoff process. Further, doubling circuit speed requires emitter $\rho_c \approx 5\,\Omega{\cdot}\mu\mathrm{m}^2$ and narrow 200-nm base contacts. Dielectric sidewall spacer processes eliminate the need for evaporated self-aligned base contacts [18], and by doing so, emitter-base short-circuits associated with liftoff are avoided. Furthermore, the sidewall spacer allows for very thin emitter semiconductor layers, minimizing undercut during mesa formation. Fig. 6 shows an early prototype HBT with an emitter dielectric sidewall. More advanced processes at Rockwell Scientific have produced high HBT yield at 0.25-μm emitter width, demonstrating devices with 326 GHz f_τ, 305 GHz $f_{\max}$, and $C_{\rm cb}/I_c < 0.55$ ps/V [19].

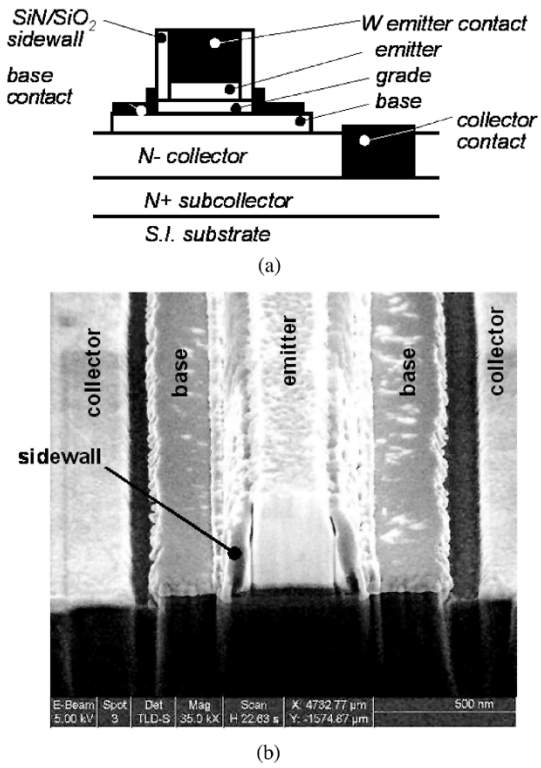


Fig. 6. Dielectric sidewall spacer process. (a) Sidewall process schematic. (b) SEM cross section of a fabricated device.

B. Collector Pedestal Implant—Reduced $C_{\rm cb}$

At the 0.25-μm emitter (width) scaling generation, a significant challenge is maintaining an acceptably small collector to emitter junction area ratio $A_{jc}/A_{\rm je}$. While the base contact transfer length L_T is 200 nm for a base contact $\rho_{v,b} = 20\,\Omega{\cdot}\mu{\rm m}^2$ to an $R_{\rm sheet} = 500\,\Omega$, 200-nm-wide base contacts present challenges in process design for high yield fabrication, and in addition present significant bulk metal resistance along the length of the base contact. Closely following the SiGe device structure [20], an implanted N^+ collector pedestal reduces the capacitance underneath where the base contact lies [Fig. 7(a)], permitting somewhat higher base contact resistivities and wider base contacts at a given level of device performance. The pedestal also substantially reduces the $C_{\rm cb}$ associated with the large base-pad interconnect used in some device technologies. Pedestals can be used with mesa, dielectric-sidewall, or regrown emitter-base junction HBTs.

Initial pedestal HBT results from UCSB [21] have demonstrated high quality regrowth of the active device layers with expected common-emitter *I–V* characteristics shown in Fig. 7(b). Gummel characteristics of these devices show low leakage currents ($I_{cbo} = 320$ pA at $V_{\rm cb} = 0.3$ V) with collector and base ideality factors of $n_c = 1.14$ and $n_b = 1.25$, respectively. RF device performance suffered from high emitter resistance ($\rho_c \approx 90\ \Omega \cdot \mu{\rm m}^2$) due to errors made in device fabrication and only 170 GHz f_τ and 150 GHz $f_{\rm max}$ were measured. With pedestal implants, there has been observed both significantly reduced $C_{\rm cb}$ [Fig. 7(c)] together with moderately increased device

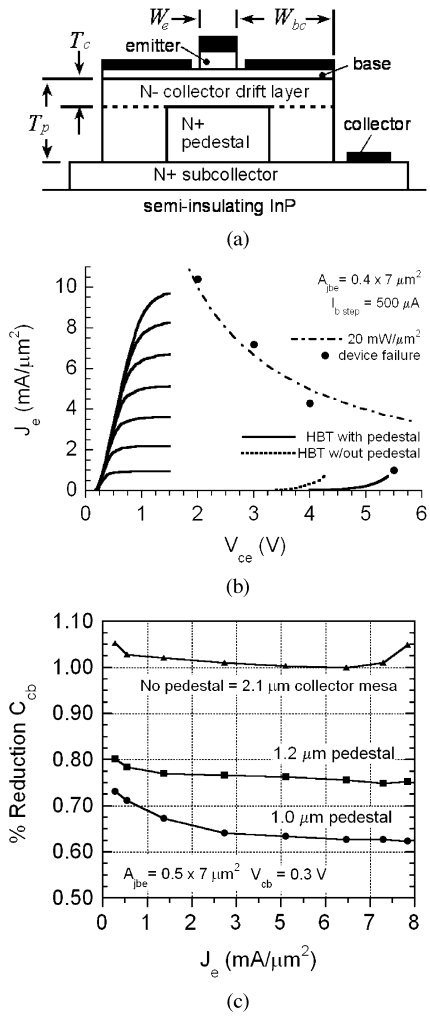
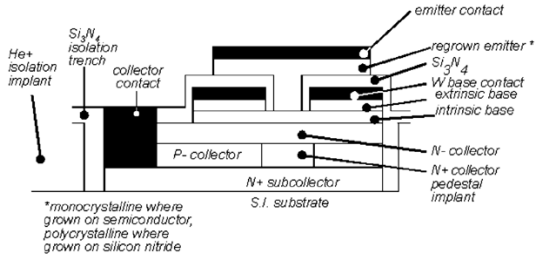


Fig. 7. Topology and electrical performance for a UCSB pedestal InP HBT. (a) Pedestal process schematic. (b) Common-emitter I-V characteristics for the pedestal HBT. (c) Amount of $C_{\rm cb}$ reduction for varying pedestal width.

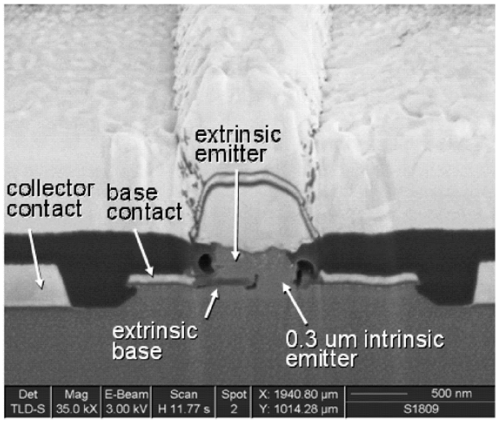
breakdown voltage—where on the same wafer ${\rm BV_{CEO}} = 4.0$ V and 3.3 V (at $I_c = 50$ μA) for a 100-nm drift-collector T_c with and without the pedestal, a 20% increase. The high-field region of the drift-collector for the pedestal device is now buried within the collector mesa (above the pedestal implant), such that surface breakdown effects associated with the $\approx 10^{12}$ cm^{-2} (N-type) surface state charge density typical of ill-passivated InP surfaces have a reduced effect. Increased breakdown in collector pedestal InP DHBTs has also been observed and reported in [22].

C. Emitter Junction Regrowth

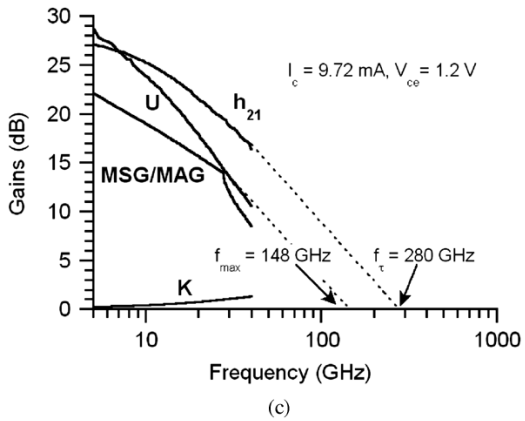
Dielectric sidewall and collector pedestal processes address neither base nor emitter contact resistivity scaling limits. Again, closely following the SiGe device structure, there has been developed an HBT process flow [Fig. 8(a)] in which a low-resistivity polycrystalline InAs regrowth forms a T-shaped emitter whose ohmic contact is much larger than the emitter junction for reduced $R_{\rm ex}$. Such reductions of emitter resistance through an increased contact/junction area ratio is an alternative to materials engineering for reduced emitter access resistance.



(a)



(b)



(c)

Fig. 8. Regrown-emitter InP-HBT topology and results from UCSB. (a) Schematic of regrown-emitter III–V HBT. (b) SEM cross section of regrown HBT. (c) Measured microwave gains at peak f_τ and $f_{\max}$.

Recall that an emitter $\rho_c \approx 5\ \Omega\cdot\mu\text{m}^2$ is targeted for 260-GHz clock rate, a resistivity $\approx 1.6:1$ better than the best reported results thus far obtained [17]. The emitter regrowth process also permits an extrinsic base region of $N_A > 10^{20}$ cm^{-3} doping and a total extrinsic and intrinsic thickness of 100 nm for reduced base resistance R_{bb}. Self-aligned refractory base ohmic contacts lie under the extrinsic emitter regions.

Regrown-emitter devices from UCSB have demonstrated 280 GHz f_τ and 148 GHz $f_{\max}$ in such processes [23], shown in Fig. 8(b). Presently, device performance is limited by both difficulties in emitter regrowth over the edges of the emitter etch window [Fig. 8(c)] and by partial passivation of the base doping by hydrogen associated with the PECVD Si_3N_4 deposition process. The fabrication process is now being substantially revised, where a fully epitaxial regrown-emitter InP HBT process is now being pursued with initial results reported in [24].

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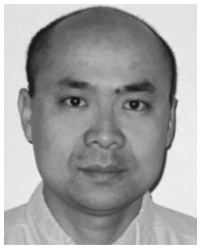

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