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Low Turn-On Voltage InP/$In_{0.7}Ga_{0.3}As$/InP Double Heterojunction Bipolar Transistors

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While InP based double heterojunction bipolar transistors (DHBT) is are key devices in high-speed electronics[1], there is continuing demand for higher frequency electronics operating at lower power, particularly in military and aerospace applications. Low power is obtained by both reducing the device operating current $I_c = J_e A_e$ through reduced emitter area A_e and through reducing the supply voltage V_{ce}, the latter in bipolar logic circuits being proportional to the base-emitter turn-on voltage V_{be}. While low V_{be} can be obtained using the InAs/AlSb material system, PNP transistors face challenges with collector transit time and collector charging rate I_C/C_{cb} due to the low hole velocity. NPN HBTs with InAs base layers have been reported[2], but the low bandgap of the InAs collector remains a challenge. In this work, low V_{be} HBTs were developed in the InP based material system, taking advantage of both its maturity and the high bandgap and breakdown field of an InP collector.

A low V_{be} is obtained using a strained $In_xGa_{1-x}As$ base with a high indium composition x. Matthews-Blakeslee theory predicts an 89 Å maximum thickness for a $In_{0.7}Ga_{0.3}As$ strained base layer on InP. Unfortunately, at least 300A of low band gap material is required for the base, the collector setback layer, and the strained portions of the heterojunction grades. Thus, nucleation of dislocations is inevitable and is a major concern. The DHBT structure (Figure 1) was grown on semi-insulating InP. A 250 Å $In_{0.7}Ga_{0.3}As$ base layer was grown for low turn-on voltage and a 75 Å $In_{0.7}Ga_{0.3}As$ setback layer was introduced between the base and the base-collector grade. Other layers were lattice matched to InP. The sub-collector and collector layers were grown at 470 °C, as is optimum for InP and $In_{0.53}Ga_{0.47}As$. To reduce nucleation of dislocations, the temperature was reduced to 350 °C during base and emitter layer growth. The surface showed a light cross-hatch pattern indicating some strain relaxation.

Figure 2 shows common-emitter characteristics of a large area device having a 100 μm x130 μm base-collector junction and a 60 μm x 60 μm emitter-base junction. The current gain is 148 and breakdown voltage is 4 V. Figure 3 shows a Gummel plot from a large area device. With 0.3V base-collector offset voltage, the leakage current I_{cbo} is 0.3 μA at V_{cb}=0.3 V. Though this leakage is higher than the 4.3 nA I_{cbo} for similar lattice matched DHBTs in our laboratory, the 23 pA/μm^2 I_{cbo} per unit junction area is sufficiently small that I_{cbo} of typical μm-scale transistors will be dominated by surface leakage. The turn-on voltage reduction was measured by comparing Gummel curves of $In_{0.7}Ga_{0.3}As$-base and $In_{0.53}Ga_{0.47}As$-base transistors with 0.4 um x 7.5 um emitter-base junction area and 1.2 μm x 11 μm base-collector junction area (fig. 4). A 0.13V reduction in V_{be} is observed, consistent with the 0.15V calculated from theory. These small-area devices showed μA-level I_{cbo} due to a processing error, and the common-emitter DC characteristics were consequently poor.

In conclusion, InP/$In_{0.7}Ga_{0.3}As$/InP DHBT were grown on InP. The expected V_{be} reduction was clearly observed. Though a surface cross-hatch pattern was observed, the common-emitter characteristics and leakage currents of large-area test devices are acceptable for circuit applications.

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[1] Y. Wei, S. Lee, K. Sundararajan, M. Dahlstrom, M. Urteaga, M. Rodwell. "High current (100 mA) InP/InGaAs/InP DHBTs with 330 GHz fmax," 14th Indium Phosphide and Related Materials Conference, p.47-50. Piscataway, NJ (2002)

[2] S.Thomas III, K.Elliott, D.H.Chow, A.Arthur, B.Shi, P.Brewer, R.Martinez, "Fabrication of InAs-Based Heterojunction Bipolar Transistors", 2002 IEEE Device Research Conference, Santa Barbara, California, June 24-26, 2002

Layer	Material	Doping (cm^{-3})	Thickness (Å)
Emitter Cap	$In_{0.53}Ga_{0.47}As$	2×10^{19} : Si	300
Grade	$In_{0.53}Ga_{0.47}As$ /$In_{0.52}Al_{0.48}As$	2×10^{19} : Si	200
N^+ Emitter	InP	1×10^{19}: Si	700
N^- Emitter	InP	8×10^{17} : Si	500
Delta Doping	InP	3×10^{18} : Si	30
Grade	$In_{0.53}Ga_{0.47}As$ /$In_{0.52}Al_{0.48}As$	4×10^{17} : Si	275
Base	$In_{0.7}Ga_{0.3}As$	3×10^{19} :Be	250
Set back	$In_{0.7}Ga_{0.3}As$	2×10^{16} : Si	75
Grade	$In_{0.53}Ga_{0.47}As$ /$In_{0.52}Al_{0.48}As$	2×10^{16} : Si	340
Delta Doping	InP	2.5×10^{18} :Si	30
Collector	InP	2×10^{16} : Si	1555
Sub collector	$In_{0.53}Ga_{0.47}As$	1×10^{19} : Si	250
Sub collector	InP	1×10^{19} : Si	1250
InP (100) semi-insulating substrate			

Figure 1 : Sample structure of InP/$In_{0.7}Ga_{0.3}As$/InP HBT

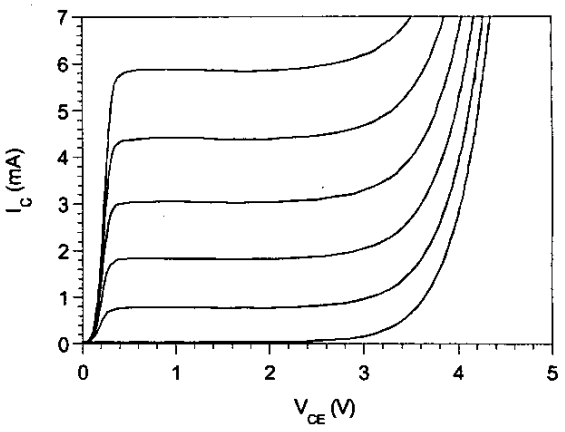

Figure 2 : Common emitter characteristics of a InP/$In_{0.7}Ga_{0.3}As$/InP HBT with a 60 × 60 μm emitter. The base current steps are 10 μA .

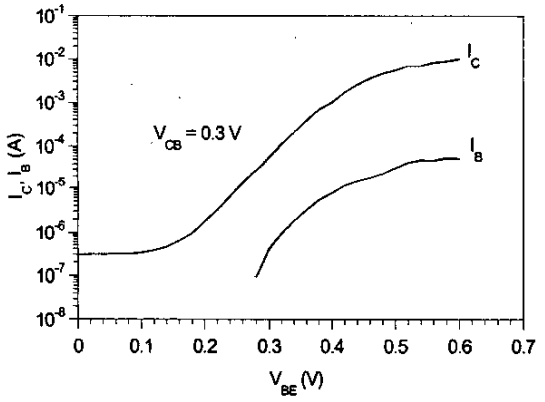

Figure. 3 : Gummel characteristics of an InP/$In_{0.7}Ga_{0.3}As$/InP HBT with a 60 μm × 60 μm emitter-base junction and a 100 μm × 130 μm base-collector junction.

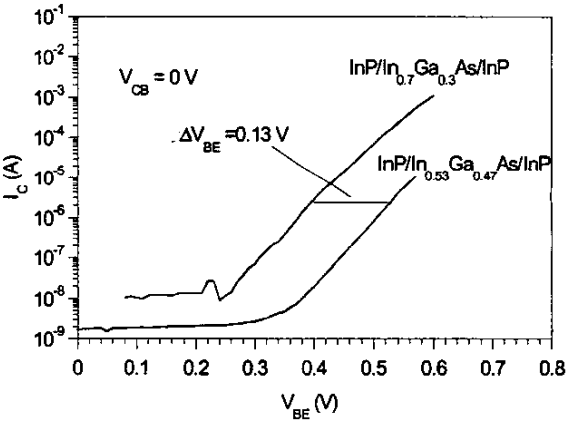

Figure. 4 : Collector currents comparison in Gummel characteristics for trasistors with a 0.4 μm × 7.5 μm emitter-base junction. The InP/$In_{0.7}Ga_{0.3}As$/InP HBT shows 0.13 V lower V_{be} than the InP/$In_{0.53}Ga_{0.47}As$/InP HBT