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InAs/InAsP composite channels for antimonide-based field-effect transistors

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We report the growth and transport characteristics of stepped InAs/$InAs_{1-x}P_x$ quantum wells with AlSb barriers. Electron mobilities and carrier concentrations in these composite stepped quantum wells were studied as a function of growth temperature and phosphorus content. For $InAs_{1-x}P_x$ grown at 430 °C substrate temperature (nominal $x=0.2$), a high 22 500 $cm^2/V\,s$ electron mobility was observed, while 7100 $cm^2/V\,s$ mobility was observed in a single strained $InAs_{1-x}P_x$ quantum well layer. Heterostructure field-effect transistors fabricated using the composite quantum wells exhibited increased breakdown voltage and a 14:1 reduction in source-drain dc conduction when compared to a similar InAs-channel device. © *2004 American Institute of Physics.*
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The InAs/AlSb quantum well system is attractive for the realization of high-speed low-power heterostructure field-effect transistors (HFETs) because of high electron mobility (as high as 30 000 $cm^2/V\,s$ at 300 K) and high feasible sheet electron density.[1] Unfortunately, the small band gap of the InAs channel causes electron impact ionization even at low drain voltages, producing low breakdown voltage, threshold shifts due to hole accumulation (kink effect), and high output conductance.[2,3] Proposed approaches to improve breakdown in InAs HFETs include the use of a back gate,[3] increased quantum confinement,[4] and an additional InAs subchannel.[5] In InGaAs/InAlAs HFETs grown on InP substrates, breakdown voltage can be greatly improved by using an InGaAs/InP composite channel, wherein low-field electron transport under the HFET gate occurs in the high-mobility InGaAs layer, and high-field transport between gate and drain in the wide-band-gap InP layer.[6,7] In a similar approach, we here demonstrate InAs/$InAs_{1-x}P_x$ composite channels grown on AlSb. The objective is to increase the breakdown voltage of InAs-based HFETs through the increased band gap of an inserted $InAs_{1-x}P_x$ subchannel. $InAs_{1-x}P_x$ has a direct band gap, and a large separation (>0.6 eV) between Γ and L conduction band minima for all ratios x.[8–10] We therefore expect high peak electron velocity in the high-field region between gate and drain. Potential challenges are the composition control of the $InAs_{1-x}P_x$ layers and mobility degradation of both the InAs and $InAs_{1-x}P_x$ layers arising from strain.

The objective of this work is to determine the growth conditions required to achieve high mobilities in both the InAs channel and the $InAs_{1-x}P_x$ subchannel. Several sets of layer structures are used to study the effect of the substrate temperature and phosphorus content on the mobilities in InAs and $InAs_{1-x}P_x$ channel layers. Phosphorus ratios are investigated by dynamic secondary ion mass spectrometry (SIMS). In addition to room-temperature Hall measurements, temperature-dependent Hall measurements are performed on selected samples to understand the effect of strain on the mobilities and carrier concentrations in the composite channels. We also report the dc and rf performance of InAs/InAsP composite-channel HFETs that are based on these newly developed materials.

The samples were grown by solid-source molecular beam epitaxy (MBE) on semi-insulating (001) GaAs substrates. On top of a 2-μm-AlSb buffer layer and a 0.25-μm-$Al_{0.8}Ga_{0.2}Sb$ mesa floor, which were grown at 570 and 530 °C, respectively, three different structures were grown (Fig. 1). The structures in Figs. 1(a) and 1(b) were designed to characterize InAs channels and $InAs_{1-x}P_x$ subchannels, respectively, and the structure in Fig. 1(c) shows the HFET device profile. Except for the $InAs_{1-x}P_x$ subchannel layers, the same growth temperature (T_G), 480 °C, was used in each layer above the 8-nm-AlSb bottom barrier. Interfaces between the well and its barriers were forced to be InSb-like.[11] In samples used for HFET fabrication, [Fig. 1(c)], p-type Be (1.5×10^{12} cm^{-2}) and n-type Te (0.9

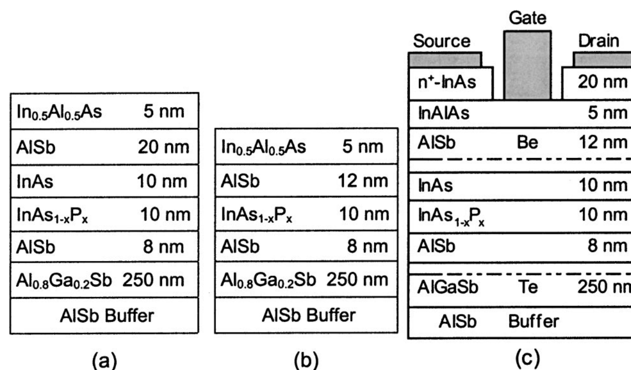

FIG. 1. (a) InAs/$InAs_{1-x}P_x$ composite-channel 2-DEG structure; (b) $InAs_{1-x}P_x$ 2-DEG structure; (c) InAs/$InAs_{1-x}P_x$ composite-channel HFET profile.

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$\times 10^{12}$ cm^{-2}) delta doping sheets, 50 Å above and 300 Å below the composite channels, respectively, were introduced both for modulation doping and to introduce a vertical field in the well to facilitate electron transfer between the InAs and $InAs_{1-x}P_x$ layers. Double caps, n^+-InAs cap (1×10^{19} cm^{-3}) and InAlAs, were used to develop a recessed gate in order to reduce the series resistance in source and drain access regions.

The InAsP layers were grown as digital alloys. During $InAs_{1-x}P_x$ growth, the In shutter, the As valve and the P valve were kept open and the As and P fluxes controlled only by shutters. The In flux was such that the bulk InAs growth rate is 0.25 μm/h, while the As and P fluxes were such that the growth was always group-V rich. Given the shutter times and growth rates employed, we estimate an ~1 nm superlattice period. During shuttering, there is likely a significant group V background in the chamber, hence the intended InAs and InP layers forming the superlattice may contain significant concentrations of P and As, respectively. Because P is particularly volatile, we expect the P composition in the $InAs_{1-x}P_x$ superlattice to be higher than expected from the shutter times employed. This is supported by x-ray diffraction measurements of unstrained, bulk $InAs_{1-x}P_x$ digital alloys grown by the same approach.

Samples in van der Pauw geometry were prepared for 10–300 K Hall measurements. For samples grown with n^+-InAs/$In_{0.5}Al_{0.5}As$ caps, Hall measurements were performed only after removing the n^+-InAs cap, so as to prevent parallel conduction in this layer. $InAs_{1-x}P_x$ composition was also examined through the relative As and P secondary ion fluxes using a Physical Electronics 6650 Quadrupole secondary ion mass spectrometer (SIMS). A Cs^+ primary ion beam (1 kV) formed 80×80 μm^2 craters. Only positive secondary ions were monitored, ion data were collected from the center 15% of the ion crater area, and no electron beam charge neutralization was required. SIMS calibration is not absolute and hence these data provide only a relative comparison of P content between $InAs_{1-x}P_x$ samples.

The layer structures in Fig. 1(a) and 1(b) were designed to characterize InAs channels and $InAs_{1-x}P_x$ subchannels, respectively. Band calculations for the structure of Fig. 1(a) indicated that most electrons were located in the InAs channel, hence the measured Hall mobility (μ_H) is that of the InAs channel layer. Table I lists the room-temperature Hall and SIMS data for samples with varying $InAs_{1-x}P_x$ compositions and growth temperatures. At a fixed growth temperature we observed (Table I) a monotonic relationship between the phosphorous proportion x determined by SIMS (SIMSPR) and the P shutter time ratio (PSR), the percentage time in which the P shutter is open during growth of one $InAs_{1-x}P_x$ superlattice period. At 480 °C growth temperature, μ_H becomes poorer with increased P shutter time ratios. At a fixed PSR, increased growth temperature resulted in reduced mobilities, increased sheet carrier concentrations (N_s) and increased SIMSPR, which are particularly pronounced at growth temperatures between 480 and 530 °C. At 430 °C growth temperature, the carrier concentration is low and the $\mu_H > 20\,000$ cm^2/V s even for a 40% PSR in the $InAs_{1-x}P_x$ subchannel.

To independently characterize the $InAs_{1-x}P_x$ subchannels, similar quantum well structures were grown in which the InAs well layers were omitted [Fig. 1(b)]. Samples with 20% PSR were grown at 400, 430, and 460 °C (Table II). The highest mobility (7100 cm^2/V s) and the lowest carrier concentration are obtained for 430 °C growth. Note that 430 °C growth temperature also produced the highest InAs channel mobility (Table I). $InAs_{1-x}P_x$ growth with 30% PSR (Table II) resulted in similar 5700 cm^2/V s mobility and carrier concentration as growth with 20% PSR.

TABLE I. Measured SIMS and room-temperature Hall data for the $InAs/InAs_{1-x}P_x$ composite-channel 2-DEG structures [Fig. 1(a)] with nominal x: 0–0.4 grown at 430, 480, and 530 °C. As/P shutter time is respective open times of As and P shutters in one period of digital $InAs_{1-x}P_x$ superlattice.

Sample	As/P shutter time (s)	T_G (°C)	μ_H (cm^2/V-s)	N_s (cm^{-2})	PSR (%)	SIMSPR (%)
A	14.40/0	480	26.1×10^3	1.1×10^{12}	0.0	0.0
B	12.96/1.58	480	21.5×10^3	1.2×10^{12}	10.9	22.8
C	12.24/2.38	480	23.3×10^3	1.1×10^{12}	16.3	26.0
D	11.52/3.17	480	17.2×10^3	1.2×10^{12}	21.6	32.1
E	11.52/3.17	480	19.9×10^3	1.1×10^{12}	21.6	32.1
F	10.8/3.96	480	16.5×10^3	1.3×10^{12}	26.8	36.4
G	10.8/3.96	480	17.8×10^3	1.1×10^{12}	26.8	36.7
H	10.08/4.75	480	14.4×10^3	1.3×10^{12}	32.0	38.4
I	11.52/3.17	430	22.5×10^3	1.1×10^{12}	21.6	30.5
J	10.8/3.96	430	23.2×10^3	1.0×10^{12}	26.8	33.4
K	10.08/4.75	430	23.2×10^3	1.1×10^{12}	32.0	38.2
L	8.64/6.34	430	20.9×10^3	1.2×10^{12}	42.3	39.8
M	11.52/3.17	530	1.6×10^3	3.1×10^{12}	21.6	38.2

Hall measurements were performed between 10 and 300 K for composite-channel samples A, B, D, and H in Table I (Fig. 2). Samples with low PSR or SIMSPR exhibit the greatest increase in mobility at low temperatures. Carrier concentration increases monotonically with PSR or SIMSPR.

Prior studies on InAs/AlSb quantum wells indicated that the electron mobilities are limited by phonon scattering at room temperature and by interface roughness scattering at low temperatures.[12,13] The strain introduced by the $InAs_{1-x}P_x$ subchannel may increase interface roughness[14] and defects may be generated if the strain relaxes, both effects introducing scattering centers, and degrading mobility. Defects generated by strain relaxation can also act as donors, thereby increasing the quantum well electron concentration. Moderately reduced growth temperature can suppress lattice relaxation and prevent defect generation.[14,15] This may explain the high mobilities and low carrier concentrations observed (Table I) at 430 °C growth temperature even for samples with high SIMSPR (high strain).

TABLE II. Measured room-temperature Hall data for the $InAs_{1-x}P_x$ 2-DEG structures [Fig. 1(b)] with nominal x: 0.2–0.3 grown at 400, 430, and 460 °C growth temperatures.

Sample	As/P shutter time (s)	T_G (°C)	μ_H (cm^2/V s)	N_s (cm^{-2})	PSR (%)
N	11.52/2.88	400	5.3×10^3	1.1×10^{12}	21.6
O	11.52/2.88	430	7.1×10^3	8.1×10^{11}	21.6
P	11.52/2.88	460	4.8×10^3	2.0×10^{12}	21.6
Q	10.08/4.32	430	5.7×10^3	8.4×10^{11}	32.0

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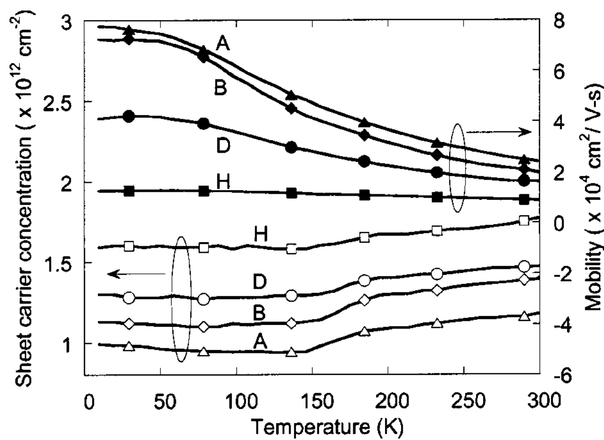

FIG. 2. Low-temperature Hall measurements for the samples A, B, D, and H in Table I.

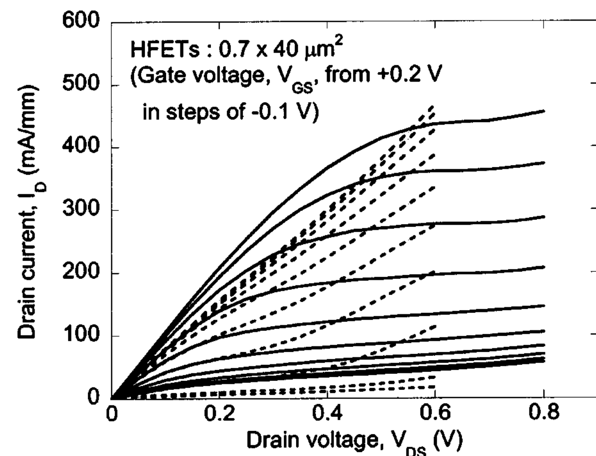

FIG. 3. dc common-source characteristics of $InAs/InAs_{1-x}P_x$ composite-channel (solid lines) and InAs single-channel (dotted lines) HFETs with 0.7-μm-gate lengths.

In contrast, for samples grown at 480 °C, mobilities and carrier concentrations change with phosphorus ratio (Table I and Fig. 2). Note that at 30% PSR (sample H), mobility varies little with temperature throughout the measured range (Fig. 2), indicating that the dominant scattering mechanism at room temperature is not phonon scattering. Instead, we suspect that scattering from either interface roughness or strain-generated defects dominates. Raising growth temperature from 480 to 530 °C, SIMSPR increases, mobility decreases, and carrier concentration increases greatly (Table I). This suggests that higher strain due to enhanced P incorporation into the $InAs_{1-x}P_x$ layer together with increased strain relaxation at the increased growth temperature significantly degraded the $InAs/InAs_{1-x}P_x$ composite channels.

Based on the above growth studies, an $InAs/InAs_{1-x}P_x$ (nominal $x=0.2$) composite-channel structure [Fig. 1(c)] was grown for HFET fabrication. Hall measurement showed 14 500 $cm^2/V\,s$ electron mobility and 1.7×10^{12} cm^{-2} electron sheet concentration. HFETs were fabricated using Pd/Ti/Pd/Au source and drain contacts, mesa isolation, a recess etch through the n^+ InAs cap in the gate contact region, and separate Ti/Pt/Au gate and interconnect metal depositions. In regions where the n^+ cap was not removed, the sheet resistance was 220 Ω/sq., while the specific contact resistance was 0.065 Ω mm.

Figure 3 compares the common-source dc characteristics of 0.7-μm-gate length HFETs using simple InAs and composite $InAs/InAs_{1-x}P_x$ channels. For $V_{DS}>0.2$ V, the composite-channel devices show a marked reduction in the dc output conductance ($G_{DS}\equiv\partial I_D/\partial V_{DS}$), with G_{DS} reduced from 415 to 30 mS/mm at $V_{DS}=0.6$ V and $I_D=200$ mA/mm. In addition, the source-drain breakdown voltage exceeds 0.8 V for the composite-channel device. A high 950 mS/mm peak transconductance is observed for a 0.5-μm-gate length device. From 5 to 40 GHz S-parameters measurements of a 0.7-μm-gate-length composite-channel HFET, extrapolated current gain and power gain cutoff frequencies of 46 and 61 GHz were determined. Thus, compared to InAs-channel devices, composite-channel HFETs show significantly improved breakdown voltage and significantly reduced dc output conductance. It suggests reduced impact ionization for the composite channel device. InAs/InAsP composite-channel HFETs warrant further investigation as potential enhancement to InAs-based HFETs.

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