Design and characteristics of strained InAs/InAlAs composite-channel heterostructure field-effect transistors

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We report composite-channel heterostructure field-effect transistors (HFETs) with an InAs channel and an $In_{0.9}Al_{0.1}As$ subchannel. The HFETs are grown on antimonide buffer layers. Two composite-channel structures with different planar Te doping schemes are designed, fabricated, and characterized. High radio-frequency transconductances of above 0.9 S/mm and ~55 GHz current gain cutoff frequencies are achieved in devices with 500 nm gates. Planar Te doping in the buffer layers reduces the high kink-effect currents otherwise found in InAs/AlSb HFETs, an effect which can be attributed to either increased breakdown field in the $In_{0.9}Al_{0.1}As$ subchannel or to suppression of hole blocking in the buffer. The present limitations to device performance and suggested approaches for their elimination are discussed. © *2005 American Institute of Physics*.
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I. INTRODUCTION

The InAs/AlSb quantum well system is attractive for the realization of high-speed low-power heterostructure field-effect transistors (HFETs) because of high electron mobility (as high as 30 000 $cm^2/V\,s$ at 300 K) and high feasible sheet electron density.[1] Due to the narrow InAs energy gap of ~0.36 eV, impact ionization effects can become dominant for short gate lengths when drain bias exceeds the energy gap in the channel.[2,3] Further, because the staggered band lineup at InAs/AlSb heterojunctions leaves holes without confinement, some of the impact-ionized holes are drawn into negatively biased gate, giving rise to a significant gate leakage component; others accumulate in the buffer layers and induce nonsaturating drain characteristics by the feedback mechanism, known as the kink effect.[4,5]

Proposed approaches to improve breakdown include the use of a back gate,[6] increased quantum confinement,[7] dual gating,[8] and an additional InAs subchannel.[9] In InGaAs/InAlAs HFETs grown on InP substrates, breakdown voltage can be greatly improved by using an InGaAs/InP composite channel, wherein low-field electron transport under the HFET gate occurs in the high-mobility InGaAs layer, and high-field transport between gate and drain in the wide band gap InP layer.[10–12] Considering the band lineup and lattice constants, InAs/InAsP and InAs/InAlAs are two possible material combinations to form composite channels in antimonide-based HFETs. Studies of $InAs/InAs_{0.8}P_{0.2}$ composite channel have been reported elsewhere.[13] A potential challenge with such channels is the composition control of group V components.

As an alternative to the growth difficulties of InAsP channels, $InAs/In_{0.9}Al_{0.1}As$ composite-channel HFETs are designed, fabricated, and characterized in the present work. The objective is to increase the breakdown voltage of InAs-based HFETs through the increased band gap of the inserted $In_{0.9}Al_{0.1}As$ subchannel. $In_{0.9}Al_{0.1}As$ has a direct 0.57 eV band gap, and a large separation (~0.6 eV) between Γ and L conduction band minima.[14–16] We therefore expect high peak electron velocity in the high-field region between gate and drain. Because the InAs channel and $In_{0.9}Al_{0.1}As$ subchannel are, respectively, −1.27% and −1.94% lattice mismatched to the AlSb buffer layer, strain effect on the band gap and band lineup must be considered in the layer design and simulation. Because doping is an important factor on the carrier distribution and transfer in the composite channel,[10,17] we choose two different doping schemes in this study: one doping scheme is planar Te doping in top barrier, while the second is Te doping in the buffer layers. Finally, the structural design and measured dc and microwave characteristics are discussed.

II. DESIGN, GROWTH, FABRICATION AND CHARACTERIZATION

A. Strained band gap engineering and one-dimensional simulation

As mentioned earlier, a composite-channel device benefits from high mobility in the narrow band gap channel, and large impact ionization energy and high saturation velocity in the wide band gap subchannel. To fully take advantage of the composite channel, it is important to assure carrier transfer to the wide band gap $In_{0.9}Al_{0.1}As$ subchannel in the HFET high field region before hot electrons can impact ionize in the narrow band gap channel. This high-field region lies between the gate and drain. Proper introduction of a vertical electric field into the layer structure and carefully controlled conduction band offset between the two channels are crucial design

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parameters controlling carrier transfer. In the strained $In_{0.9}Al_{0.1}As$ composite channel cladded by AlSb buffer and top barrier, the band gaps of InAs and $In_{0.9}Al_{0.1}As$ and their band offsets must be evaluated in order to predict the carrier distribution in the composite channel as a function of bias.

To avoid generation of defects at the interface due to lattice relaxation, and to avoid degradation in the composite channel transport properties, the total strain energy introduced by the strained InAs and $In_{0.9}Al_{0.1}As$ layers cannot exceed a critical value, above which the nucleation of misfit dislocation occurs. The thickness of the epilayer which corresponds to the critical strain energy defines the critical thickness in the system. In discussing the problem of the critical thickness, we follow the considerations presented by Ball and van der Merwe.[18] The basic assumption of the theory is that the configuration of the epitaxial system is the one of minimum energy. For a particular bicrystal which consists of a semi-infinite substrate/buffer M and an epitaxial layer N of thickness t grown along the (001) direction (M denotes AlSb and N denotes $In_xAl_{1-x}As$ in this work), the critical thickness t_c of the $In_xAl_{1-x}As$ epitaxial layer is given as

$$t_c = \frac{b(1-\nu\cos^2\beta)}{8\pi|f_0|(1+\nu)\sin\beta\cos\gamma}\ln\left(\frac{\rho t_c}{b}\right), \tag{1}$$

where b is the magnitude of the Burgers vector. β and γ are the angles between the Burgers vector and the dislocation line, and between the glide plane of dislocation and the interface, respectively, ν is Poisson's ratio and ρ is a numerical factor used to take the core energy of dislocation into account (usually $\rho=4$).[18] The term f_0 is the natural misfit between the $In_xAl_{l-x}As$ and the AlSb buffer, and defined by

$$f_0 = \frac{a_0^{\mathrm{str}} - a_0}{a_0} \tag{2}$$

where a_0^{str} and a_0 stay for the lateral atomic spacing in the strained and unstrained overgrown layers. From (1), t_c may be calculated for a given natural misfit f_0.

When strain is insufficient to form defects, growth of the $InAs/In_{0.9}Al_{0.1}As$ layers is elastically strained, and it is reasonable to apply elastic theory to evaluate the band gap and band lineup. Assuming[19] that hydrostatic strain only causes a shift in the conduction band edge, and biaxial strain splits the degenerate valence band heavy-hole and light-hole maxima, the shifts of conduction band edge (ΔE_c), heavy-hole band edge (ΔE_{hh}), light-hole edge (ΔE_{lh}), and split-off band edge (ΔE_{so}) can be described by

$$\Delta E_c = a_c(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}), \tag{3}$$

$$\Delta E_{\mathrm{hh}} = a_v(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) - \frac{1}{2}\delta E_{001}, \tag{4}$$

$$\Delta E_{\mathrm{lh}} = a_v(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) - \frac{1}{2}\Delta_0 + \frac{1}{4}\delta E_{001} + \frac{1}{2}\left[\Delta_0^2 + \Delta_0\delta E_{001} + \frac{9}{4}(\delta E_{001})\right]^{1/2}, \tag{5}$$

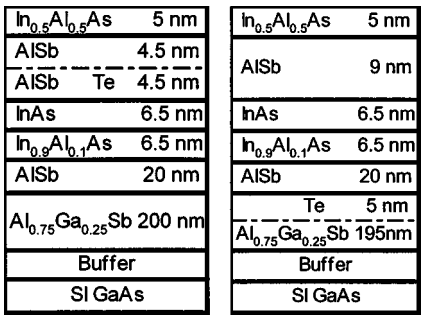

FIG. 1. Schematic composite-channel layer structures for HFETs with (a) a top-barrier planar Te doping (structure A) and (b) a buffer planar Te doping (structure B).

$$\Delta E_{\mathrm{so}} = a_v(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) - \frac{1}{2}\Delta_0 + \frac{1}{4}\delta E_{001} - \frac{1}{2}\left[\Delta_0^2 + \Delta_0\delta E_{001} + \frac{9}{4}(\delta E_{001})\right]^{1/2}, \tag{6}$$

where a_c and a_v are hydrostatic deformation potential for the conduction and valence band respectively, ε_{xx} and ε_{yy} correspond to the strain tensors parallel to the interface plane, and ε_{zz} corresponds to strain tensor perpendicular to the interface plane. Δ_0 is spin-orbit splitting energy, and δE_{001} is given by $\delta E_{001}=2b'(\varepsilon_{zz}-\varepsilon_{xx})$, where b' is the shear deformation potential. All parameters used in the above equations are available either from analytic calculations or experimental data for most III–V compound semiconductors.[20]

To understand the carrier distribution and transfer behavior in the quantized $InAs/In_{0.9}Al_{0.1}As$ composite channel, a one-dimensional simulator,[21] which simultaneously solves Poisson's and Shrödinger's equations self-consistently, was used. Based on the above calculation, the effect of strain on the composite channel conduction and valence bands was also taken into account in the program. Simulating two device layer structures shown in Fig. 1, we obtained their band diagram with quantum states and carrier distribution in the composite channel. A plot which includes the relationship between the bias and normalized carrier population in each channel will be shown.

B. Growth and fabrication

The material for this study was grown by molecular beam epitaxy employing a solid-source Gen II MBE machine. The growth front was monitored by reflection high-energy electron diffraction (RHEED) and the growth temperatures were measured by a pyrometer facing the wafer. The samples initially used 300 Å AlSb for the buffer layer, which was grown metamorphically on a semi-insulating 2 in. GaAs wafer at 570 °C. During growth of the mismatched AlSb layer, the RHEED pattern transferred from a spotty one to a streaky 1×3 reconstructed pattern within the first 100 Å of AlSb growth. Thereafter a 0.8 μm-thick $Al_{0.8}Al_{0.2}Sb$ buffer was grown as the growth temperature was lowered to 530 °C. This layer is included because it is more resistant to oxidation than AlSb. The active device layers were grown on top of the buffer layers. These included a 2000-Å-thick $Al_{0.75}Ga_{0.25}Sb$ layer, which serves as a chemically stable

mesa floor, a 200 Å thick AlSb back barrier, a 130 Å strained $InAs/In_{0.9}Al_{0.1}As$ (65 Å/65 Å) composite channel, a 90-Å-thick AlSb top barrier, and a 50 Å highly lattice-mismatched $In_{0.50}Al_{0.50}As$ cap layer. The strained $In_{0.9}Al_{0.1}As$ subchannel layer was deliberately grown at low 450 °C to suppress defect generation due to lattice relaxation.[22,23] A Te delta doping sheet was used in each of the two structures grown, where one structure used 3×10^{12} cm^{-2} doping 45 Å above the InAs channel; the other structure used 1.5×10^{12} cm^{-2} doping 250 Å below the $In_{0.9}Al_{0.1}As$ subchannel.

The devices were fabricated using a conventional planar process. After depositing Pd/Ti/Pd/Au source and drain contacts,[24] which were annealed at 180 °C for 20 min in the air, device mesas were formed for device isolation using both wet and dry etching processes. Following optical gate lithography, Ti/Pd/Au gate metals were then evaporated and lifted off. Finally, Ti/Pd/Au interconnects bonding pads were formed by metal evaporation and lift-off.

C. Electrical characterization

Standard electrical measurements were used to characterize material quality and device performance. Room-temperature Hall measurements were performed in van der Pauw geometry on as-grown material. From Hall data, low-field carrier mobility and sheet resistance in the composite channel were obtained. During device fabrication, contact resistance and sheet resistance were examined using transmission line method (TLM) patterns. HFET common-source dc characteristics were measured, and S parameters were measured on wafer from 5 to 40 GHz. From the measured S parameters, we determined the current gain, h_{2l}, Mason's unilateral power gain, U, and radio-frequency (rf) transconductance. The cutoff frequency, f_T, and maximum oscillation frequency, $f_{\max}$, were obtained by extrapolating $|h_{2l}|^2$ and U to 0 dB, respectively, with a -20 dB/decade slope after removing the effects of the pad parasitic capacitances through standard de-embedding techniques.

III. RESULTS

A. Band gap engineering and simulation results

When AlSb/AlGaSb buffer layers are grown, the lattice constant is not precisely controlled. Therefore, in our calculations, we instead modeled growth on an AlSb buffer. Note that the AlSb buffer has a slightly larger lattice constant, and the calculated critical thickness is thereby slightly smaller than what it should be. Based on (1), the critical thickness as a function of In ratios of $In_xAl_{1-x}As$ grown on AlSb was calculated (Fig. 2). We calculate 180 Å critical thickness for InAs grown on AlSb, and 110 Å for $In_{0.9}Al_{0.1}As$ grown on AlSb. In the reported HFETs, both layers were grown at 65 Å thickness, hence the accumulated strain energies of the two layers are 36% and 59% of the critical strain energy. We assume that the critical energy is similar in the InAs and $In_{0.9}Al_{0.1}As$ layers. The total accumulated strain energy is 95% of the critical strain energy. This suggests that both InAs channel and $In_{0.9}Al_{0.1}As$ subchannel were grown pseudomorphically, and hence Eqs. (3)–(6) describe the changes in band gaps and band offsets resulting from strained layer growth of the composite channel. Results are shown in Fig. 3, where the InAs and $In_{0.9}Al_{0.1}As$ band gaps decreased from 0.36 and 0.57 eV to 0.23 and 0.34 eV, respectively. The calculated conduction band offset between the InAs channel and the $In_{0.9}Al_{0.1}As$ subchannel is 94 meV. In addition, the composite channel system maintains the advantage of a deep quantum well, but maintains the disadvantage of a zero of hole confinement in the channel.

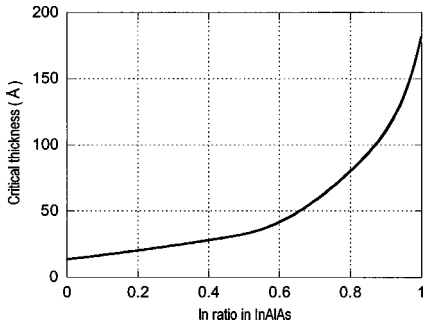

FIG. 2. Critical thickness dependence on In ratio for the $In_xAl_{1-x}As$ layer grown on AlSb buffer.

Applying the results of these band calculations, the two device structures were simulated.[21] Figures 4(a) and 4(b) represent the band diagrams of the A and B layer structures shown in Figs. 1(a) and 1(b), respectively. The quantized ground and second states are shown as E_0 and E_1 in each figure. A study of carrier distribution and sheet carrier concentration versus gate bias is given in Fig. 5. Both devices yield the same -0.82 V threshold voltage. With no gate bias applied, 75% electrons are in the InAs channel in the A structure, compared to 53% in the B structure. As negative gate bias is applied, electrons transfer to the $In_{0.9}Al_{0.1}As$ layer. Over 50% of the electrons are in the $In_{0.9}Al_{0.1}As$ subchannel at a low -0.2 V gate bias for the B structure, but less than 35% of the electrons in the A structure transfer to the $In_{0.9}Al_{0.1}As$ subchannel even with gate bias at the threshold voltage. The A structure, having Te doping in the top barrier, will not effectively transfer electrons to the wide band gap $In_{0.9}Al_{0.1}As$ subchannel in the HFET's high-field regions.

B. Material and device performance

Table I lists the mobility, sheet carrier density, and sheet resistance in the Hall measurements for the two as-grown

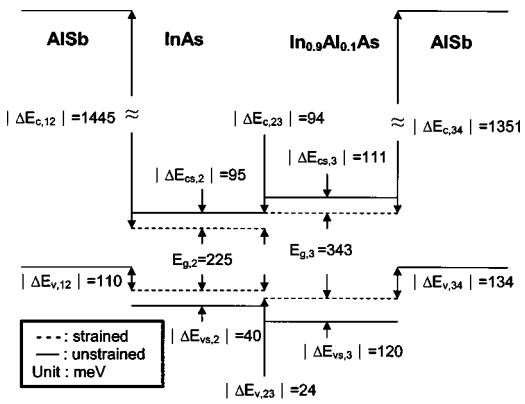

FIG. 3. Calculated band edge shifts of the strained $InAs/In_{0.9}Al_{0.1}As$ composite channel. 1:top AlSb; 2: InAs; 3: $In_{0.9}Al_{0.1}As$; 4: bottom AlSb.

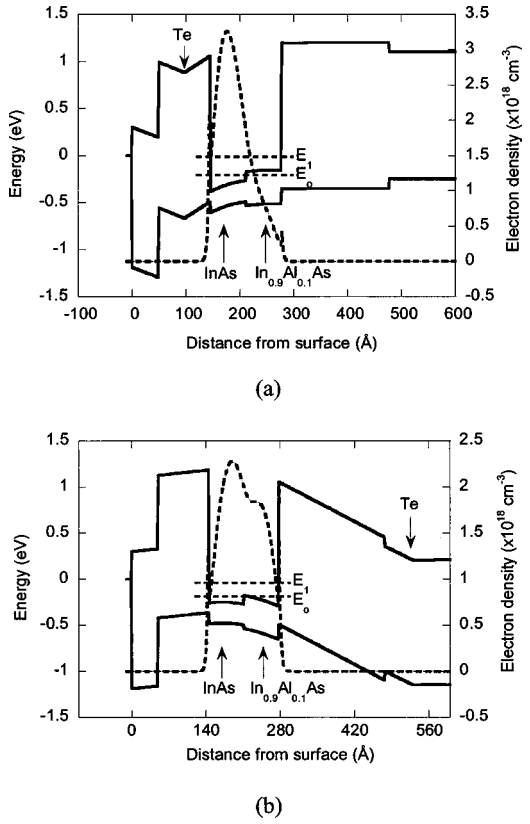

FIG. 4. Calculated band diagrams and carrier distributions for (a) A structure and (b) B structure. E_0 and E_1 are ground and second bound states, respectively.

structures. Sheet resistance and contact resistance in the TLM measurements after device fabrication are also shown. Mobilities near 17 000 $cm^2/V\,s$ were measured in both structures. The similar sheet resistance in both measurements implies that high low-field mobility in the composite channel is maintained. Based on these results, the source series resistances, R_s, are estimated to be 0.38 Ω-mm for both structures when 2 μm source-to-gate spacing is employed.

Figures 6(a) and 6(b) show common-source dc characteristics for the two devices with 0.5 μm gate length. The HFET dc curves measured on sample A yield high kink currents for V_{ds} greater than approximately 0.3 V. This is typically observed in InAs single-channel HFETs. Moreover, the threshold voltage, V_{th}, shows a strong dependence of drain bias, shifting from -0.8 V ($V_{ds} \leqslant 0.3$ V) to -1.2 V (V_{ds} $=0.8$ V). It is noted the measured threshold voltage at low drain bias shows good agreement with simulation. For the sample B HFET, reduced kink currents are observed at high drain biases. The figure shows both the measured source and drain currents. Note that the increase in the drain currents for $-0.6\ \text{V} \leqslant V_{gs} \leqslant -0.8\ \text{V}$ and $0.6\ \text{V} \leqslant V_{ds} \leqslant 0.8\ \text{V}$ is not reflected as a corresponding increase in the source currents. This indicates that the increased drain current under this bias region is due to direct gate-to-drain leakage, and not source-to-drain breakdown associated with the kink effect.

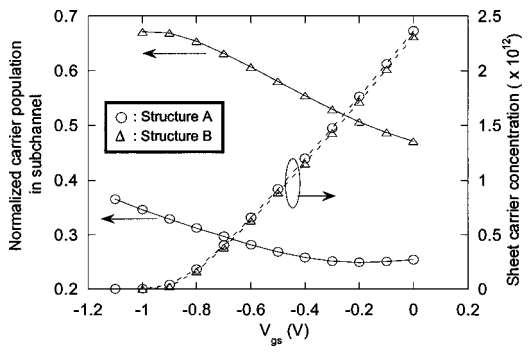

FIG. 5. Gate voltage dependence of calculated sheet carrier concentrations and normalized carrier populations in the $In_{0.9}Al_{0.1}As$ subchannel.

TABLE I. Summary of Hall and TLM results.

Structure	μ ($cm^2/V\,s$)	N_s (cm^{-2})	Hall R_s (Ω/sq.)	TLM R_s (Ω/sq.)	R_c (Ω/mm)
A	17 500	2.30×10^{12}	155	154	0.071
B	16 660	2.78×10^{12}	135	140	0.108

In Fig. 7, a strong evidence of serious impact ionization in the HFET of sample A is characterized by the peak gate currents near V_{th}.[5,7] At 0.8 V drain bias, for example, the on-state gate leakage current is as high as 10 mA/mm, while the off-state gate current is lower than 0.6 mA/mm. Figure 8 shows the dependence of the transconductance, g_m, and drain current on the gate bias, V_{gs}, at 0.7 V drain bias for both samples. Compared to 800 mS/mm peak transconductance

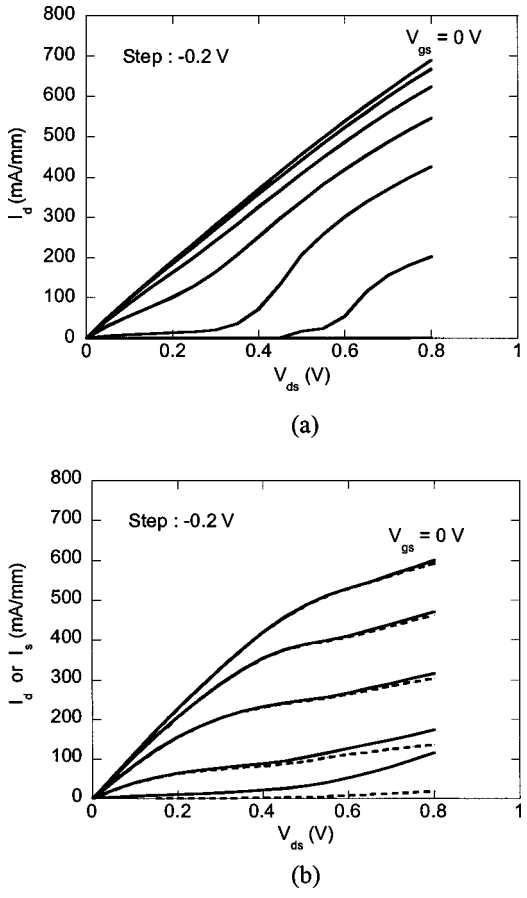

FIG. 6. Common-source dc characteristics of the two composite-channel HFETs with a gate of 0.5×40 μm^2. (a): A structure; (b): B structure. The dotted curves in (b) are the source current while the solid lines are the drain current.

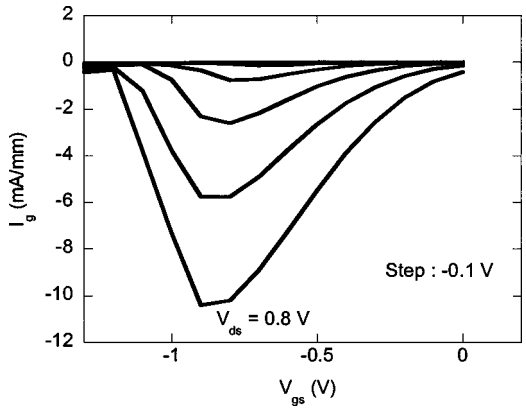

FIG. 7. Gate leakage current of the 0.5 μm gate length device shown in Fig. 6(a).

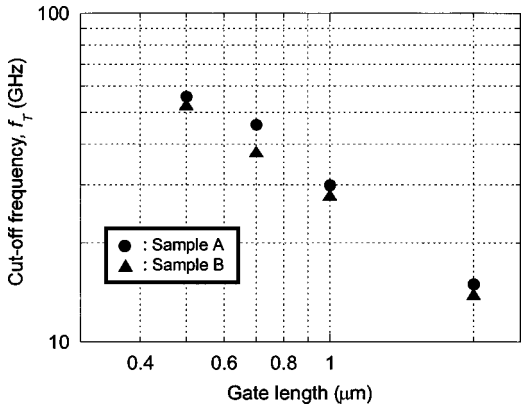

FIG. 9. Gate length dependence of current gain cutoff frequencies.

and -0.78 V threshold voltage in the HFET of sample B, the HFET of sample A shows a higher 1300 mS/mm peak transconductance and more negative -1.15 V threshold voltage. The peak of dc transconductance near $V_{gs}=V_{th}$ is often associated with the kink effect.[25]

The gate length dependence of current gain cutoff frequency, f_T, for both A and B devices are shown in Fig. 9. Slightly higher f_T is obtained with sample A. The maximum f_T obtained for samples A and B with 0.5 μm gate length are 56 and 53 GHz, respectively, while the maximum oscillation frequencies, f_{max}, are 65 and 73 GHz. From the measured S parameters, the 0.5 μm gate length HFETs of samples A and B showed transconductances of 900 mS/mm ($V_{ds}=0.3$ V, $V_{gs}=-1.1$ V) and 975 mS/mm ($V_{ds}=0.7$ V, $V_{gs}=-0.38$ V) at 25 GHz, respectively. Note that the two samples show dc transconductances of 4 and 800 mS/mm at these bias conditions. There is consequently stronger evidence in sample A than in sample B of the dc-rf dispersion commonly associated with the kink effect. From the variation of $1/(2\pi f_T)$ versus gate length, we determine average electron velocities of 1.9 and 1.8×10^7 cm/s for samples A and B. From the observed extrinsic transconductances at 25 GHz and the source access resistance determined from TLM data, the intrinsic rf transconductances are 1370 and 1550 mS/mm in the HFETs of samples A and B, respectively.

IV. DISCUSSION

The generally accepted theory of kink effect in conventional InAs/AlSb HFETs is that impact-ionized holes generated in the high-field region of the channel accumulate primarily in the buffer.[5] This causes an increase in drain current, which then further shifts device threshold voltage. In the simulation, it is predicted that only the B structure with the Te planar doping in the buffer shows the effective carrier transfer from the InAs channel to the $In_{0.9}Al_{0.1}As$ subchannel (Fig. 5), as is required to take advantage of the increased band gap of the composite channel. Experimental data with sample A support this conclusion: drain breakdown is low, gate leakage shows a pronounced peak near threshold, and there is strong dc-rf dispersion in transconductance. The sum of the 0.225 eV band gap of the strained InAs channel and the 0.06 eV well ground state energy approximately corresponds to the bias at which strong gate leakage and high drain conductance are observed. This observation is consistent with Bude and Hess's full-band structure Monte Carlo calculation:[26] a large $E_{\Gamma-X}$ and $E_{\Gamma-L}$ separation, coupled with a narrow band gap, leads to the threshold energy of impact ionization close to the band gap energy. Experimental data for the HFET of sample B shows reduced drain conductance and greatly reduced dc-rf dispersion in transconductance. These data suggest reduced kink effect through hole accumulation while Te dopping in the buffer provides a vertical electric field for electron transfer to the wide band gap $In_{0.9}Al_{0.1}As$ subchannel in the HFET high-field region, and it also provides a valence band potential in the substrate, which inhibits hole accumulation in the buffer. Both effects will reduce the kink effect. With the presently available data, we cannot determine quantitatively the respective magnitudes of the two effects. Observation of the peak in gate leakage current (Fig. 7) is not a useful indicator of kink effect for sample B because such features are swamped by high gate leakage current.

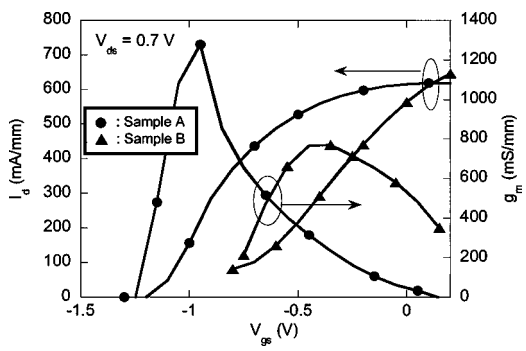

FIG. 8. Direct current transconductance and drain current as a function of gate bias at 0.7 V drain bias.

To better understand the gate leakage current, it was measured as a function of V_{gs}, with $V_{ds}=0$ V. The experimental configuration is shown in the inset of Fig. 10, while the experimental data and approximate theoretical calculation are in Fig. 11. The theoretical calculations, by the Wentzel–Kramers–Brillouin (WKB) method,[27] assume gate leakage by tunneling between bound states in the InAs well and valence band states in the barrier (Fig. 10). The depletion region extends laterally from the region under the gate at $V_{gs}\sim V_{th}$, becoming progressively wider as V_{gs} is made more

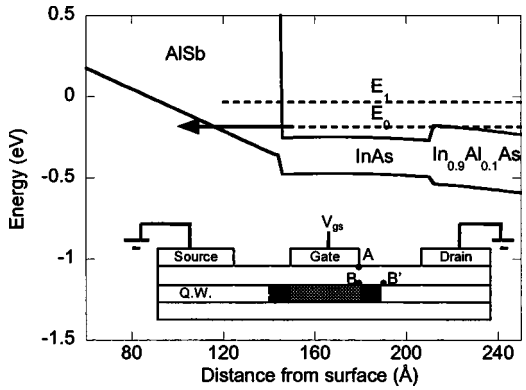

FIG. 10. Calculated band structure, along the line A-B, for the HFET of structure B at a high gate bias voltage. The arrow shows the interband tunneling between the InAs channel and the AlSb valence band. The inset is the schematic device profile where source and drain are grounded. The crosshatched area in the quantum well represents the depletion region for $V_{gs} \sim V_{th}$; the black area represents the lateral expansion of the depletion region from $V_{gs} \sim V_{th}$ to $V_{gs} \ll V_{th}$.

negative (B vs B' in the inset of Fig. 10). This lateral depletion distance is hard to calculate, and is neglected in the tunneling calculations, which assume that the full potential V_{gs} is applied between points A and B of Fig. 10. The calculations further assume tunneling between the full area of gate electrode and the two-dimentional electron gas of the quantum well below it. This latter approximation is reasonable for $V_{gs} > V_{th}$ but fails below pinchoff.

As shown in Fig. 11, the observed reduction in gate-channel breakdown of sample B is consistent with WKB calculations, although the very close agreement must be viewed as statistically fortuitous. WKB calculations predict a larger gate-drain breakdown for sample A, and yet larger breakdowns are observed experimentally. These data suggest that the high gate leakage at sample B results from band-band tunneling associated with the high vertical field in the AlSb top barrier layer.

Introduction of a vertical field by Te doping of the buffer layer is necessary for electron transfer to the wide band gap $In_{0.9}Al_{0.1}As$ layer, but increases the field in the top barrier and hence increases gate leakage through tunneling. The Te buffer doping also improves hole confinement through introducing a valence band energy barrier. Options to decrease gate leakage include dipole doping of the top barrier, or a strained $In_{0.5}Al_{0.5}As$ layer in the top barrier to increase the valence band energy barrier.

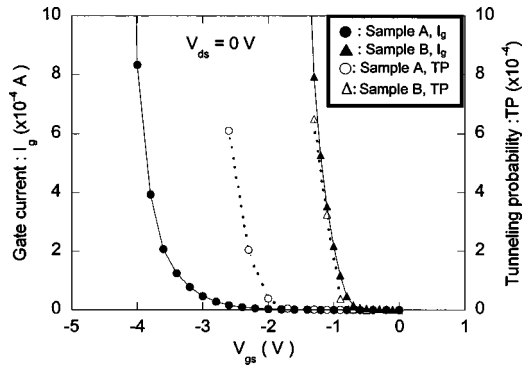

FIG. 11. The gate bias dependence of measured gate currents and calculated interband hole tunneling probabilities for the HFETs of samples A and B with grounded source and drain.

V. CONCLUSION

We have demonstrated an $InAs/In_{0.9}Al_{0.1}As$ composite-channel HFET that alleviates the serious kink currents in InAs single-channel HFETs. As shown in both simulation and device results, a vertical electrical field for enhanced carrier transfer coupled with a hole barrier in the buffer layers are important parameters in composite-channel layer design. The present limitation to our composite-channel devices is the enhanced gate leakage currents at high gate biases arising from the high vertical field and the InAs/AlSb type-II lineup which results in increased interband tunneling. Further work is needed to reduce gate leakage. An $InAs/In_{0.9}Al_{0.1}As$ composite channel coupled with a hole blocking Te doping in the buffer provides an alternative approach to alleviate the high kink currents in the InAs single-channel HFETs.

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