Implanted pedestal-subcollector InP DHBT technology

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Continued scaling of InP based double heterojunction bipolar transistors (DHBTs) is required for their use in high speed, low power digital logic and mixed-signal systems. The base collector capacitance is an important parasitic impacting analog speed and digital delay. However, the collector cannot be independently scaled due to limitations with current mesa technology [1]. We describe here a novel InP HBT technology in a simple, manufacturable process employing only Fe and selective Si implants to enable scaling of C_{cb}, whose brief results were in [2]. The Fe is implanted first (Fig. 1a) which is followed by a patterned, deep Si implant at 350 KeV/4x10^{14} ions-cm^{-2}. Fe, a mid-gap acceptor in InP, fully compensates Si donors when the Fe concentration exceeds that of Si. A buried and isolated N^{++} subcollector layer is thus formed (Fig. 1b). An N^{+} pedestal linking to the buried subcollector is then formed by a second selective Si implant (Fig. 1c). This eliminates the parasitic capacitance associated with the base access pad. The Fe implanted region is the extrinsic portion of the device, where the capacitance is reduced. The intrinsic collector base junction is defined by the pedestal and this allows the base contact width to be larger, enabling high device yield.

RBS measurements indicate a fully crystalline substrate following anneal of the implants, prior to growth (Fig. 2). The active InP DHBT layers are grown by MBE. TLM measurements show the base $\boldsymbol{r}_s$ » 600 Ω and $\boldsymbol{r}_c \cong 18$ Ω·µm^2. The implanted subcollector sheet resistance $\boldsymbol{r}_s = 21$ Ω. The DC current gain $\boldsymbol{b}$ is ≈ 35 and BV_{CEO} is ≈ 6.9V (Fig. 3). Figure 4 compares the variation of C_{cb} versus V_{cb} between the implanted pedestal-subcollector DHBT and a triple mesa DHBT, with similar 120 nm collectors [2]. C_{cb} is reduced by ~30% with the pedestal. These DHBTs exhibit a maximum 352 GHz f_t and 403 GHz f_{max} (fig. 5). SIMS and capacitance-voltage data indicate that the Fe implant compensates the subcollector implant to a depth of 130 nm, increasing the extrinsic collector depletion depth and reducing the capacitance per unit area.

This fully implanted pedestal-subcollector DHBT technology provide the following enhancements: elimination of C_{cb} in the base interconnect pad area, compensation of donor-like states at the growth interface, a single, fully crystalline MBE growth and increased wafer planarity. In this first demonstration of this process, the f_t and f_{max} are the highest reported for DHBTs with implanted collectors.

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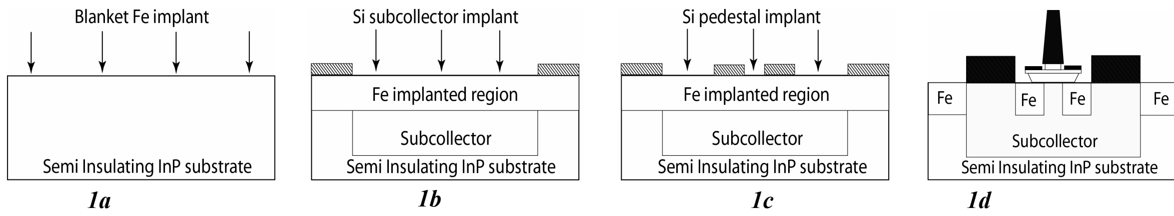

Figure 1: Implanted pedestal-subcollectorDHBT process

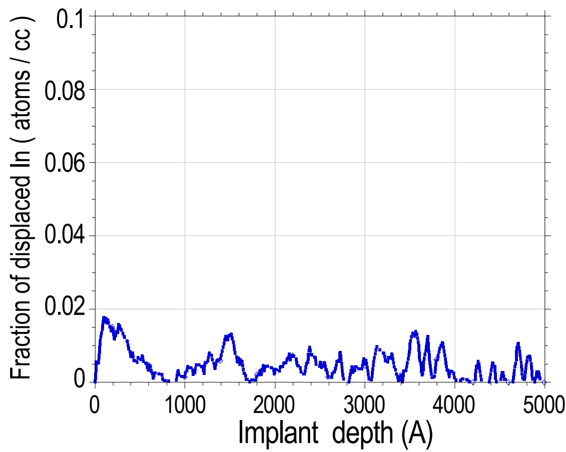

Figure 2: RBS measurements of defects after anneal of the implants. The sample is fully recovered if the fraction of displaced In is < 2%

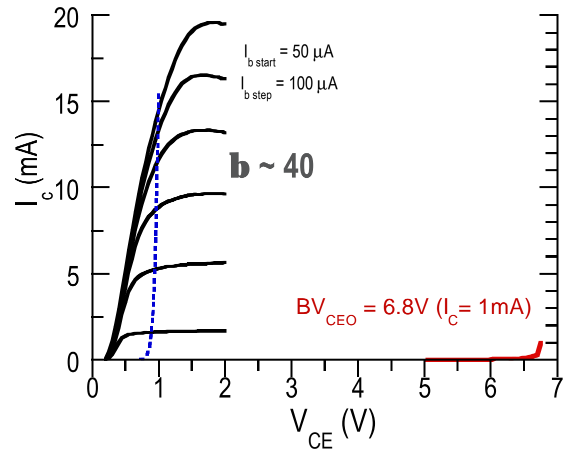

Figure 3: DC device characteristics of the implanted pedestal- subcollector DHBT

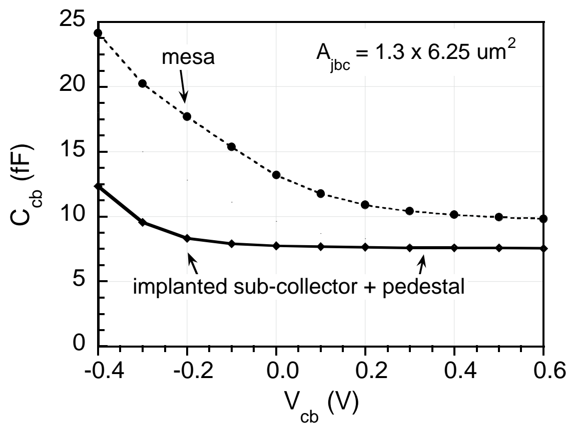

Figure 4: Capacitance voltage characteristics

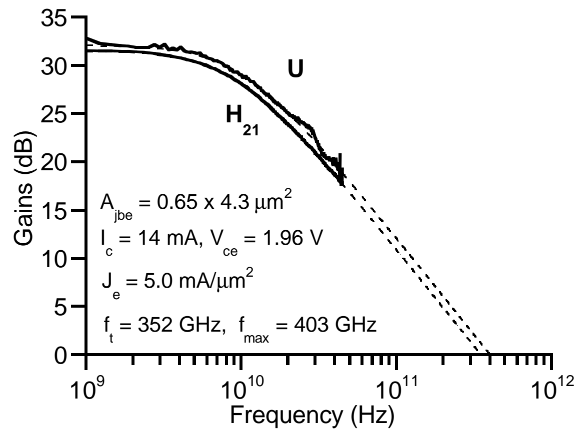

Figure 5: Measured microwave gains of the implanted pedestal- subcollector DHBT