

**Corrado Carta**

**High Speed Electronics Group  
Electrical and Computer  
Engineering Department**

**email : [carta@ece.ucsb.edu](mailto:carta@ece.ucsb.edu)**

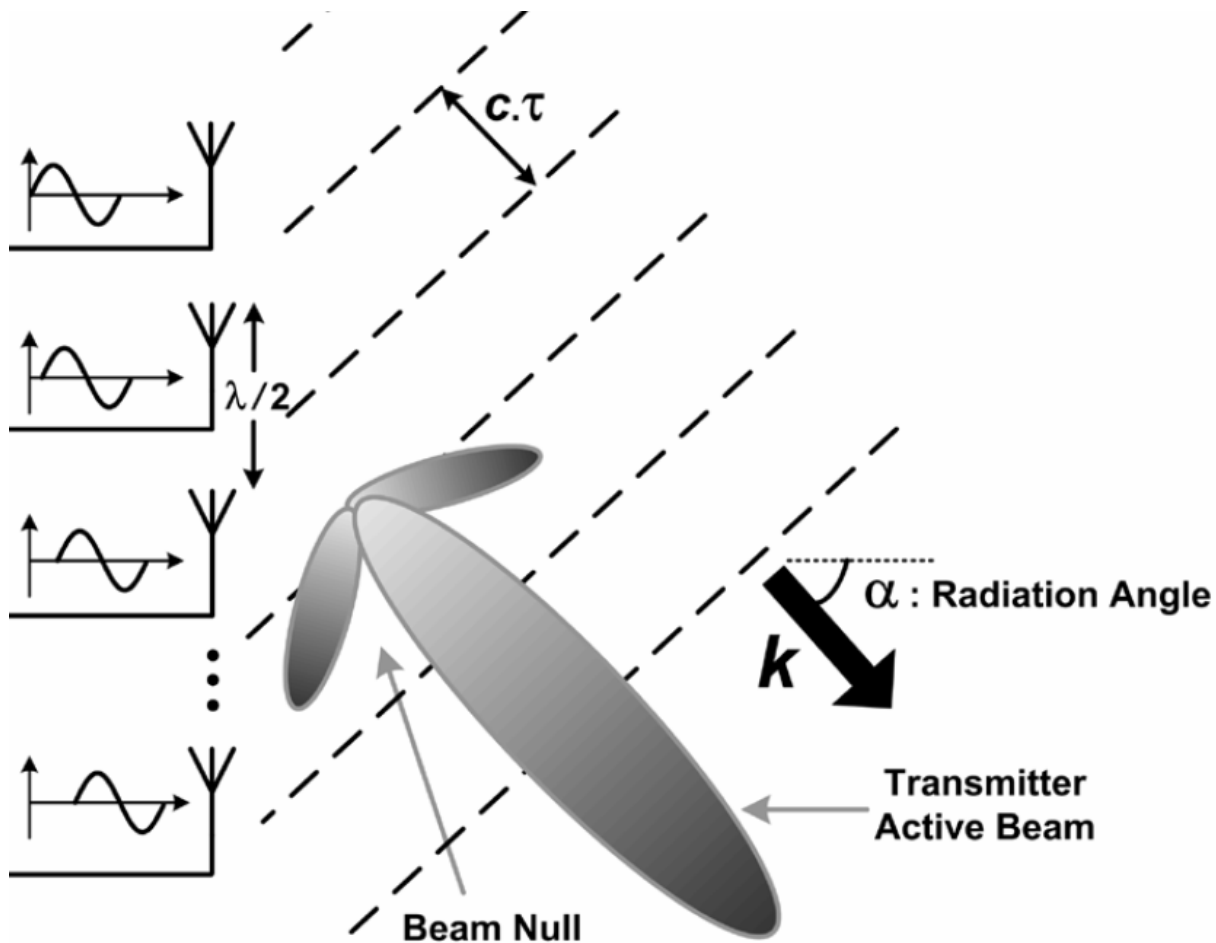


**University of California  
at Santa Barbara (UCSB)**

**A Mixed-Signal  
Row/Column  
Architecture for  
Very Large  
Monolithic  
mm-Wave  
Phased Arrays**

**Corrado Carta,  
Munkyo Seo and  
Mark Rodwell**

# Phased Array: basic (intuitive) concept



Picture from Hajimiri et al., © IEEE

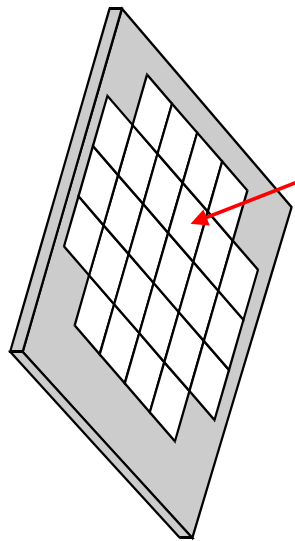
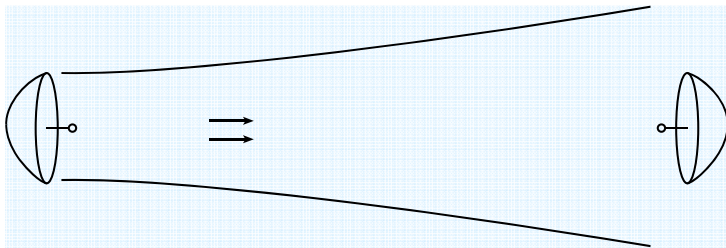
- Think of a transmitter “generating” a plane wave traveling on a arbitrary direction, by producing the proper phases
- Same applies to the receiver (as for any antenna)
- A bi-dimensional array can steer azimuth and altitude just by electronically adjusting the phases

# Overview

- mm-Wave communications and phased arrays
- Need for high directivity calls for large arrays
- Innovative row/column architecture
- IF bus design
- LO bus design
- Active microwave mixer design (ECL compatibility)
- Conclusion

# mm-Wave communications

$$\left( \frac{P_{received}}{P_{transmitted}} \right) = \left( \frac{D_t D_r}{16\pi^2} \right) \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}$$

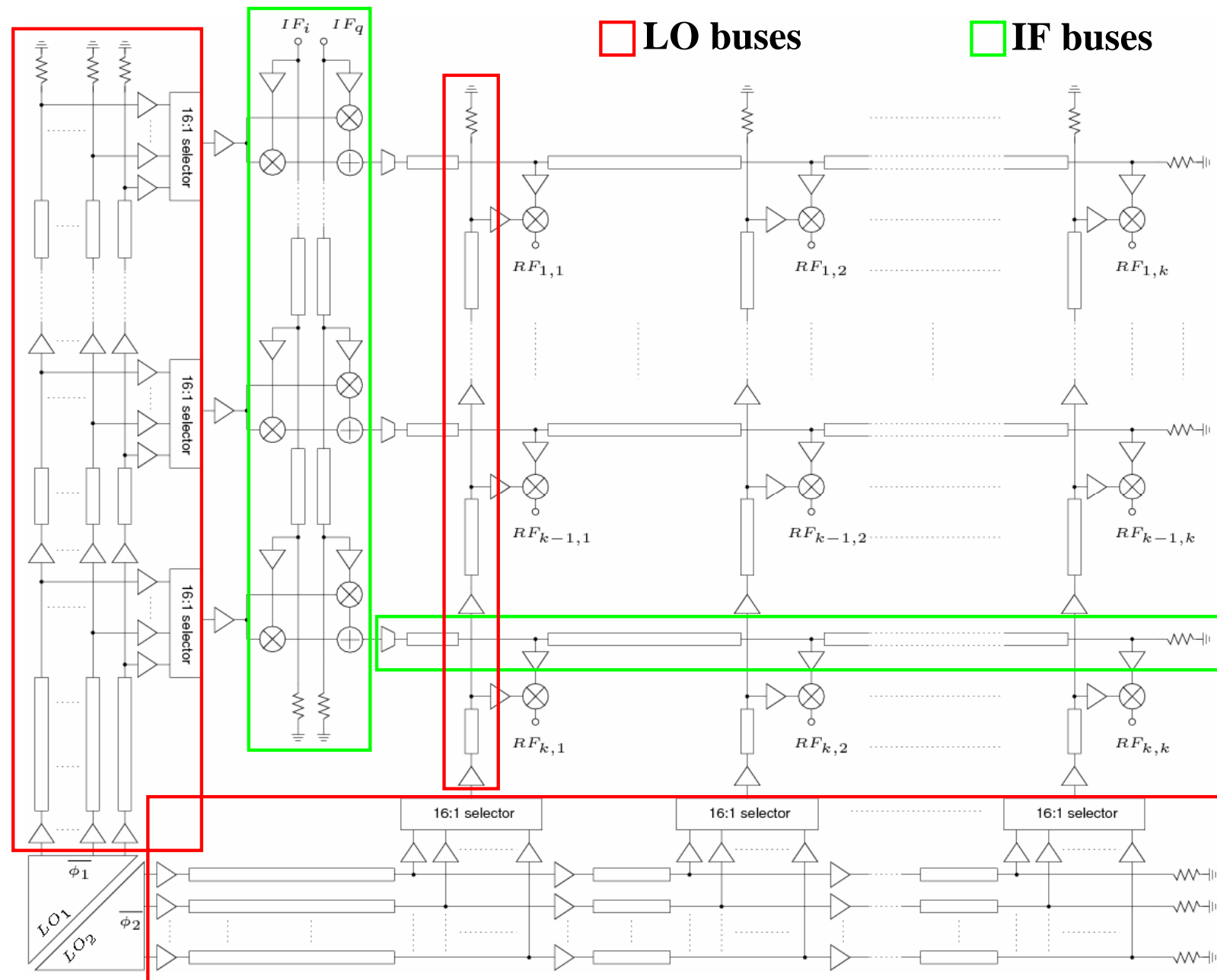


$$\text{Area} = (\lambda/2)^2$$

- mm-wave enables 1-10Gbps wireless communications
- Small  $\lambda$  and atmospheric attenuation imply short distance
- Directional antennas (large  $D_x$ ) can increase link range
- mm-wave systems must use phased arrays
- High directivity requires electronic beam steering...
- ...but small element area demands monolithic integration
- *How to make a large monolithic phased array?*

# Mixed-signal row-column architecture

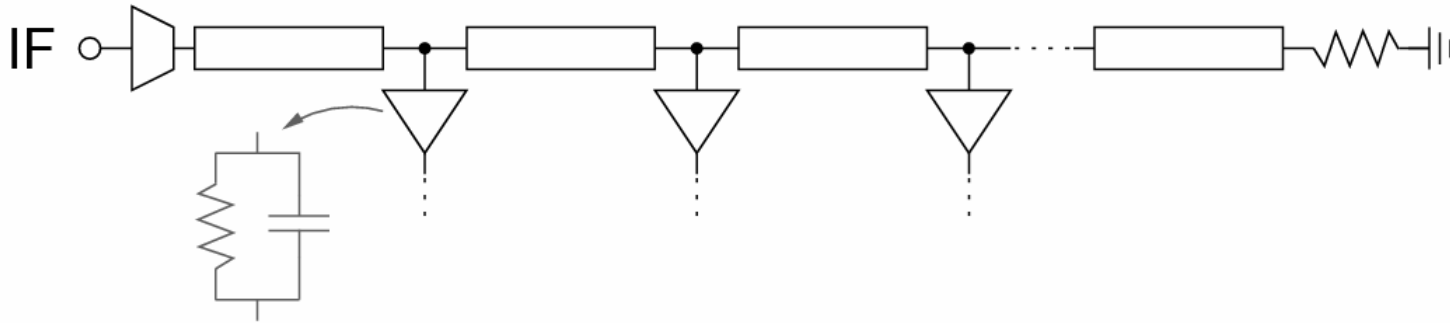
  LO buses
   IF buses



- 16 discrete phases of two LOs
- Phase on each element is set by row first, then by column
- This is enough to select any direction above array
- Element number scalable ( $N^{1/2}$  complexity)
- Limit in IF and LO buses (frequency and max N)

# IF bus: design

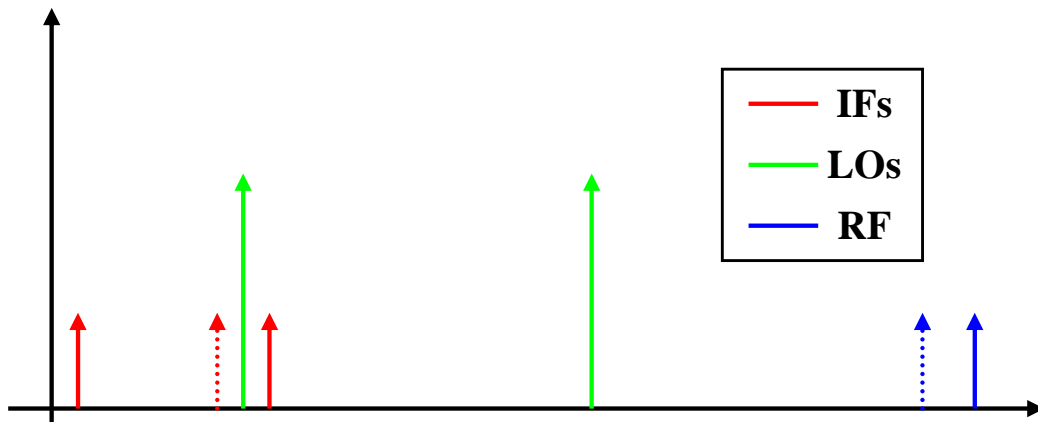
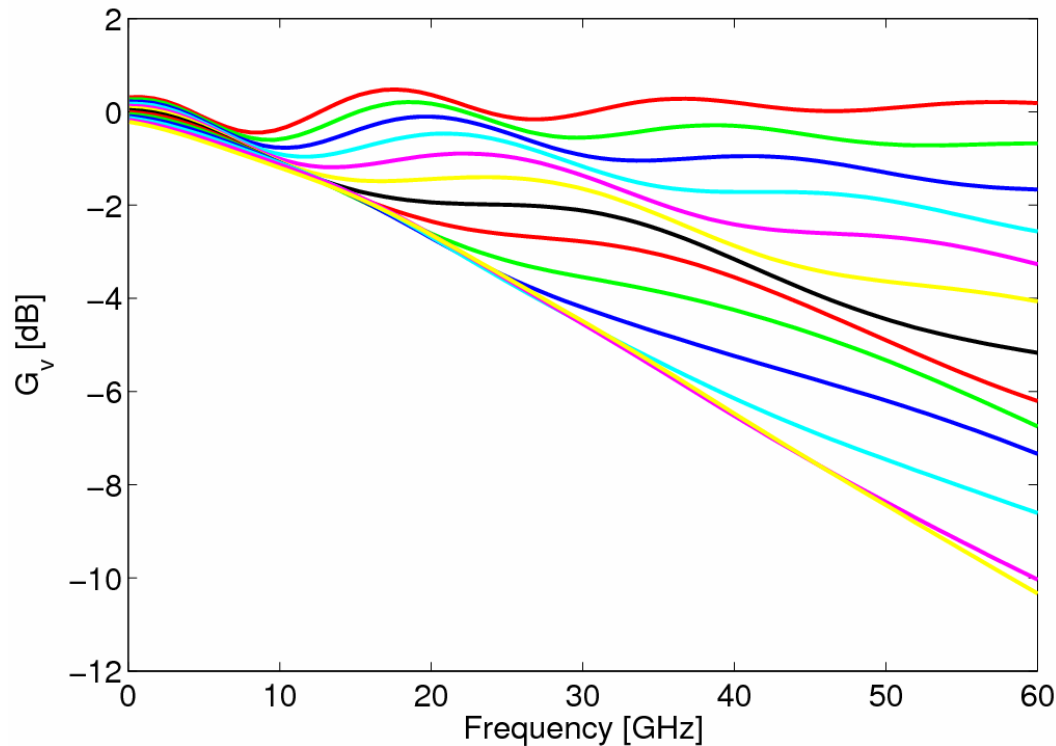
IF bus: synthetic T-line ~ TWA



$$Z_o = \sqrt{\frac{L_L}{C_S + C_L}}$$

- IF signal is analog and must travel on a linear bus
- Exploit long connections and periodic load to make a synthetic t-line:
  - Linear
  - 50Ω input
  - Well controlled amplitudes and phases at tap points
- It is entirely passive

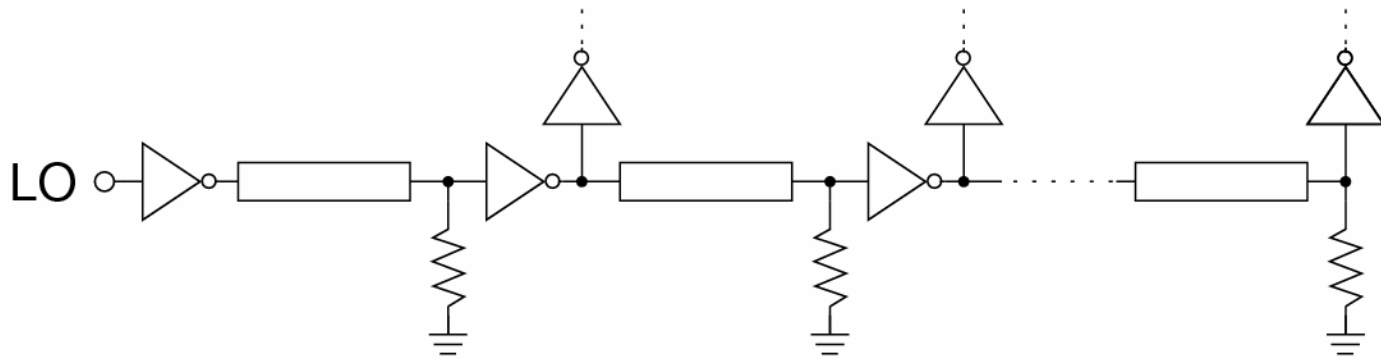
# IF bus: simulation



- Simulation of a 14 tap point t-line, on a standard  $0.18\mu\text{m}$  RF BiCMOS technology
- Application and frequency plan sets max frequency and N
- Max RF might be quite higher than max IF, e.g.:
  - $\text{LO}_1=15\text{GHz}$
  - $N=12$  @  $\text{IF}_2=15\text{GHz}$
  - $\text{IF}_1 < 1\text{GHz}$  (e.g. 1Gbps QAM)
  - $\text{LO}_2=\text{RF} - \text{LO}_1$
- Much higher than max IF!!!

# LO bus: design

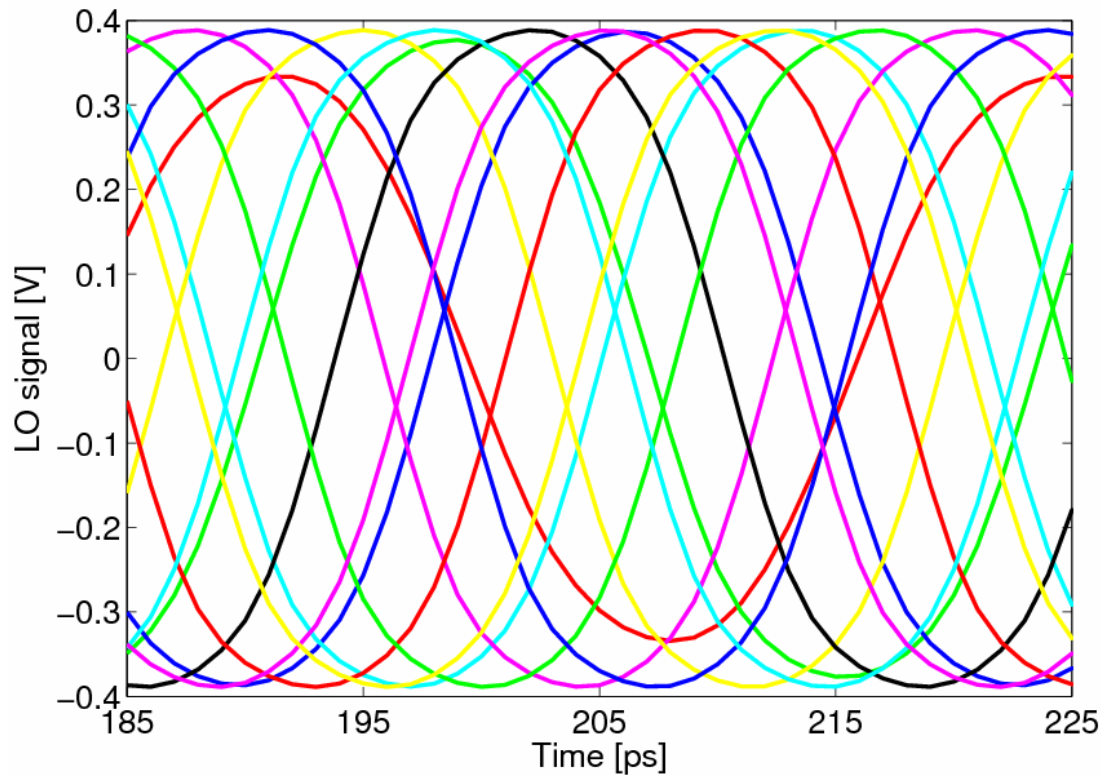
## LO bus: digital buffers



- LO signals need no linearity, just phase and frequency information
- Exploit robustness of digital design
- ECL (fastest logic) inverters drive terminated t-lines
- Periodic loads are selector inputs or other inverters driving column lines
- Full compatibility (DC levels) with Mixers and selectors, both feasible as ECL gates

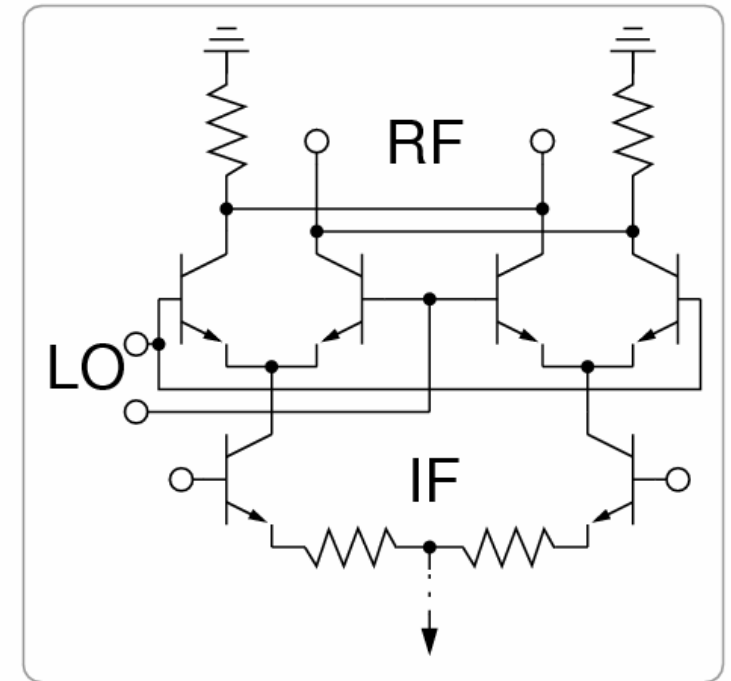
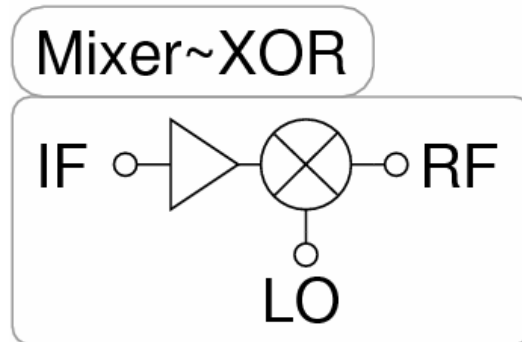


# LO bus: simulation



- Simulation of a 12 tap-point 30GHz LO bus (same tech. as before)
- Signal levels are steady and adequately recovered – no sensible sign of degradation
- Limit is only in max frequency of operation of ECL inverters
- Virtually no limit in number of tap-points (just the power consumption...)
- It is **much faster** than the analog IF bus

# Mixer design (time buffer)



- ECL compatibility is very important
- It's robust and avoids bulky capacitors
- An ECL XOR gate is “almost” a mixer...
- ...just resistive degeneration needed to linearize the IF-to-RF conversion gain (analog path)

# Conclusion

- We propose a scalable and robust architecture for the integration of large phased arrays in Silicon technologies
- Row/Column phase distribution minimizes wiring complexity and reduces system design to IF and LO bus design
- Analog design is necessary for IF bus, but it is limited in size or max frequency very early. Analog systems are hardly scalable!
- Digital design allows faster operation and larger sizes: mixed-signal design of phased arrays enables better performances (max frequency and directivity)