Wideband DHBTs Using a Graded Carbon-Doped InGaAs Base

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Abstract—We report an InP/InGaAs/InP double heterojunction bipolar transistor (DHBT), fabricated using a mesa structure, exhibiting 282 GHz f_{τ} and 400 GHz $f_{\rm max}$. The DHBT employs a 30 nm InGaAs base with carbon doping graded from $8\cdot 10^{19}/{\rm cm}^3$ to $5\cdot 10^{19}/{\rm cm}^3$, an InP collector, and an InGaAs/InAlAs base–collector superlattice grade, with a total 217 nm collector depletion layer thickness. The low base sheet (580 Ω) and contact ($<10~\Omega$ - μ m 2) resistivities are in part responsible for the high $f_{\rm max}$ observed.

Index Terms—Carbon doping, heterojunction bipolar transistor, palladium.

I. INTRODUCTION

EVELOPMENT of analog and digital ICs operating at 80–160 GHz clock frequencies requires improved transistor performance [1]. Based upon analyzes of emitter-coupled logic (ECL) gate delay [1], [2], target specifications for 160 Gb/s optical transmission include >3 V breakdown, >450 GHz f_{τ} and $f_{\rm max}$, maximum emitter current density $J_{e,{\rm max}} > 7$ mA/ μ m² at $V_{\rm cb} = 0$ V, and low base–collector capacitance charging time ($C_{\rm cb}/I_c < 0.3$ ps/V). Improved transistor bandwidth can be obtained by simultaneously reducing the collector depletion thickness, the collector and emitter junction widths, the emitter contact resistivity, and, in mesa HBTs, the base sheet and contact resistivity [2].

Here we report InP/InGaAs/InP mesa DHBTs with 282 GHz f_{τ} and 400 GHz $f_{\rm max}$. High $f_{\rm max}$ is obtained through low base sheet and Ohmic contact resistivities, obtained in part through high carbon base doping and Pd/Ti/Pt/Au Ohmic contact metal. Prior to this work, the highest $f_{\rm max}$ reported for a mesa DHBT is 300 GHz using an InP/GaAsSb/InP epitaxial design [3], while 462 GHz $f_{\rm max}$ was reported for a transferred substrate DHBT [4].

II. DESIGN

To achieve high f_{τ} and $f_{\rm max}$, the base resistance $R_{\rm bb}$ and base–collector capacitance $C_{\rm cb}$ must be simultaneously minimized. In a mesa HBT, $C_{\rm cb}$ is reduced through use of

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narrow base contacts on either side of the emitter stripe. $R_{\rm bb}$ has components arising from base current spreading under the emitter stripe, the emitter–base gap, and the base contacts. The first two components are reduced through low base sheet resistance, hence high base doping, narrow emitter junctions, and a small spacing between the emitter junction and the base contact [2], [12]. The third component—the base contact resistance—is minimized by using very high base doping.

The top portion of the base, upon which contacts are placed, is carbon-doped at $N_A=8\cdot 10^{19}~{\rm cm}^{-3}$. At such high doping β is limited by Auger recombination, varying as $\beta\propto (N_AT_B)^{-2}\propto \rho_{s,{\rm base}}^{-2}$. A thin $T_B=30$ nm base was therefore selected. A built-in drift field was introduced to further reduce base transit time and increase β . At $N_A\approx 8\cdot 10^{19}~{\rm cm}^{-3}$, doping is degenerate, the variation in Fermi energy with doping is strong, and large drift fields are induced with moderate changes in doping. Assuming Fermi–Dirac statistics and including bandgap narrowing [7-7], a linear grading of N_A from $8\cdot 10^{19}$ to $5\cdot 10^{19}~{\rm cm}^{-3}$ produces a 49 meV potential drop and a $16.5~{\rm kV/cm}$ drift field. Assuming $D_{n,b}=43~{\rm cm}^2/{\rm sec}$ average diffusivity and $4\cdot 10^7~{\rm cm/s}$ exit velocity, the calculated base transit time is reduced from 0.18 to $0.10~{\rm ps}$.

The base-collector conduction band discontinuity ΔE_C between InGaAs and InP must be suppressed by grading. The base-collector grade employs a 20 nm InGaAs setback layer $(T_{\rm setback})$ and a 24 nm InAlAs/InGaAs chirped superlattice $(T_{\rm grade})$, grading from InGaAs to In_{0.26}Ga_{0.26}Al_{0.48}As, producing zero conduction band energy offset at the interface. The superlattice period is small, 1.5 nm, reducing miniband effects and their associated degradation in transit time and β [8]. The Si pulse-doped layer (3 nm thickness, $N_{d,\mathrm{pulse}}=3\cdot 10^{18}~\mathrm{cm^{-3}}$) has sheet doping $T_{\mathrm{pulse}}N_{d,\mathrm{pulse}}=\varepsilon\Delta E_c/q^2T_{\mathrm{grade}}$ selected [8] to suppress the change in the conduction band quasifield at the interface with the InP collector. The conduction-band potential drop across the setback layer is $\Delta \phi_{\rm setback} \cong (V_{\rm cb} + \phi_{\rm bi}) T_{\rm setback} / T_c +$ $qN_{d,\text{pulse}}T_{\text{pulse}}T_{\text{setback}}/\varepsilon + (qN_d - J/v)T_cT_{\text{setback}}/2\varepsilon.$ The second term, of magnitude 0.25 V, is present due to the change in the conduction band quasifield at the interface between the grade and the setback layers. The setback-layer potential drop provides electrons incident on the grade with kinetic energy $q\Delta\phi_{\rm setback}$, reducing the likelihood of current blocking. Only for $V_{\rm cb} > 5.0~{
m V}$ does $q\Delta\phi_{\rm setback}$ exceed $E_{\rm gap,\ InGaAs}m_h^*/(m_h^*-m_e^*)$, the energy required for impact ionization in the InGaAs setback layer. Since InP-collector DHBTs generally exhibit breakdown $V_{\rm br, ceo} \cong (25 \, \text{to} \, 35 \, \text{V}/\mu\text{m}) \times T_c$ [12], impact ionization in the

setback layer should have minimal effect on $V_{\rm br,ceo}$. Similarly, breakdown by impact ionization will occur in the InP collector at a smaller $V_{\rm cb}$ than is required for breakdown in the grade.

 $C_{\rm cb}/I_c$ is a key parameter determining logic speed. To ensure full depletion, hence low $C_{\rm cb}$ at a minimum voltage $V_{\rm cb,min}$, the maximum collector doping must satisfy $[V_{\rm cb,min}+\phi_{\rm bi}]=qN_dT_c^2/2\varepsilon+qN_{d,\rm pulse}T_{\rm pulse}T_{\rm setback}/\varepsilon$. Targeting nearly complete depletion at $V_{\rm cb}=0$ V, $N_d=2\cdot 10^{16}$ cm $^{-3}$ was selected. The collector field reverses (Kirk effect) at the setback-grade interface at an emitter current density $J_{\rm max}$ satisfying

$$[V_{\rm cb} + \phi_{\rm bi}] = (J_{\rm max} A_e / A_{c,\rm eff} v_{\rm electron} - q N_d) T_c^2 / 2\varepsilon + q N_{d,\rm pulse} T_{\rm pulse} T_{\rm setback} / \varepsilon$$
 (1)

where $(A_{c,\text{eff}}/A_e)$ is the degree of current spreading in the collector [9].

III. GROWTH AND FABRICATION

The samples were MBE grown on 3" SI-InP wafers. The structure features a 25 nm thick carbon doped base and an InP emitter. The collector is composed of a 20 nm InGaAs setback layer and a 24 nm InAlAs/InGaAs chirped superlattice grade on top of 170 nm InP. The subcollector has a thin layer of In-GaAs on top of InP to reduce thermal resistance. Base contacts extend 1 μ m on each side of the 8 μ m long emitters. The devices are made using selective wet etching. Wet etching of the emitter semiconductor creates an 80 nm undercut space between the base contacts and the emitter junction. After PdTiPdAu base contact deposition [10], a 1 \times 2 μ m TiPdAu plug is deposited on the end of the base contact with a height equal to that of emitter metallization. The emitter and collector contacts are TiPdAu. The emitter and base contacts are annealed at 300 °C and the collector contact at 270 °C. HBTs are planarized and passivated with polyimide.

IV. RESULTS

The specific emitter resistivity is 25 Ω - μ m², the collector sheet and contact resistances are 7 Ω and $\sim 50 \Omega - \mu m^2$, while the base contact resistance is too low to measure reliably, below 10 Ω - μ m². From the 580 Ω base sheet resistance, a 55 cm²/V·s average hole mobility is determined. The HBTs have $\beta = 22-28$ (Fig. 1), while $V_{\rm BR,CEO}=7.5$ V. On-wafer RF measurements were performed on devices with on-wafer transmission-line extended reference planes and line-reflect-line calibration. An HBT with a 0.54 μ m emitter junction width and a 2.7 μ m width base–collector junction (Fig. 2) exhibited a 282 GHz $f_{ au}$ and 400 GHz $f_{\rm max}$ at $J_e=2.3~{\rm mA}/\mu{\rm m}^2$ and $V_{\rm CE}=1.5~{\rm V}$. Figs. 3 and 4 show the variation of f_{τ} and $C_{\rm cb}$ with bias on a similar HBT; the collector is not fully depleted until $V_{\rm cb} = V_{\rm ce} - V_{\rm be} \cong 0.35$ V, indicating collector doping above the design value. From Fig. 3 and (1), $(A_{c,\text{eff}}v_{\text{electron}}/A_e) = (4.0 \pm 0.7) \cdot 10^7$ cm/s is determined. This high value suggests that the collector grade does not reduce the electron velocity. High f_{τ} and record f_{max} are obtained due to low base transit time and low base contact resistivity together with a nonblocking base-collector grade. Reducing N_d to obtain a fully depleted collector at $V_{\rm cb}=0$

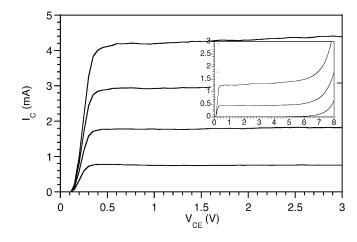


Fig. 1. Common-emitter characteristics for an HBT with a 0.44 μ m \times 7.7 μ m emitter junction area. The base current steps are 50 μ A.

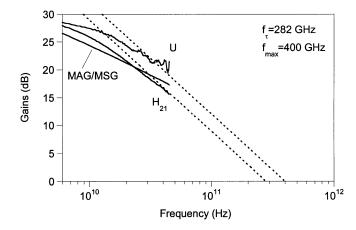


Fig. 2. Measured RF gains of an HBT with a 0.54 μ m \times 7.7 μ m emitter, and a 2.7 μ m width base–collector junction, measured at $I_C=15$ mA and $V_{\rm CE}=1.7$ V

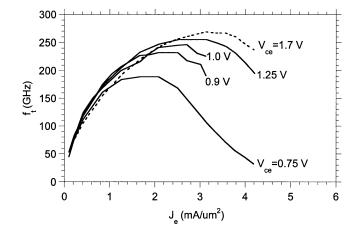


Fig. 3. Variation of f_{τ} versus I_C and $V_{\rm CE}$, of an HBT with a 0.54 μ m \times 7.7 μ m emitter, and a 2.7 μ m width base–collector junction.

V would result (1) in a $\sim 0.7 \text{ mA}/\mu\text{m}^2$ reduction in the Kirk threshold at all applied $V_{\rm cb}$.

V. SUMMARY

InP/InGaAs/InP DHBTs with heavy carbon base doping can obtain high current densities and high bandwidths even in

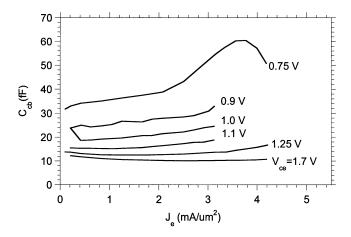


Fig. 4. Variation of $C_{\rm cb}$ versus I_C and $V_{\rm CE}$. Note that $V_{\rm be}=0.85$ –0.90 V over the same bias range.

conventional mesa structures. Unlike earlier wideband mesa DHBTs that employed either MOCVD-grown InP/GaAsSb/InP or InP/InGaAs/InGaAsP/InP layer structures, the DHBTs reported here employ both InGaAs base layers and InAlAs/InGaAs base–collector superlattice grades, and are grown by MBE. High f_{τ} and record $f_{\rm max}$ are obtained due to low base transit time and low base contact resistivity together with a nonblocking base–collector grade. The results demonstrate performance obtainable from aggressive scaling of InP HBTs in a mesa process; large-scale IC development will require process flows having improved yield at large integration scales.

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