Student Paper

InP Heterojunction Bipolar Transistor with a Selectively Implanted Collector Pedestal

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To increase the logic speed of heterojunction bipolar transistors (HBT's), the base-collector junction capacitance (C_{bc}) should be reduced as much as possible. In a mesa structured HBT, a large portion of C_{bc} originates from the extrinsic base-collector region under the base contact. To reduce this extrinsic C_{bc}, we report an HBT structure with a collector pedestal under the HBT's intrinsic region by using selective ion implantation and MBE regrowth (Fig.1), the first such structure reported in III-V HBT's. It is designed so that the depleted collector thickness in HBT's extrinsic region is much larger than the depleted collector thickness in HBT's intrinsic region, and therefore the extrinsic base-collector capacitance can be significantly reduced. Although C_{bc} can also be reduced by forming a narrow N+ subcollector stripe lying under the emitter[1], such structures can have large collector access resistance Rc arising from long, narrow N+ layer. For emitter lengths greater than ~2μm, the resulting collector resistance then limits the maximum HBT current density under low-voltage (logic) operation. The collector pedestal structure, however, does not significantly increase collector access resistance relative to a standard mesa structure, and is consequently the approach most widely employed in Si/SiGe technology. Here we report first results on pedestal collector implants in III-V technology.

The fabrication process of the device is shown in Fig.2. The subcollector template was grown by MBE and consisted of a 2000Å n+ InP subcollector layer, a 50 Å InGaAs n+ subcollector contact layer, a 2000Å undoped InP collector pedestal layer, and a 300Å undoped InGaAs sacrificial cap layer. After the growth of this template, tungsten alignment marks were formed and a PECVD SiN implant mask was defined. The implant window was 0.2μm wider than the emitter. ^{28}Si was then implanted at 110KeV with a dose of $6\lambda 10^{13}$cm^{-2} at 200πC and annealed at 750πC for 10 sec. Annealing at 750πC or above resulted in almost 100% of implant activation(Fig.3). The InGaAs sacrificial layer was then removed and the collector drift layer, base, and emitter were regrown by MBE (Table1). The base was 400Å thick while the collector depletion region above the collector pedestal was 1000Å thick. Outside the pedestal, the depletion layer was 3000Å thick. Triple-mesa HBT's were then fabricated using optical lithography and wet etching. Fig.4 shows the SEM image of a device after mesa isolation.

Fig. 5(a) and 5(b) show the common emitter and Gummel characteristics of a 0.5λ6 μm^2 device, measured from 0-500kA/cm^2 current density. $V_{CE,SAT}$ is less than 0.8V at 500kA/cm^2 current density and ß=25. The Gummel characteristics were measured with 0.3V collector-base reverse bias, so that the base-collector junction leakage I_{cbo} could be observed. Fig. 5(b) indicates I_{cbo}~200 nA for a device with 60μm^2 base-collector junction area. This leakage current is acceptably low for most circuit applications. The microwave 2-port parameters were characterized. The cut-off frequencies f_T=170GHz and f_{max}=127GHz were measured at J=500kA/cm^2 and V_{CE}=1.4V. The f_{max} of the present HBT's is lower than expected due to the incomplete depletion of the extrinsic collector region. This has resulted from unexpectedly large charge density at the regrown interface. To correct this, device fabrication runs in progress use a compensating p- doping in the unimplanted portion of the collector pedestal epitaxial layer.

In conclusion, a new InP HBT structure with a selectively implanted collector pedestal has been demonstrated. The present results exhibit low I_{cbo} and hence high junction quality can be obtained in a collector pedestal process incorporating regrowth. The 500kA/cm^2 current density at a low 0.7V V_{CE}

indicates that the pedestal structure maintains low collector access resistance. RF performance of the present transistor was found to be limited by the charge at the regrowth interface. Improved performance is expected through reducing the regrowth interfacial charge and through the compensating p- doping in the collector pedestal layer.

References:

[1] M. Sokolich, M.Y. Chen, D.H. Chow, Y. Royter, S. Thomas III, C.H. Fields, D.A. Hitko, B. Shi, M. Montes, S.S. Bui, Y.K. Boegeman, A. Arthur, J. Duvall, R. Martinez, T. Hussain, R.D. Rajavel, K. Elliot, and J.D. Thompson, to be presented at 25th IEEE GaAsIC Symposium.

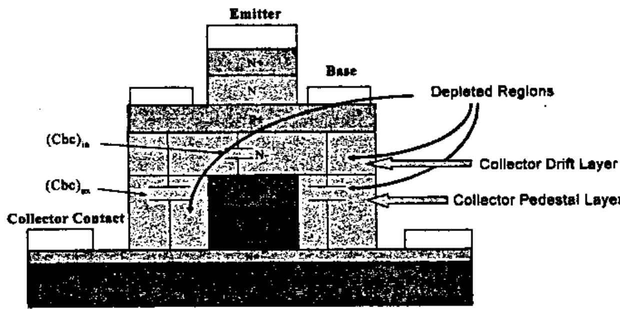

Fig. 1 Schematic cross-section of the HBT with selectively implanted collector pedestal.

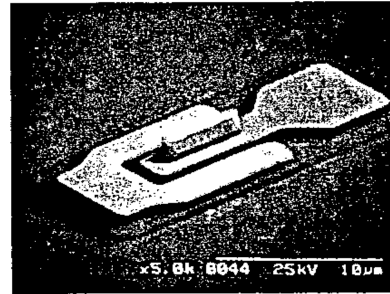

Fig. 4 Fabricated 0.5μm λ 6 μm HBT before planarization.

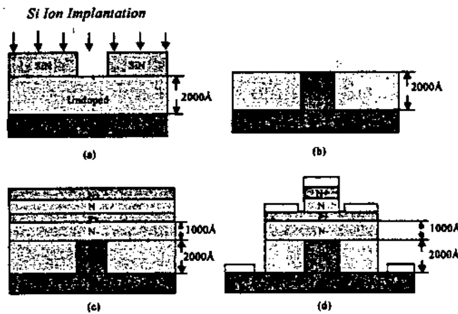

Fig. 2 Fabrication steps: (a) implant window definition and Si ion implant, (b) implant mask removal and HT annealing, (c) HBT structure regrowth, (d) triple-mesa HBT fabrication.

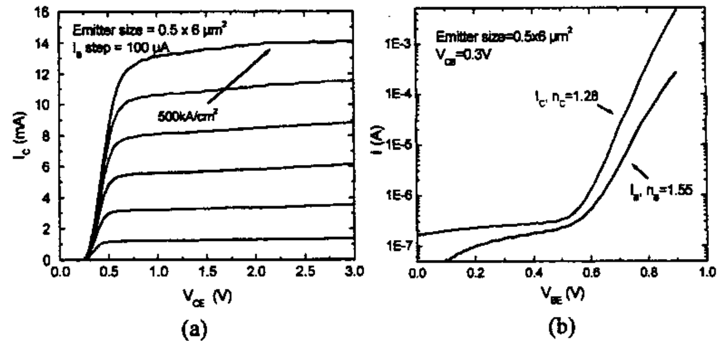

Fig. 4 (a) Common Emitter characteristics and (b)Gummel plots of an HBT with 0.5λ6 μm² emitter size.

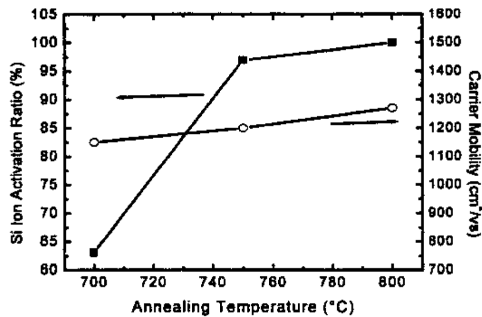

Fig. 3 The dependence of implanted dopants' activation efficiency and carrier mobility on the annealing temperature.

Layer	Material	Thickness (Å)	Doping (cm^{-3})
Cap	InGaAs	400	Si:$2x10^{19}$
Emitter	InP	800	Si: $2x10^{19}$
	InP	100	Si: $8x10^{17}$
	InP	300	Si: $3x10^{17}$
Base	InGaAs	400	C: $6x10^{19}$
Collector	InGaAs	200	Si: $3.6x10^{16}$
	InGaAs/InAlAs	240	Si: $3.6x10^{16}$
	InP	30	Si: $3x10^{18}$
	InP	530	Si: $3.6x10^{16}$

Table 1 Parameters of the HBT epitaxial layers grown above the collector pedestal layer.