InGaAs/InP DHBTs WITH A 75nm COLLECTOR, 20nm BASE DEMONSTRATING 544 GHz f_τ, BV_{CEO} = 3.2V, and BV_{CBO} = 3.4V

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***Abstract*— We report InP/InGaAs/InP double heterojunction bipolar transistors (DHBT) fabricated using a conventional mesa structure. The devices employ a 20 nm highly doped InGaAs base and a 75 nm InP collector containing an InGaAs/InAlAs superlattice grade. These devices exhibit a maximum f_τ = 544 GHz with a 347 GHz f_{max}, which is the highest f_τ for an InP DHBT, and highest f_τ at a 75 nm collector thickness for any HBT. The devices have been scaled vertically for reduced base and collector electron transit times, and the base-collector mesa has been kept narrow to minimize the capacitance C_{cb} associated with thinner collectors. The current gain $\beta \approx 50$, BV_{CEO} = 3.2 V, BV_{CBO} = 3.4 V, and the devices operate up to 24 mW/μm^2 (failing at J_e = 12 mA/μm^2, V_{ce} = 2.0 V, $\Delta T_{failure} \approx 348$ K).**

***Index Terms*—InP heterojunction bipolar transistor**

I. Introduction

Amongst InP HBT manufacturers, efforts are now under way both to obtain high circuit yield at $> 10{,}000$ devices per IC and to simultaneously extend device and circuit bandwidth. Geometric scaling theory suggests [1] that a $\sqrt{2}:1$ increase in device and logic bandwidth can be obtained by concurrent lithographic scaling–reducing the width of the emitter W_e and collector W_c by $\sim$ 2:1, epitaxial scaling–reducing the collector thickness $T_c \sim \sqrt{2}:1$, increasing current density J_e by $\sim$ 2:1, and reducing the base thickness T_b by somewhat more than $\sqrt[4]{2}:1$, and contact resistivity scaling–reducing the emitter $\rho_{c,e}$ and base $\rho_{c,b}$ Ohmic contact resistivities by $\sim$ 2:1. Lithographic scaling to 0.15-0.25 μm W_e has been demonstrated [2], [3], albeit on devices with epitaxial dimensions comparable to HBTs having 0.5 μm W_e [4]. Similarly, the effects of epitaxial scaling on breakdown, current density, transit time, and thermal resistance can be measured on HBTs with relatively large emitter dimensions, as was done here.

Prior to this work, the highest f_τ reported for an InP DHBT was 491 GHz with an f_{max} of 415 GHz, having a 30 nm base and 100 nm collector [5], where BV_{CEO} is approximately 3.2-3.4 V. Here we report InGaAs/InP DHBTs having a 20 nm base and 75 nm collector, exhibiting a peak 544 GHz f_τ, a record for a DHBT, simultaneous with 347 GHz f_{max}, BV_{CEO} = 3.2 V, and BV_{CBO} = 3.4 V. In comparison, other reported InP HBTs having a 75 nm collector include an InGaAs-collector InP-SHBT having 509 GHz f_τ and 219 GHz f_{max} [6], and a Type-II InP-DHBT (GaAsSb base, InP collector) demonstrating 358 GHz f_τ and 194 GHz f_{max} [7].

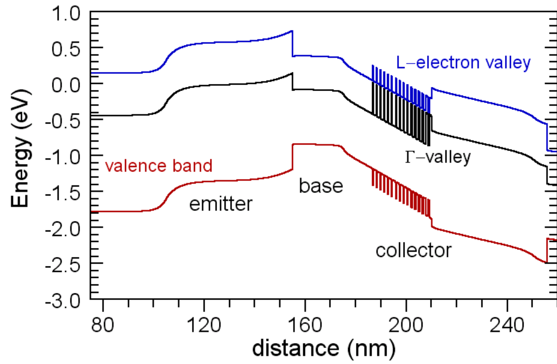
TABLE I
InP DHBT epitaxial layer structure

Thickness,nm	Material	Doping, cm^{-3}	Description
10	$In_{0.85}Ga_{0.15}As$	$5 \cdot 10^{19}$: Si	Emitter cap
15	$In_xGa_{1-x}As$	$4 \cdot 10^{19}$: Si	Cap grading
10	$In_{0.53}Ga_{0.47}As$	$4 \cdot 10^{19}$: Si	Emitter cap
70	InP	$3 \cdot 10^{19}$: Si	Emitter cap
10	InP	$1 \cdot 10^{18}$: Si	Emitter
40	InP	$8 \cdot 10^{17}$: Si	Emitter
20	InGaAs	8 - $6 \cdot 10^{19}$: C	Base
10	InGaAs	$3 \cdot 10^{16}$: Si	Setback
24	InGaAs/InAlAs	$3 \cdot 10^{16}$: Si	B-C grade
3	InP	$3 \cdot 10^{18}$: Si	δ - doping
38	InP	$3 \cdot 10^{16}$: Si	Collector
5	InP	$1.5 \cdot 10^{19}$: Si	Subcollector
7.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$: Si	Subcollector
300	InP	$2 \cdot 10^{19}$: Si	Subcollector
—	InP	Semi-insulating	Substrate

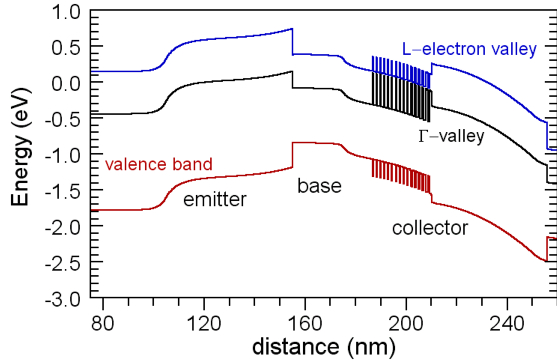
II. Design

The full Type-I InP DHBT layer structure is shown in Table I, and the associated band diagrams [8] of the device at an applied bias of V_{be} = 0.95 V, V_{cb} = 0.0 V for J_e = 0, J_{Kirk}, and 1.5$\cdot J_{Kirk}$ are shown in figures 1a-c.

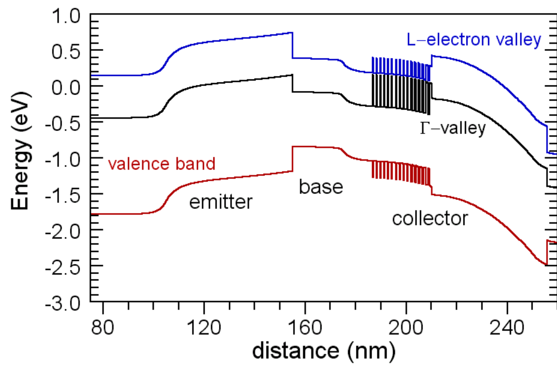
A base thickness of 20 nm was selected having a doping grade of 8-6$\cdot 10^{19}$ cm^{-3}:C that in-turn produces $\sim$ 27 meV of conduction band grading to establish a quasi-field across the base. As this was a first attempt to realize InP DHBTs with such a thin base from our laboratory, increased conduction band grading was considered too aggressive and



(a) V_{be} = 0.95 V, V_{cb} = 0.0 V, J_e = 0 mA



(b) V_{be} = 0.95V, V_{cb} = 0.0V, J_e = J_{Kirk} $\sim$ 10mA/μm^2



(c) V_{be} = 0.95 V, V_{cb} = 0.0 V, J_e $\sim$ 1.5 $\times$ J_{Kirk}

Fig. 1. Simulated band-diagram of the reported InP Type-I DHBT – 75 nm collector, 20 nm base.

not considered. At these doping levels employed across the base, a hole mobility $\mu_h \cong 55$ cm^2/V·sec was anticipated, and consistent with the extracted value from the measured base sheet resistance.

The InGaAs/InAlAs base-collector grade is unchanged compared to other UCSB InP DHBTs that have been reported [4], [5]. Because the collector thickness is only 75 nm, the InGaAs setback layer has been thinned to 10 nm so as to increase the amount of wider bandgap InP in the collector and consequently keep the HBT breakdown voltages BV$_{CEO}$ and BV$_{CBO}$ as large as possible with this grade design. From the Bandprof simulation of the HBT shown in figure 1b, electrons entering the collector from the base are accelerated by the $\sim$ 245 meV of potential difference across the conduction band of the setback layer before entering the grade–at a simulated current density of 10 mA/μm^2 and V_{cb} = 0.0 V. At higher simulated values of J_e, the potential difference across the setback changes little; however the field across the grade progressively reverses (fig. 1c) and significant reductions in the electron velocity in the collector is expected.

III. Growth and Fabrication

The epitaxial material was grown by IQE Inc. on a 3” semi-insulating InP wafer and the HBTs were fabricated in an all wet-etch, standard triple mesa process. The devices are passivated with and the wafer is planarized in benzo-cyclobutene (BCB) to minimize device leakage currents associated with semiconductor surface states. BCB also provides a low-ε_r spacer (ε_r = 2.7, T$_{BCB}$ = 1.6 μm) between the device interconnects and InP substrate to reduce spurious resonances in the RF measurements through substrate mode coupling.

IV. Measurements and Results

TLM measurements show the base ρ_s = 805 Ω and ρ_c = 16 $\Omega \cdot \mu$m^2, and collector ρ_s = 12.0 Ω and ρ_c = 4.7 $\Omega \cdot \mu$m^2. From RF parameter extraction, the emitter ρ_c = 8.6 $\Omega \cdot \mu$m^2. Figure 2 shows the common-emitter current-voltage and Gummel characteristics. The DHBTs have a current gain $\beta \cong 50$, and common-emitter and common-base breakdown voltages BV$_{CEO}$ = 3.2 V and BV$_{CBO}$ = 3.4 V (at I_c = 50 μA). The collector and base ideality factors are n_c = 1.15 and n_b = 1.47 respectively, and a low collector leakage current $I_{cbo} < 75$ pA (V_{cb} offset = 0.3 V) is observed. Thermal resistance θ_{JA} (K/mW) was measured and device junction temperature subsequently determined by the method of Liu [9] at different V_{cb} to vary the field distribution and thus power dissipation in the InGaAs setback, ternary grade, and InP layers of the collector, and determined to be θ_{JA} = 2.60 + 0.62·V_{cb} + 1.58·V_{cb}^2 (K/mW) when J_e = 5.8 mA/μm^2.

DC-45 GHz RF measurements were carried out after performing an off-wafer Line-Reflect-Reflect-Match

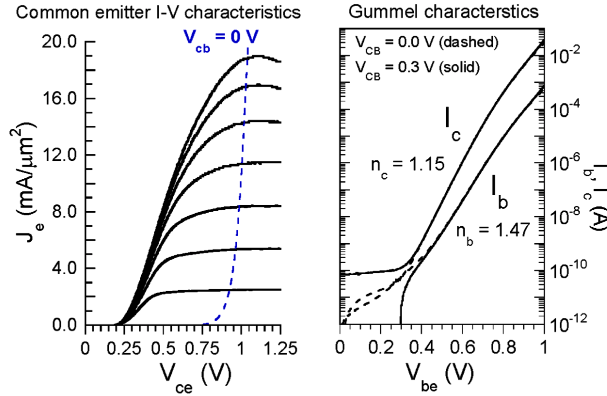


Fig. 2. Common-emitter I-V and Gummel characteristics. Emitter junction A_{je} = 0.65 × 4.3 μm^2, and $I_{b,step}$ = 175 μA

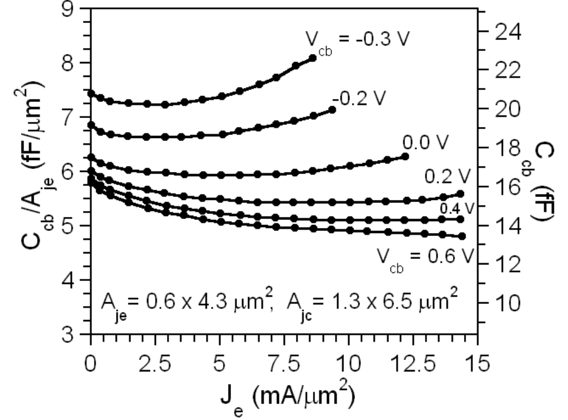
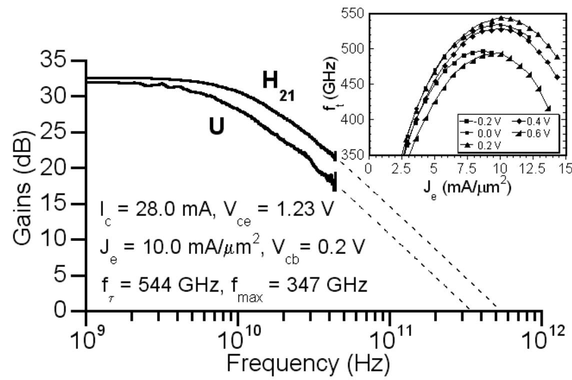
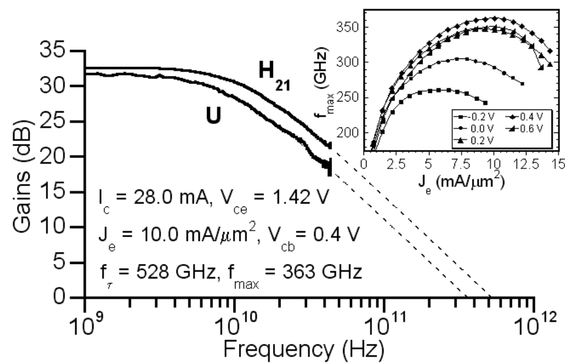


Fig. 4. Variation of C_{cb} with V_{cb} and J_e



(a) Variation of f_τ with J_e and V_{cb}



(b) Variation of f_{max} with J_e and V_{cb}

Fig. 3. Measured microwave gains H_{21} and Mason's unilateral gain U at a bias associated with peak f_τ (a) and peak f_{max} (b)

(LRRM) calibration on an Agilent 8510C network analyzer. An open and short circuit pad structure identical to the one used by the devices was measured after calibration in order to de-embed their associated parasitics from the S-parameter measurements. At a bias associated with peak f_τ, a maximum 544 GHz f_τ with a 347 GHz f_{max} (fig. 3a) was extrapolated through the method described in [4] at a bias of I_c = 28.0 mA and V_{ce} = 1.23 V (V_{cb} = 0.2 V, J_e = 10.0 mA/μm^2, C_{cb}/I_c = 0.54 ps/V, ΔT $\cong$ 102 K). Similarly, at a bias associated with peak f_{max}, a maximum 363 GHz f_{max} with a 528 GHz f_τ (fig. 3b) was demonstrated–I_c = 28.0 mA and V_{ce} = 1.42 V (V_{cb} = 0.4 V, J_e = 10.0 mA/μm^2, C_{cb}/I_c = 0.51 ps/V, ΔT $\cong$ 123 K). For both figures 3a and 3b, the variation of f_τ and f_{max} with operating current density J_e and base-collector potential V_{cb} are shown as inset plots. The device has a 0.65×4.3 μm^2 emitter junction area A_{je}, 1.4 μm base mesa width, and collector to emitter width ratio W_c/W_e = 2.15. Figure 4 shows the variation of C_{cb} versus operating J_e and V_{cb} for use in current mode logic (CML) circuit design.

High power density common-emitter I-V characteristics are shown in figure 5, where a number of HBTs having the same emitter dimension were stressed to failure. The devices are able to operate within 20% of BV_{CEO} while dissipating 18 mW/μm^2. Furthermore, at lesser collector-emitter voltages, the HBTs operate well to 20 mW/μm^2 showing few effects due to device self-heating.

V. Discussion

Amongst the InP HBT results that have been published over the past few years, there has not been a standard employed for which to determine the values of the common-emitter breakdown BV_{CEO} and common-base breakdown BV_{CBO} voltages. Collector currents ranging from 1 μA to 1 mA have been considered the appropriate value of I_c

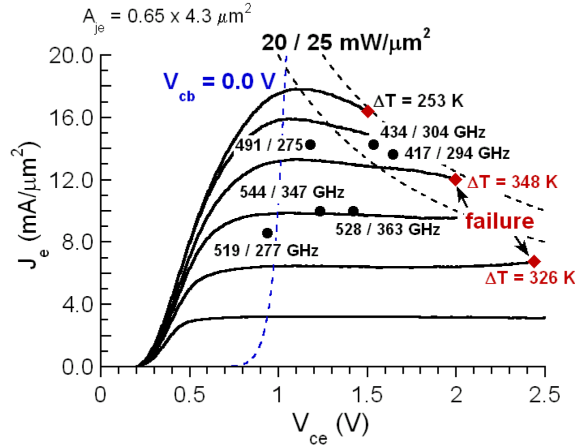
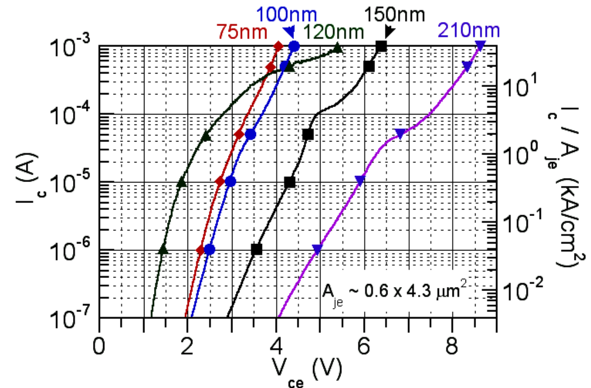
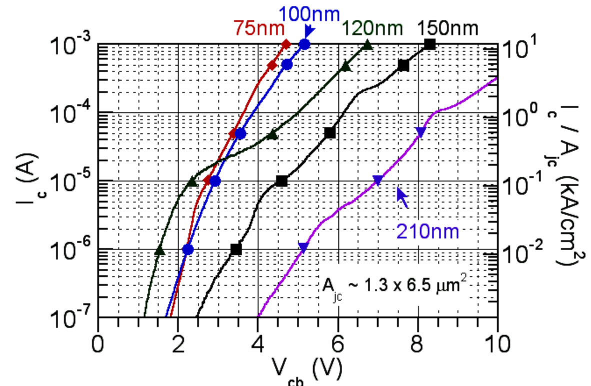


Fig. 5. High power density common-emitter characteristics. The value of f_τ/f_{max} various bias conditions are shown for the HBTs.



(a) Common-emitter breakdown current w/ varying V_{ce}



(b) Common-base breakdown current w/ varying V_{cb}

Fig. 6. Measurement of the collector breakdown current for both common-emitter (a) and common-base (b) configuration as the collector potential is increased to higher and higher values of I_c for UCSB InP DHBTs, where the collector thicknesses are listed.

from which to determine the breakdown voltage. Because of the differing I_c standard employed, a clear trend of how the breakdown voltages vary with collector thickness is not easily observed. Amongst the InP DHBT results from UCSB having different collector thicknesses, the same emitter and collector junctions have been chosen, using I_c = 50 μA, from which to determine BV$_{CEO}$ and BV$_{CBO}$. For the 75 nm collector result reported here, the authors have continued to use this standard. However, for those who would like to observe the breakdown trend of InP DHBT from our laboratory, figures 6a and 6b show the entire BV$_{CEO}$ and BV$_{CBO}$ measurement. With this, consider the following: for the 75 nm collector Type-II InP DHBT reported in [7], a BV$_{CEO}$ = 4.2 V is reported at an $I_c \sim$ 1.0 mA. In comparison for the Type-I InP DHBT reported here, a BV$_{CEO}$ = 3.2 V is reported at an I_c = 50 μA. These are considerably different values for device breakdown–however, if an I_c = 1.0 mA is considered for the HBTs here, BV$_{CEO}$ would be 4.1 V and BV$_{CBO}$ would increase from 3.4 V to 4.7 V. Consequently, the data provided in figures 6a and 6b at this time show that even down to collector thicknesses of 75 nm, Type-I InP DHBTS (ternary grading is required) are demonstrating breakdown voltages that are very similar to those of Type-II InP DHBTs (only InP is used for the collector.)

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