Indium Phosphide and Related Material Conference 2006

InGaAs / InP DHBTs with a 75nm collector, 20nm base demonstrating 544 GHz f_τ, BV_{CEO} = 3.2V, and BV_{CBO} = 3.4V

Zach Griffith and Mark J.W. Rodwell
Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA, 93106-9560, USA

Xiao-Ming Fang, Dmitri Loubychev, Ying Wu, Joel M. Fastenau, and Amy Liu
IQE Inc.
119 Bethlehem, PA 18015, USA

griffith@ece.ucsb.edu, 805-453-8011, 805-893-3262 fax

High speed HBTs: some standard figures of merit

Small signal current gain cut-off frequency (from H_{21})…

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{nk_B T}{qI_c}\left(C_{je} + C_{bc}\right) + \left(R_{ex} + R_c\right)C_{bc}$$

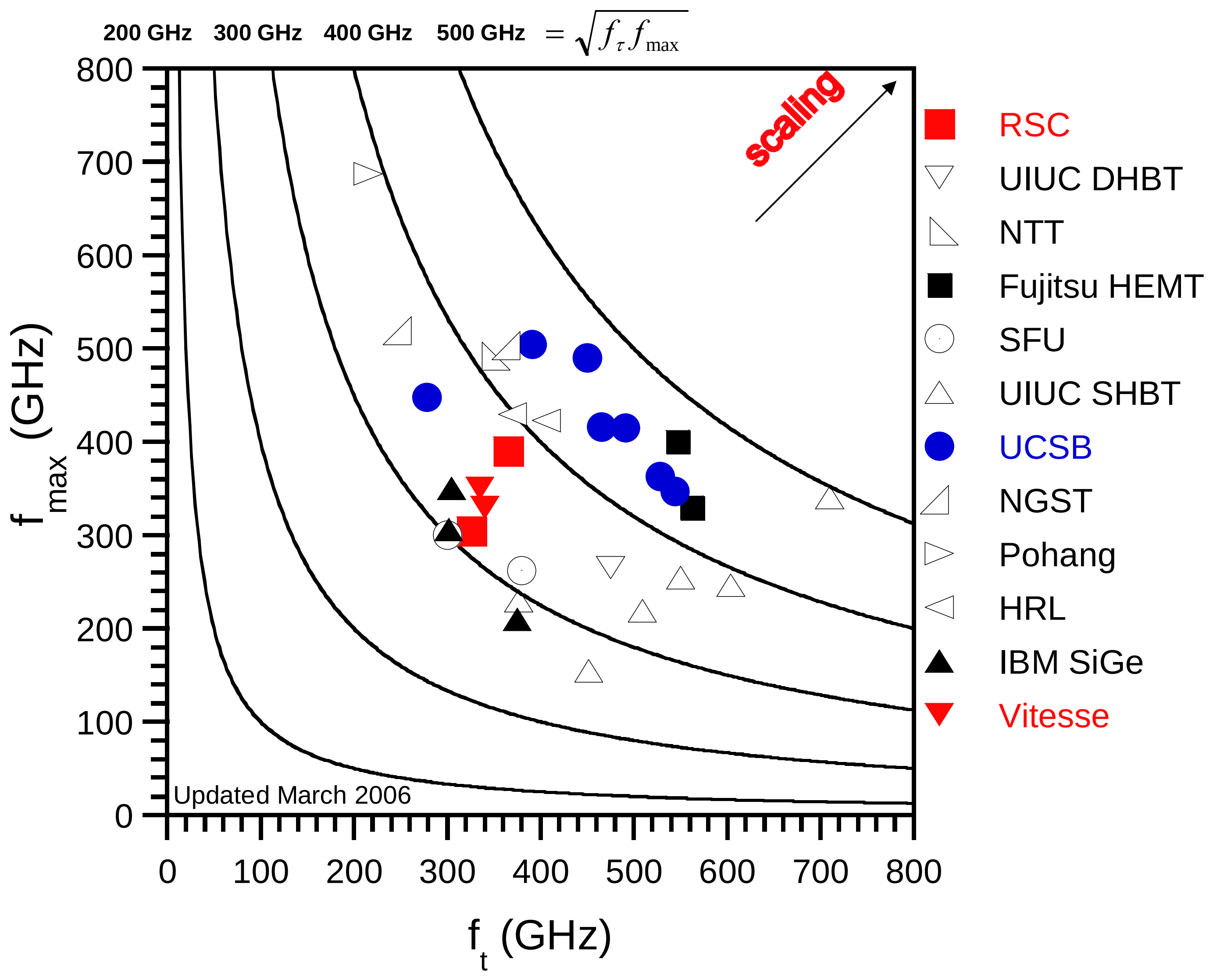
Power gain cut-off frequency (from U)…

$$f_{\max} \cong \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cb,i}}}$$

Collector capacitance charging time when switching…

$$\tau \propto \frac{C_{cb}}{I_c}\Delta V$$

Present Status of Fast Transistors



popular metrics :

f_τ or f_{max} alone

$(f_\tau + f_{max})/2$

$\sqrt{f_\tau f_{max}}$

$(1/f_\tau + 1/f_{max})^{-1}$

much better metrics :

power amplifiers :

PAE, associated gain, mW/μm

low noise amplifiers :

F_{min}, associated gain,

digital :

f_{clock}, hence

$(C_{cb}\Delta V / I_c)$,

$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

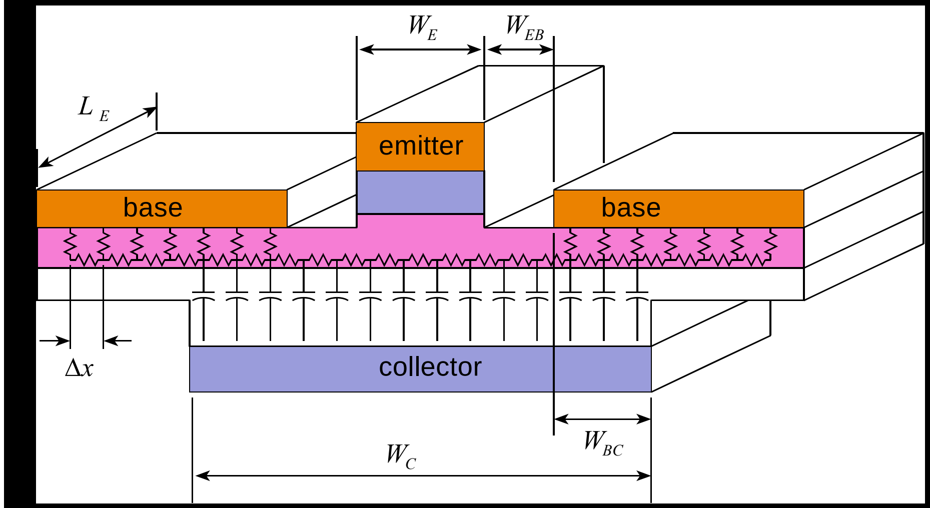
$(\tau_b + \tau_c)$

Bipolar Transistor Scaling Laws & Scaling Roadmaps

Scaling Laws:

design changes required to double transistor bandwidth

key device parameter	required change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter resistance per unit emitter area	decrease 4:1
current density	increase 4:1
base contact resistivity (if contacts lie above collector junction)	decrease 4:1
base contact resistivity (if contacts do not lie above collector junction)	unchanged



Technology Roadmap through 330 GHz digital clock rate

Parameter	scaling law	Gen. 2	Gen. 3	Gen. 4
MS-DFF speed	γ^1	158 GHz	230 GHz	330 GHz
Emitter Width	$1/\gamma^2$	500 nm	250 nm	125 nm
Resistivity	$1/\gamma^2$	15 Ω-μm²	7.5 Ω-μm²	5 Ω-μm²
Base Thickness	$1/\gamma^{1/2}$	300Å	250 Å	212 Å
Doping	γ^0	$7\ 10^{19}/\text{cm}^2$	$7\ 10^{19}/\text{cm}^2$	$7\ 10^{19}/\text{cm}^2$
Sheet resistance	$\gamma^{1/2}$	500 Ω	600 Ω	707 Ω
Contact ρ	$1/\gamma^{1/2}$	20 Ω-μm²	10 Ω-μm²	5 Ω-μm²
Collector Width	$1/\gamma^2$	1.1 μm	0.54 μm	0.27 μm
Thickness	$1/\gamma$	1500 Å	1060 Å	750 Å
Current Density	γ^2	5 mA/μm²	10 mA/μm²	20 mA/μm²
$A_{\text{collector}}/A_{\text{emitter}}$	γ^0	2.8	2.8	2.8
f_τ	γ^1	371 GHz	517 GHz	720 GHz
$f_{\max}$	γ^1	483 GHz	724 GHz	1.06 THz
I_E / L_E	γ^0	2.4 mA/μm	2.4 mA/μm	2.4 mA/μm
τ_f	$1/\gamma$	340 fs	250 fs	170 fs
C_{cb} / I_c	$1/\gamma$	440 fs/V	310 fs/V	220 fs/V
$C_{cb}\Delta V_{\text{logic}} / I_c$	$1/\gamma$	130 fs	94 fs	66 fs
$R_{bb} /(\Delta V_{\text{logic}} / I_c)$	γ^0	0.66	0.51	0.41
$C_{je}(\Delta V_{\text{logic}} / I_C)$	$1/\gamma^{3/2}$	350 fs	250 fs	180 fs
$R_{ex} /(\Delta V_{\text{logic}} / I_c)$	γ^0	0.24	0.24	0.24

key figures of merit for logic speed

Key scaling challenges

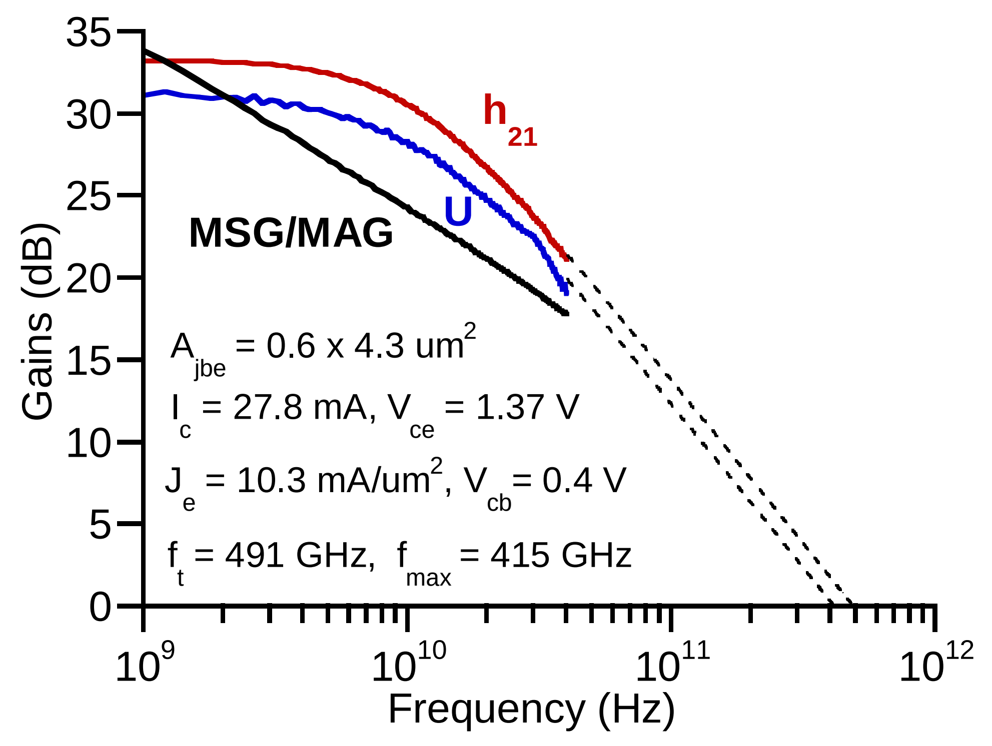
emitter & base contact resistivity

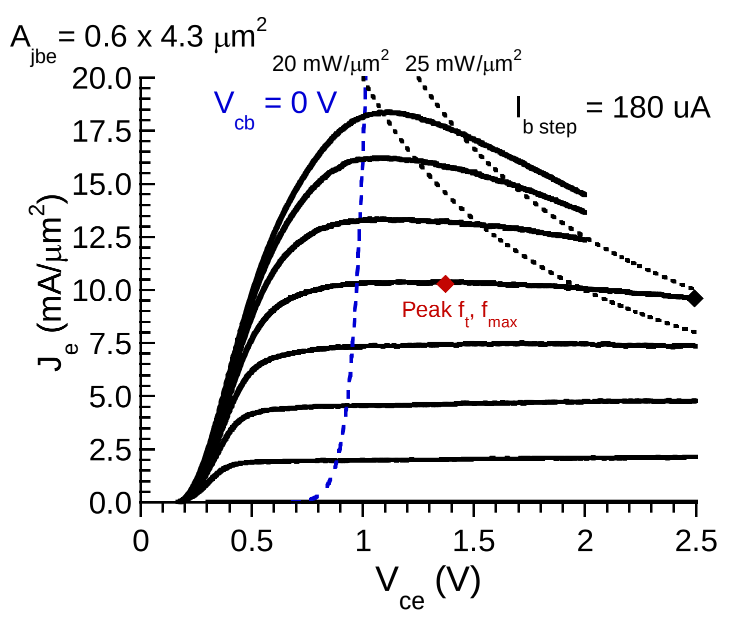
current density→ device heating

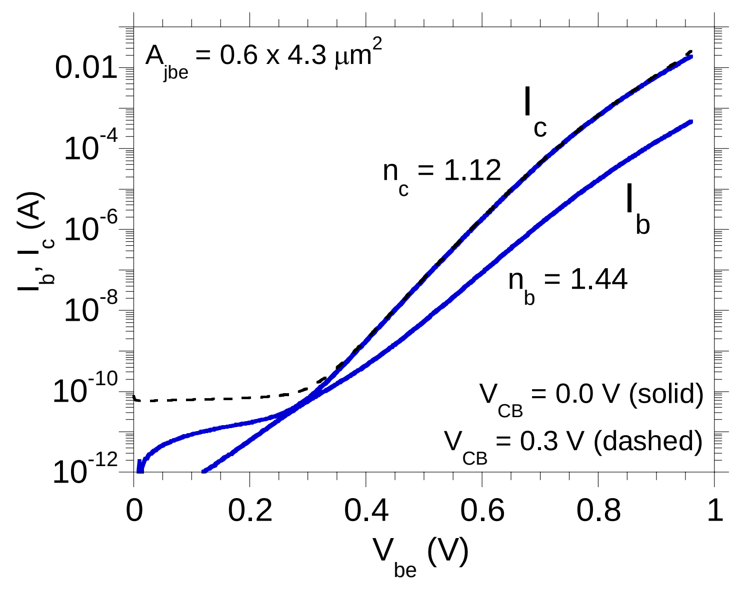
collector-base junction width scaling

& Yield !

DC, RF performance—100 nm collector, 30 nm base







Summary of device parameters—

Average β ≈ 40, $V_{BR,\ CEO}$ = 3.1 V

Emitter contact (from RF extraction), R_{cont} ≈ 7.8 Ω·µm^2

Base (from TLM) : R_{sheet} = 629 Ω/sq, R_{cont} = 6.2 Ω·µm^2

Collector (from TLM) : R_{sheet} = 12.9 Ω/sq, R_{cont} = 4.0 Ω·µm^2

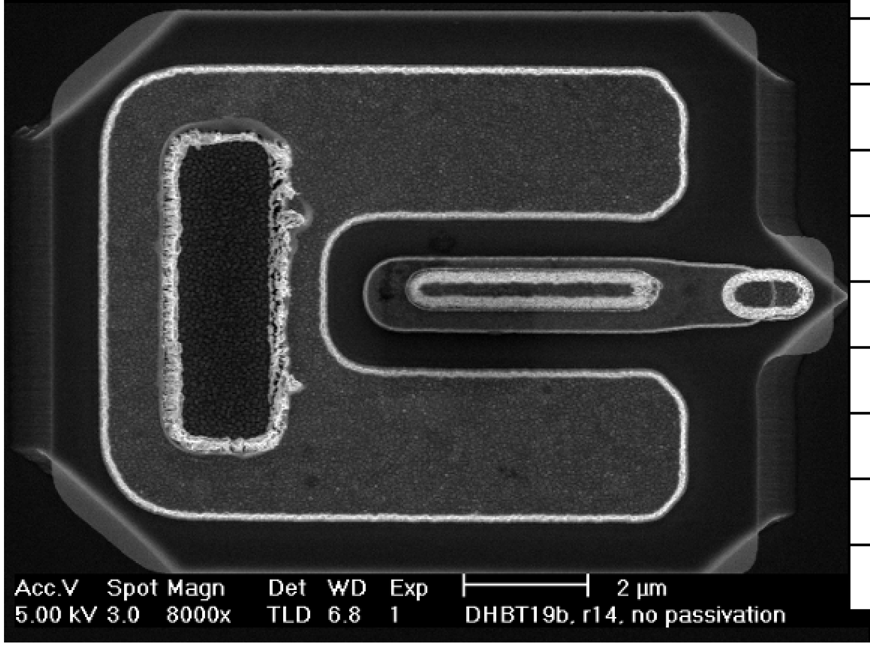
Z. Griffith, IPRM 2005, Glasgow, Scotland

Layer structure -- 75 nm collector DHBT

Objective:

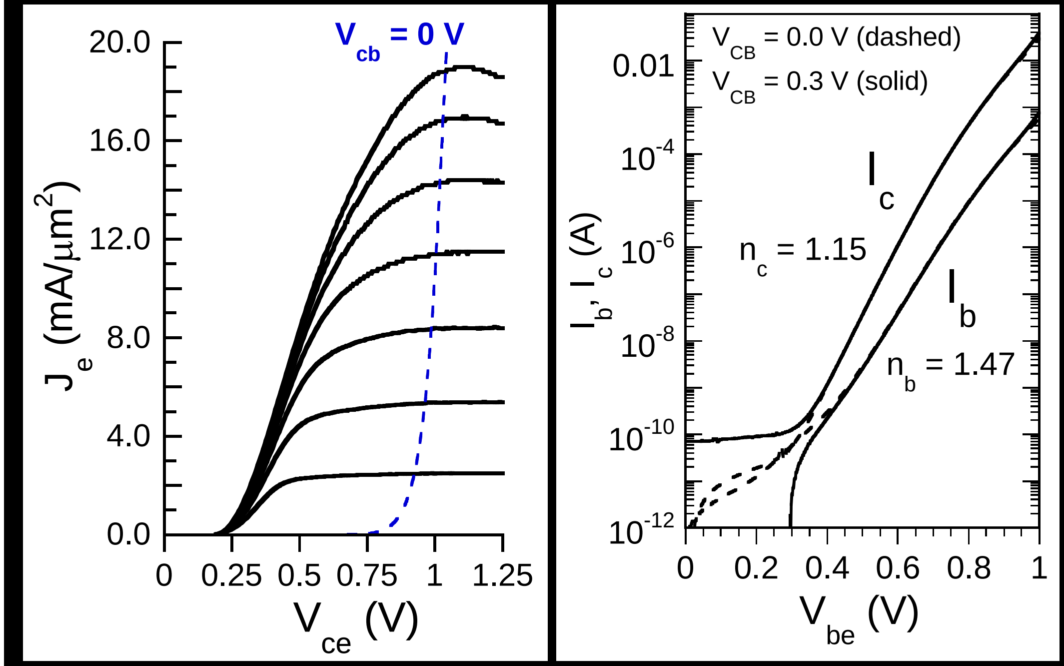
- Thin collector and base for decreased electron transit time
- High f_τ device with moderate f_{max}
- Investigate J_{max} before current blocking in the base-collector grade
- What is the HBT breakdown at this collector scaling node?

Thickness (nm)	Material	Doping cm^{-3}	Description
10	$In_{0.85}Ga_{0.15}As$	$5 \cdot 10^{19}$: Si	Emitter cap
15	$In_xGa_{1-x}As$	$> 4 \cdot 10^{19}$: Si	Emitter cap grading
10	$In_{0.53}Ga_{0.47}As$	$4 \cdot 10^{19}$: Si	Emitter
70	InP	$3 \cdot 10^{19}$: Si	Emitter
10	InP	$1 \cdot 10^{18}$: Si	Emitter
40	InP	$8 \cdot 10^{17}$: Si	Emitter
20	InGaAs	$8\text{-}6 \cdot 10^{19}$: C	Base
10	$In_{0.53}Ga_{0.47}$ As	$3 \cdot 10^{16}$: Si	Setback
24	InGaAs / InAlAs	$3 \cdot 10^{16}$: Si	B-C Grade
3	InP	$3 \cdot 10^{18}$: Si	Pulse doping
38	InP	$3 \cdot 10^{16}$: Si	Collector
5	InP	$1.5 \cdot 10^{19}$: Si	Sub Collector
7.5	$In_{0.53}Ga_{0.47}$ As	$2 \cdot 10^{19}$: Si	Sub Collector
300	InP	$2 \cdot 10^{19}$: Si	Sub Collector
Substrate	SI : InP		



InP DHBT: 600 nm lithography, 75 nm collector, 20 nm base

DC characteristics



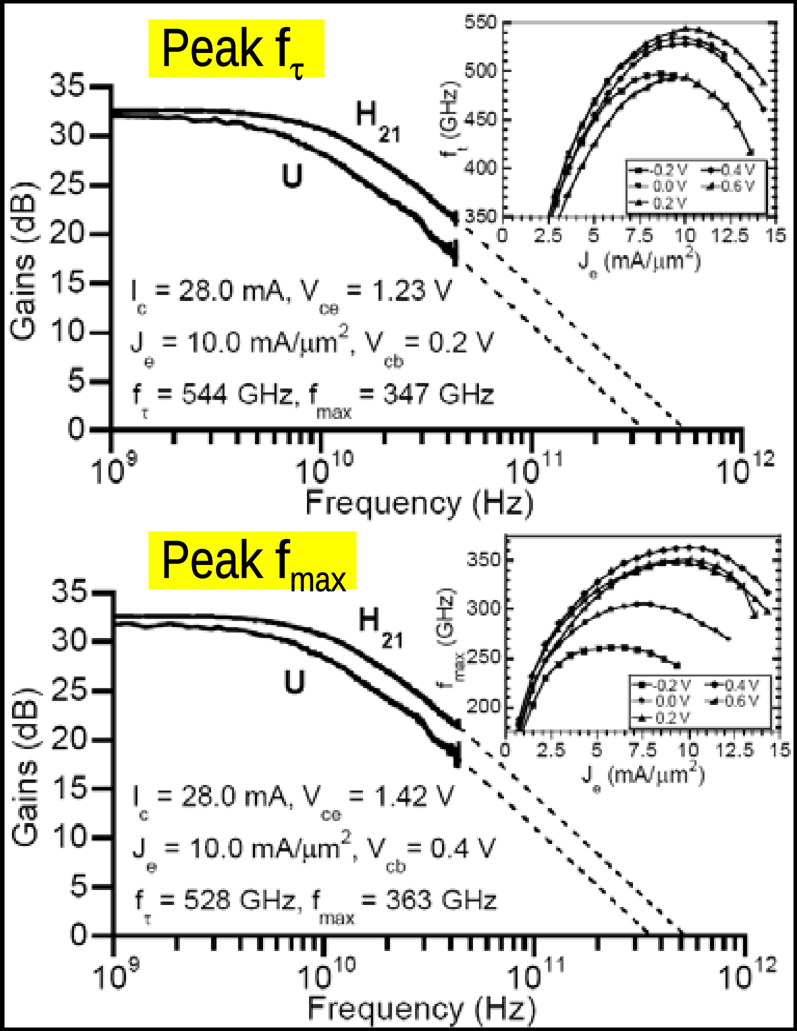
$A_{je} = 0.65 \times 4.3\ \mu m^2$, $I_{b,step} = 175\ \mu A$

Average $\beta \approx 50$, $BV_{CEO} = 3.2$ V, $BV_{CBO} = 3.4$ V ($I_c = 50\ \mu A$)

Emitter contact (from RF extraction), $R_{cont} \approx 8.6\ \Omega \cdot \mu m^2$

Base (from TLM) : $R_{sheet} = 805\ \Omega/sq$, $R_{cont} = 16\ \Omega \cdot \mu m^2$

Collector (from TLM) : $R_{sheet} = 12.0\ \Omega/sq$, $R_{cont} = 4.7\ \Omega \cdot \mu m^2$



RF characteristics

Experimental Measurement of Temperature Rise

$$\delta V_{BE}\Big|_{fixedIc} = \frac{dV_{BE}}{dT}\frac{dT}{dP}\frac{dP}{dV_{CE}}\delta V_{CE} = -\phi\cdot\theta_{JA}\cdot I_C\cdot\delta V_{CE}$$

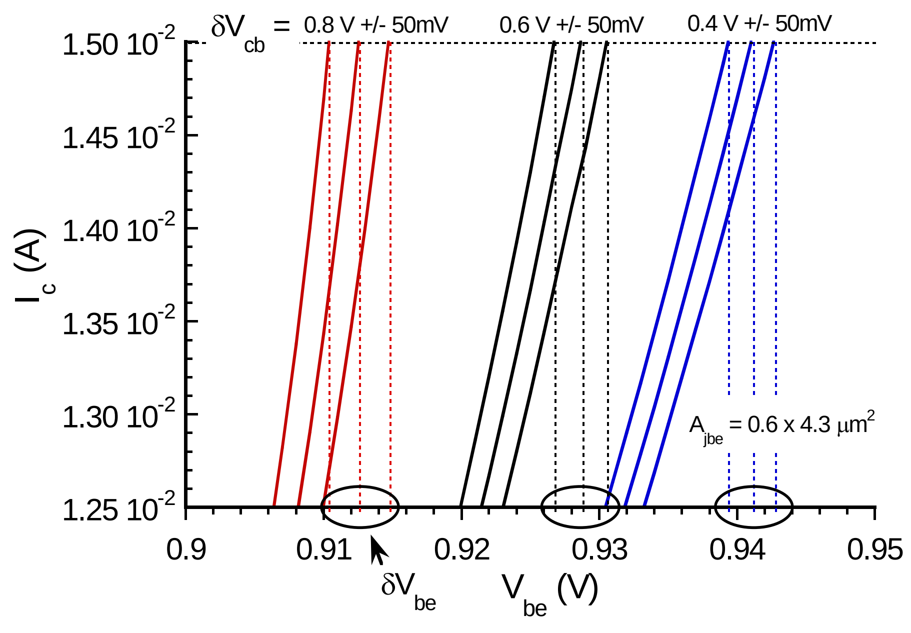
$$\Rightarrow \theta_{JA} = \frac{dV_{BE}}{dV_{CE}}\bigg|_{fixedIc}\times\frac{1}{I_C\cdot\phi} \approx \frac{\delta V_{BE}}{\delta V_{CE}}\bigg|_{fixedIc}\times\frac{1}{I_C\cdot\phi}$$

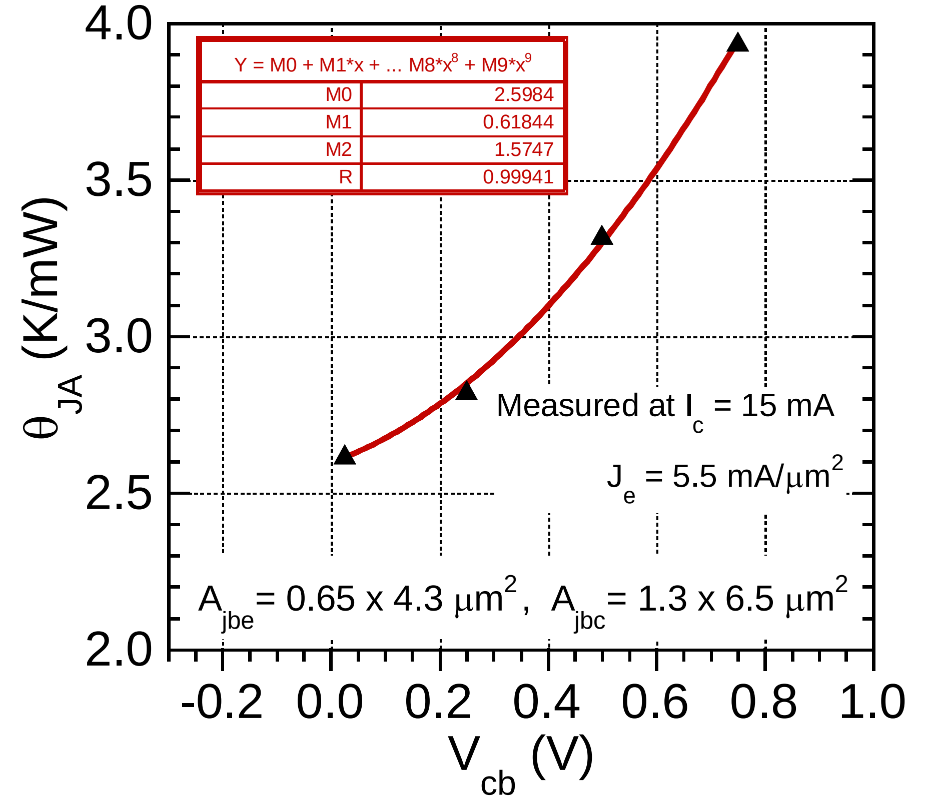
Temperature rise calculated by measuring I_C, δV_{CB} and δV_{BE}

$\theta_{JA} = 2.60 + 0.62V_{cb} + 1.58V_{cb}^2$ (K/mW)

…thermal feedback coefficient

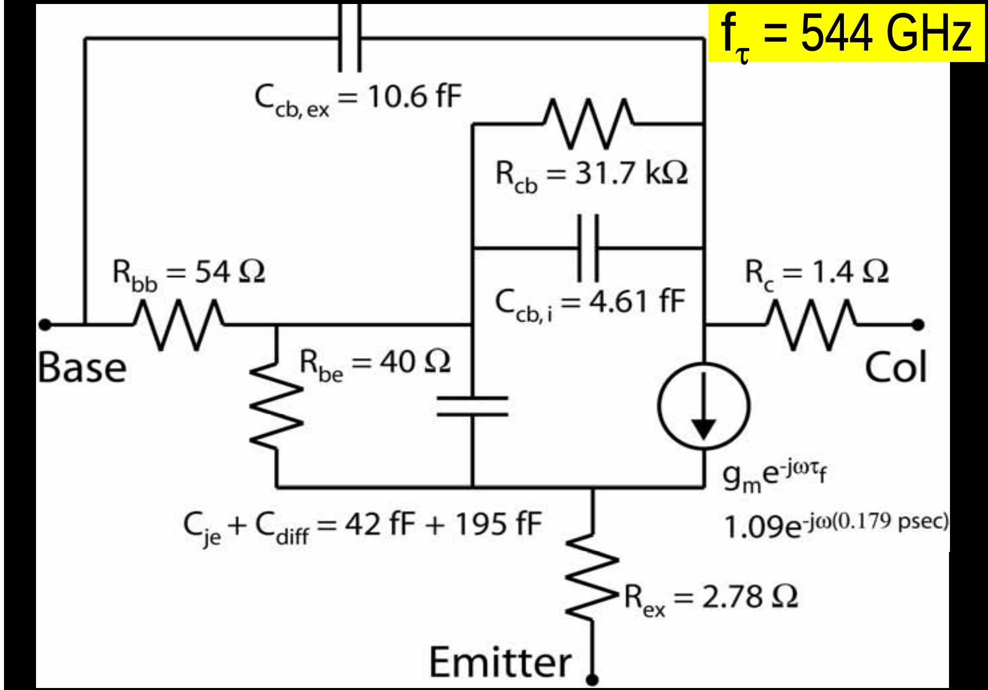
$\phi = 8.40\cdot10^{-4}$ V/K at $J_e = 5.5$ mA/μm^2

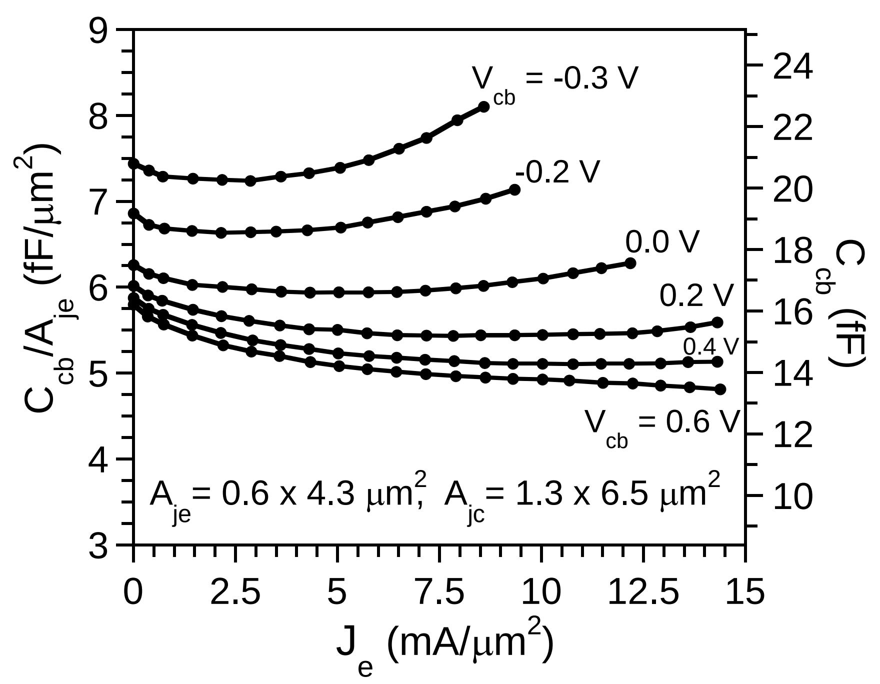




100nm collector, $\theta_{JA} = 2.36 + 0.81\cdot V_{cb}$ (K/mW)

Small signal equivalent circuit and C_{cb} vs bias



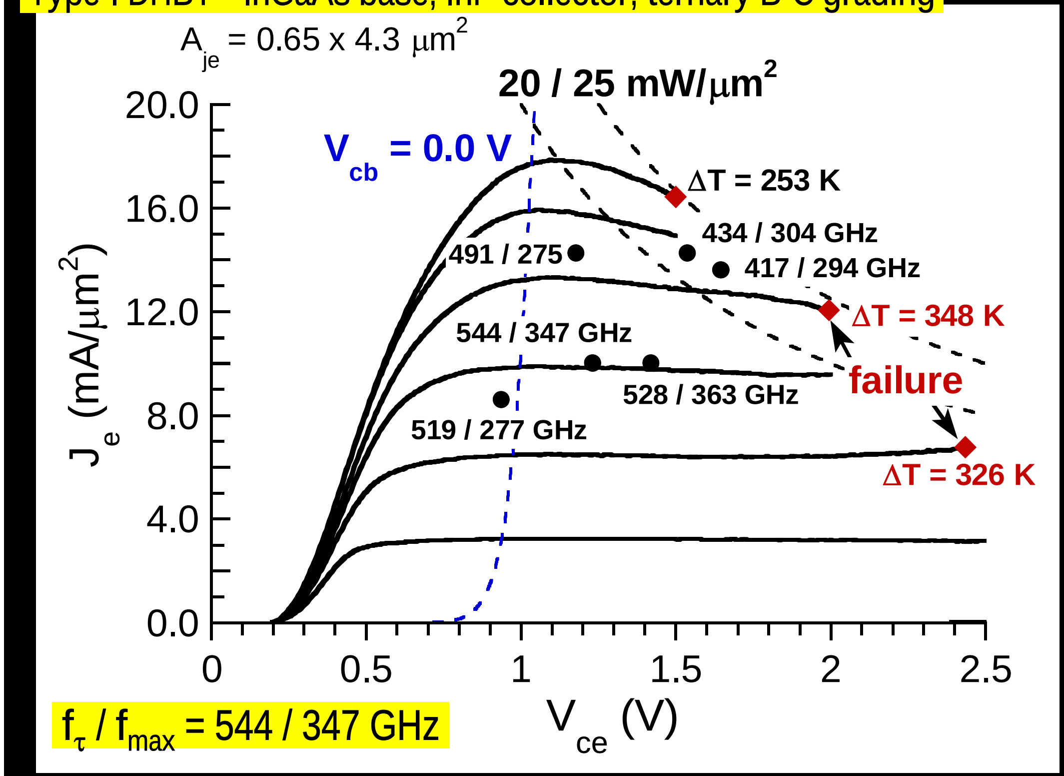


- Total forward delay $(2\pi f_\tau)^{-1}$ = 0.293 psec
- Base and collector transit time = 0.179 psec
- Delays associated with C_{cb} account for 77.5 fsec
    - this is ~ 26% of the total delay
- Increased lateral scaling of the HBT footprint required

- No evidence of Kirk effect until 8-9 mA/μm² at V_{cb} = 0.0V
- At higher J_e and V_{cb}, no C_{cb} increase until J_e > 13mA/μm²
- However, f_τ and f_{max} have decreased at these biases
- Not clear if intervalley scattering or increased temperature are the cause

High power density operation of 75 nm collector InP HBTs

Type-I DHBT—InGaAs base, InP collector, ternary B-C grading

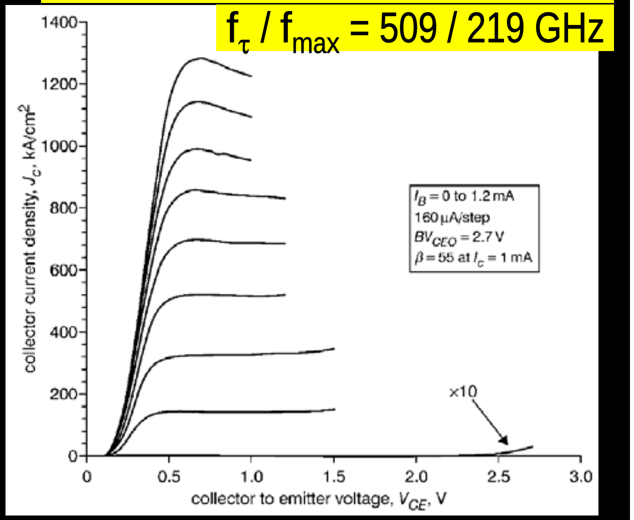


f_τ / f_{max} = 544 / 347 GHz

- InP SHBTs and InP Type-II DHBTs have yet to demonstrate high power density (> 12 mW/μm^2) operation at moderate voltages
- InP Type-I DHBTs however can operate within 20% of BV_{CEO} while dissipating ~ 18 mW/μm^2
- What is more important for digital logic?
  - BV_{CEO} , Safe Operating Area (SOA), or both…?

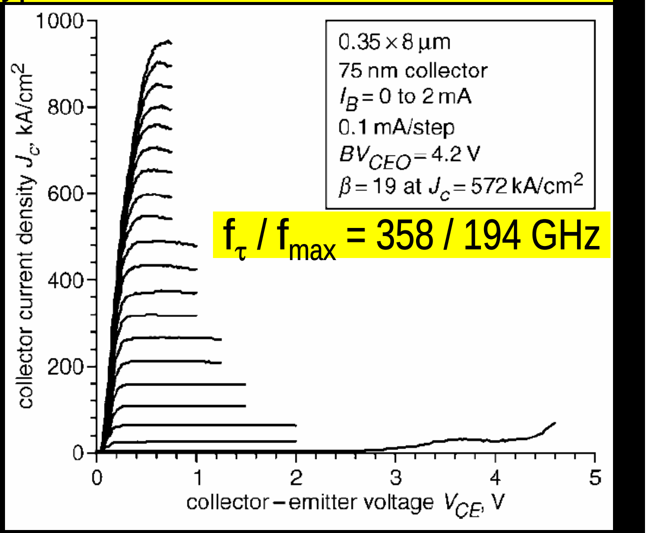
InP SHBT—InGaAs base and collector

f_τ / f_{max} = 509 / 219 GHz



W. Hafez et al., *IEE Letters*, Vol. 39, No. 20, 2003

Type-II DHBT—GaAsSb base, InP collector

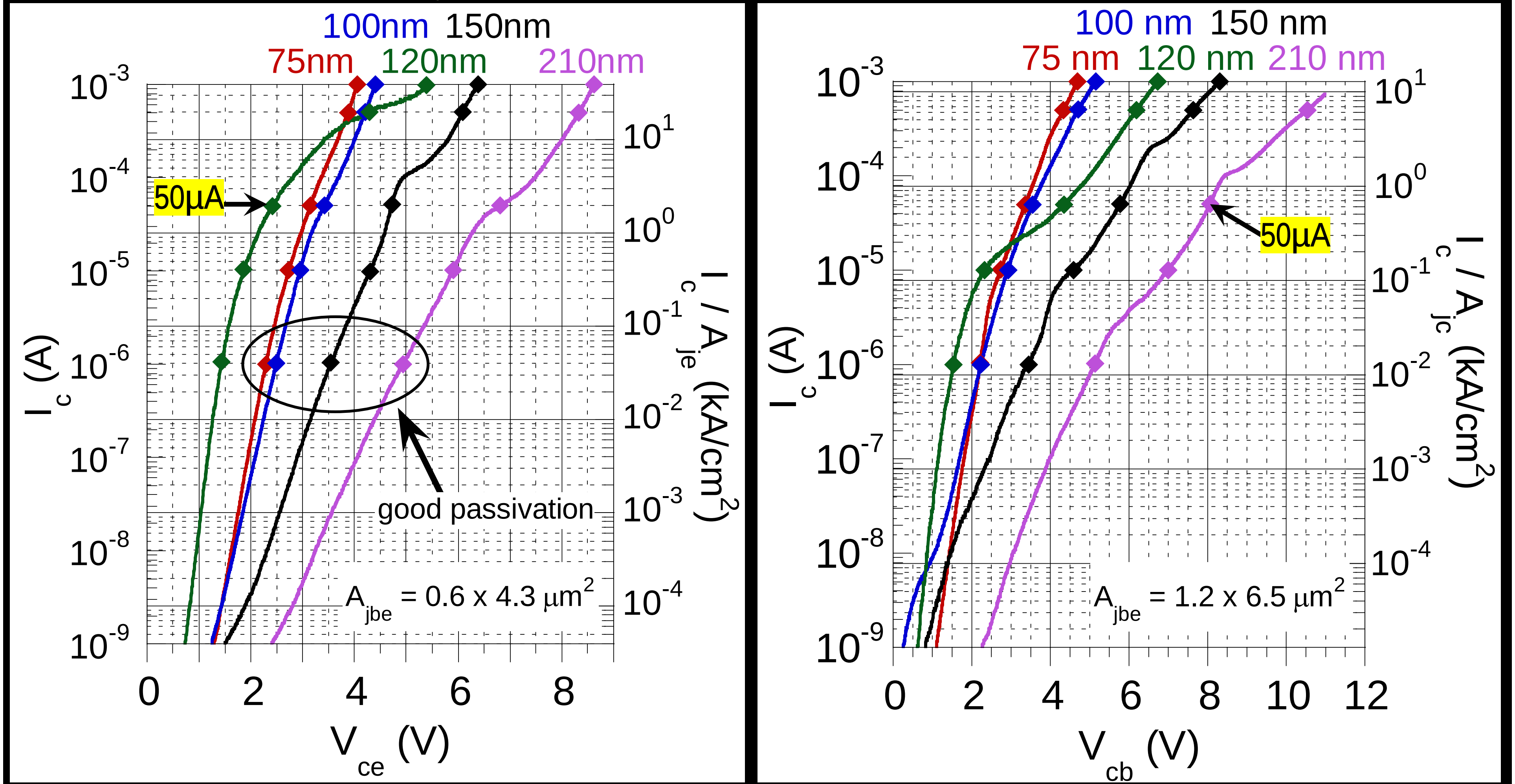


f_τ / f_{max} = 358 / 194 GHz

B.F. Chu-Kung et al., *IEE Letters*, Vol. 40, No. 20, 2004

Common emitter and base breakdown of UCSB InP Type-I DHBTs

Collector thicknesses, T_c



— Breakdown measurements for UCSB InP DHBTs using the same emitter AND collector dimensions

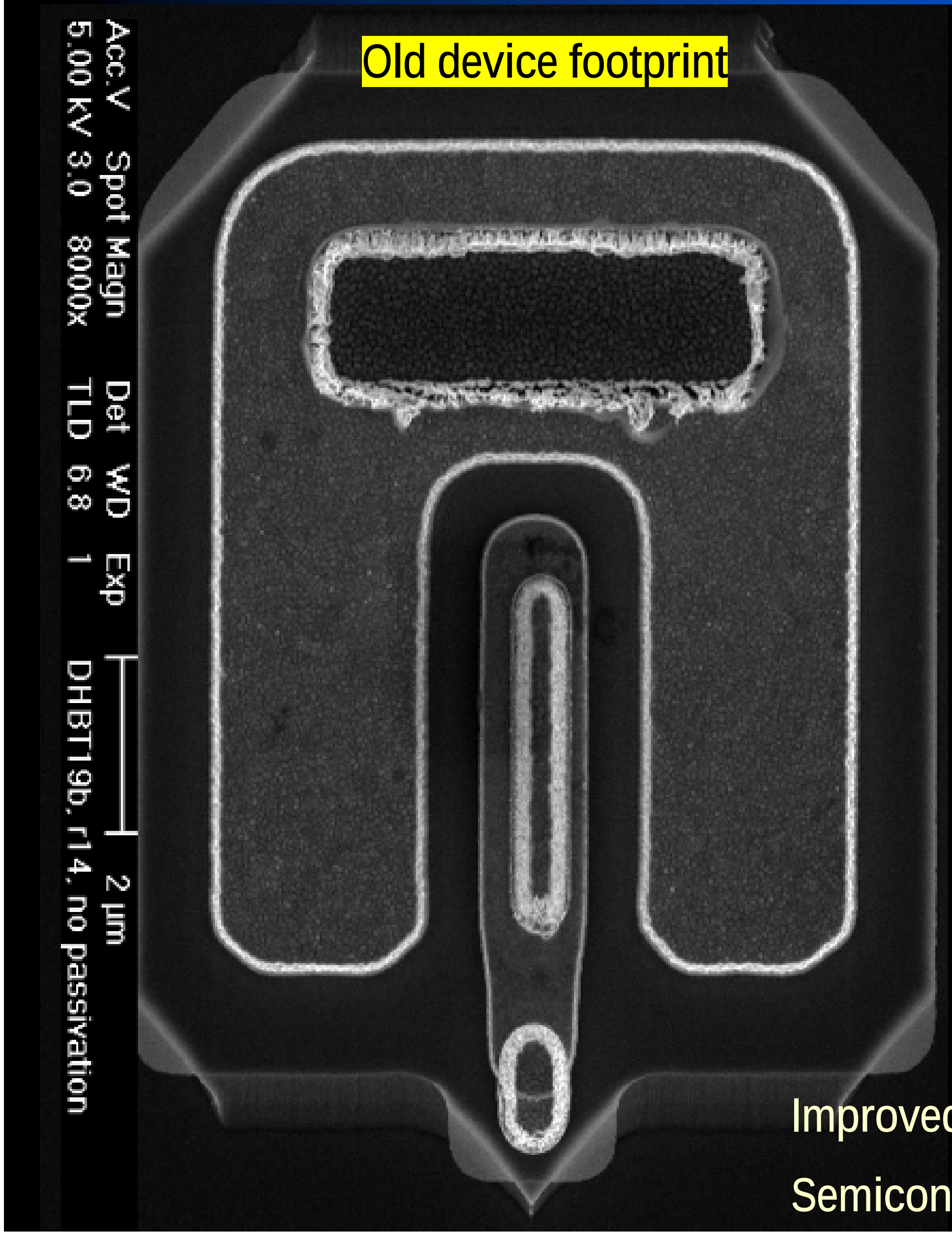
— All HBTs utilize the same device formation techniques and Benzocyclobutene (BCB) passivation

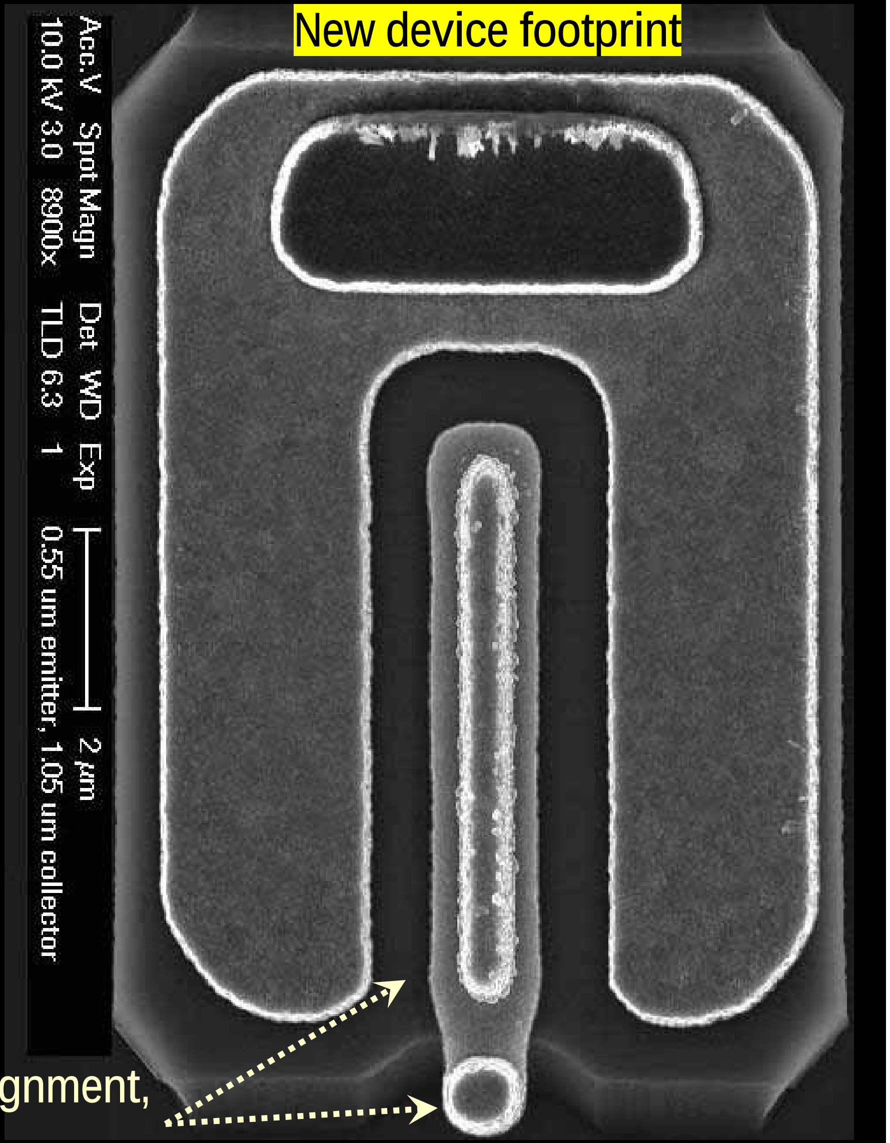
What have we been doing at UCSB to scale the HBT?

…they include

- New UCSB Nanofab stepper system—GCA Autostep 200
- Updated photoresist processes

How the HBT footprint has been improved (at 0.6 µm)

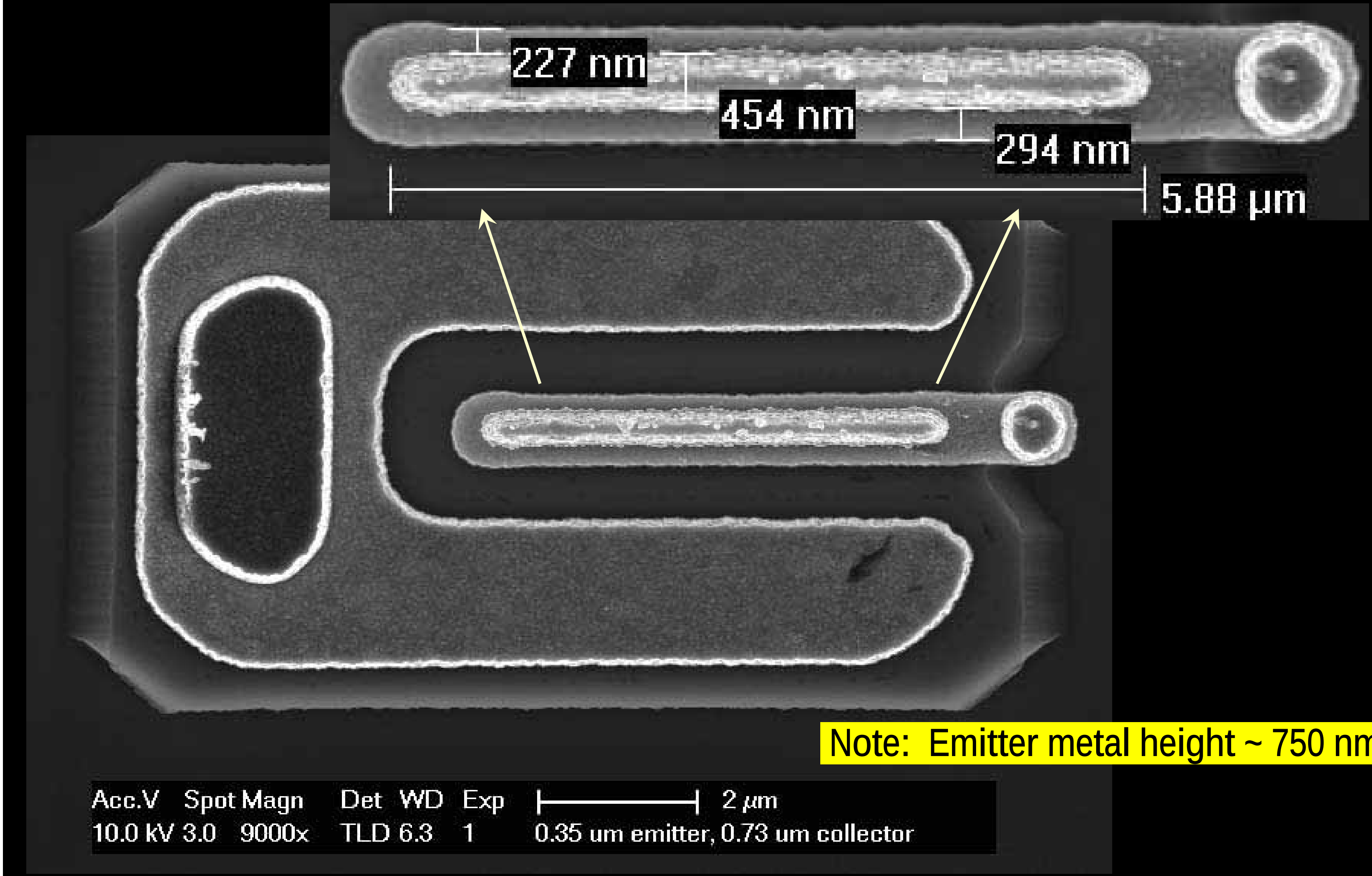

Old device footprint


New device footprint

Improved alignment,

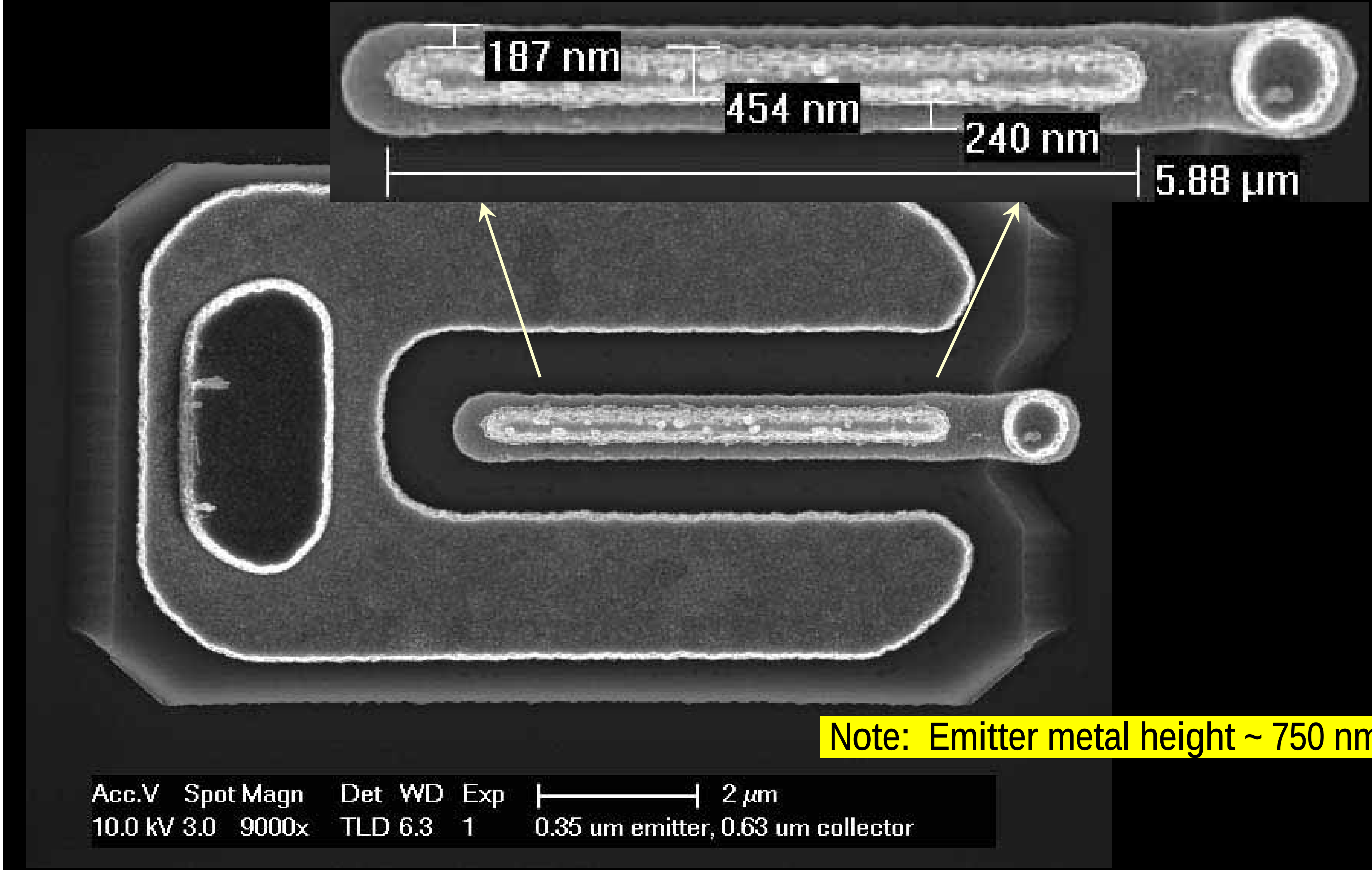
Semiconductor underneath the base post etched twice

0.35 μm emitter junction, $W_c/W_e \sim 2.1$ (similar ratio as old process)



Note: Emitter metal height ~ 750 nm

0.35 µm emitter junction, $W_c/W_e \sim 1.8$



Note: Emitter metal height ~ 750 nm

Conclusion

- A record 544 GHz f_τ has been demonstrated for an InP DHBT
- The trend in C_{cb} with bias is consistent for 75nm across a range of bias
- The 20nm base having a nominal doping of $7\cdot10^{19}$:C had a hole mobility of ~ 55 $cm^2/V\cdot sec$
- The HBT breakdown voltage for this device is similar to the values demonstrated for InP Type-II DHBTs (collector all InP)
- Lateral scaling the HBT footprint is needed…
  - Reduction of C_{cb} for increased f_τ
  - Narrow mesa for reduced R_{bb} and more balanced values of f_τ and f_{max}

This work was supported DARPA under the TFAST program, N66001-02-C-8080