Thermal Limitations of InP HBTs in 80- and 160-Gb ICs

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***Abstract*—Bipolar transistor scaling laws indicate that the dissipated power per unit collector–junction area increases in proportion to the square of the transistor bandwidth, increasing to $\sim 10^6$ W/cm^2 for InP heterojunction bipolar transistors (HBTs) designed for 160 Gb/s operation. A verified three-dimensional finite-element thermal model has been used to analyze the thermal resistance of InP in the context of 80 and 160 Gb^{-1} integrated circuits. The simulations show that the maximum temperature in the device can be significantly higher than the experimentally determined base–emitter junction temperature. Devices suitable for 160-Gb/s circuits will be thermally possible if the InGaAs etch-stop or contacting layer is removed from the subcollector.**

***Index Terms*—Heterojunction bipolar transistor (HBTs), indium phosphide (InP), thermal modeling.**

I. Introduction

INTEGRATED circuits for 40 Gb/s applications are becoming commercially available. Two major competing technologies are SiGe heterojunction bipolar transistors (HBTs) and InP HBTs. There are two types of InP HBT. While very high micrometer wave-power gains have been obtained with single HBTs (SHBTs), they suffer from low breakdown voltages and high thermal resistance because of the narrow bandgap InGaAs collector. To overcome these inherent problems, a double HBT (DHBT), which has an InP collector, can be used. Devices of this kind have been reported with a f_{max} in excess of 450 GHz [2], [3]. These results indicate that DHBTs have potential applications in 80 and 160 Gb/s ICs. This is reinforced by recent observations of frequency dividers operating above 80 GHz [4], [5]. As device design is modified for 80–160 Gbits/s applications, the current density within the device will greatly increase, resulting in higher device temperatures. Accurate thermal design is then critical for accurate circuit simulation and reliability studies.

Thermal modeling of HBTs has, to date, centered on power amplifiers [6] where multiple fingers are in close proximity to each other. These studies have concentrated on modeling the heat flow in the substrate using a semi-analytical approach developed for Si BJTs. [7]. The method does not account for the temperature gradients within the device, which are significant in submicrometer HBTs or for flow of heat through the emitter metallization, which can be high as 20% of the total heat dissipated.

Before InP circuits can be marketed for the 40-Gbit telecommunication market, the device reliability must be assessed, and this has driven an interest in the thermal resistance of InP HBTs[9], [10]. To achieve high bit rates, the collector thickness will be reduced and the devices will be operated at increased current density. This will cause the dissipated power density within the collector to increase, resulting in larger temperatures. Therefore, it is essential that the thermal performance of InP be examined within the context of high-speed digital circuits, and this paper addresses that issue.

II. Device Scaling

To achieve high-speed performance, an increase in the current density will allow a device with a smaller collector–base junction area to be used in the circuit, thereby reducing the collector–base capacitance. However, the current density cannot be increased indefinitely because the electric field at the collector–base metallurgical junction becomes zero caused by the field screening by the injected electrons (Kirk effect). If the collector doping N_D is chosen so that the collector is fully depleted at zero bias current and the applied V_{CE}, the maximum current density through the emitter junction is approximately given by

$$J_{max} = \frac{4\varepsilon v_{sat} V_{CE}}{T_C^2} \tag{1}$$

where ε is the dielectric constant of the collector, T_C is the collector thickness, and V_{sat} the saturated electron velocity in the collector [1]. The minimum time required (τ) by the transistor to switch the output voltage by ΔV can be approximated by [1]

$$\tau \approx \frac{C_{cb}\Delta V_L}{I_0} = \frac{A_c}{A_e}\frac{\Delta V_L T_C}{4 v_{sat} V_{CE}} \tag{2}$$

where I_0 is the switched current and is the product of J_{max}, given by (1) and the area of the emitter A_E. To obtain the last term of (2), the collector–base junction area is assumed to be A_C. Although the performance of digital circuits requires additional terms [1] and depends significantly on the layout of the circuit, (2) is the dominant term in InP HBT digital circuits. By reducing the collector thickness the switching time can be decreased.

It is instructive to examine the dissipated power density when operating at the limits set by (1). Under normal operating conditions, the difference between the conduction band in the base

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and in the subcollector is approximately $V_{\rm CE}$ and so the power dissipated P in the collector is approximately

$$P = A_E \cdot J_{\max} V_{\rm CE}. \tag{3}$$

If the current spreading in the collector is neglected and uniform power dissipation is assumed then the dissipated power density P_D is given by

$$P_{\rm D} = \frac{4\varepsilon v_{\rm sat} V_{\rm CE}^2}{T_C^3} = \left(\frac{A_C}{A_E}\right)^2 \frac{\Delta V_L^3}{(4\varepsilon v_{\rm sat})^2 \tau^3}. \tag{4}$$

As the thickness of the collector is reduced, the switching time will decrease but at a cost of a significant rise in dissipated power density, which will result in a higher device temperature. An alternative way of reducing the switching time is to increase the current density Kirk limit by increasing $V_{\rm CE}$. Again this is paid for by a larger increase in the power dissipation. Equation (4) can be summarized in terms of scaling laws. Using the nomenclature of [1], the dissipated power density scales as the bandwidth cubed γ^3 because the switching time τ is inversely proportional to the bandwidth. Another parameter of interest is the power dissipated per unit collector area and this scales as γ^2. One cannot predict directly from (4) the temperature variation with T_C, because the thermal resistance depends on the device geometry and layer structure. Consequently, no scaling law can be given.

III. Thermal Model

The temperature distribution within a device has been determined by using a commercial finite element solver (ANSYS) to solve the static heat diffusion equation

$$\nabla k(x,y,z) \cdot \nabla T = G(x,y,z) \tag{5}$$

where $k(x,y,z)$ is the position dependent thermal conductivity, T the temperature, and G the heat generation function. In solving three-dimensional (3-D) problems, there is a requirement to reduce the number of nodes so that storage limitations are not exceeded and the computational times are acceptable. Using symmetry, the number of nodes can be reduced. There is a natural plane of symmetry along the length of the emitter and if the base contact pad is ignored there is another orthogonal plane of symmetry. In the derivation of (4), it was assumed that the heat generation in the collector depletion region was uniform. This is not the case. The collector of a DHBT normally consists of an InGaAs set back layer and a grading layer, followed by the InP collector. As the electrons leave the base, they experience a large electric field that accelerates them. In this region close to the base, the electrons move quasi-ballistically with little scattering and so there will be little dissipation of heat. In this model, the ballistic transport region is assumed to extend over the whole of the setback and grading layer. The amount of heat dissipated in the internal resistances of the device is small, and is, therefore, neglected in this model.

Thermal conductivity of semiconductors decreases when the temperature is increased and can be modeled using the equation

$$k_T = k_{300}\left(\frac{300}{T}\right)^n. \tag{6}$$

TABLE I
Thermal Conductivities of the Materials Used in This Simulation

Material	Values used ($Wcm^{-1}K^{-1}$)	n	Experimental Range ($Wcm^{-1}K^{-1}$)	Refs
InP	0.68	1.42	0.68-0.877	[11]
InGaAs	0.048	1.375	0.048-0.061	[12]
Au	3.17	-	3.17	[13]

The thermal conductivity of gold was assumed to be temperature independent.

TABLE II
Layer Dimensions

Label in fig .4	Length (μm)	Sub-layer length (μm)	Description	
Sub	500		Substrate	
SC	0.20		InP sub collector	
ES	0.05		Etch stop layer	
		0.156		InP Collector
		0.024		InGaAs/InAlAs Grade
		0.020		InGaAs setback layer
C	0.2		Total Collector thickness	
B	0.03		InGaAs Base	
		0.12		InP Emitter
		0.04		InGaAs Emitter Cap
E	0.16		Total Emitter length	

The values of the room temperature thermal conductivity and the exponential term (n), used in this work are shown in Table I. In GaAs, the thermal conductivity reduces with heavy doping and a similar effect will also occur in InP and InGaAs. Unfortunately there is no experimental data for InP or InGaAs to incorporate into the model so the thermal conductivity of heavily doped material is assumed to be 65% of the undoped material. This is the measured reduction in GaAs.

The heat flow in the emitter and emitter metallization will be vertical before flowing in a horizontal direction in the emitter interconnect. Rather than model the layers making up the emitter and emitter metallization separately a composite thermal conductivity was used. This can be found by summing the thermal resistances of each layer. Mathematically, this is given by

$$k_E = \frac{\sum T_i}{\sum T_i k_i} \tag{7}$$

where T_i and k_i are the thickness and thermal conductivity of the ith layer. The collector and base metallizations were also multilayer, however the heat flow in these layers is not significant and so these were modeled using the thermal conductivity of gold.

IV. Simulation of Known Devices

Table II gives the layer structure for a recent high-performance device manufactured in our laboratory. A simplified layout is shown in Fig. 1. The polyimide passivation has been neglected because it has a very low thermal conductivity. These devices have a $f_{\max}$ in excess of 400 GHz [3]. The temperature profile through the device is shown in Fig. 2. To obtain this plot the input power was set to 10 mW, which was the same power used in the experimental determination of the thermal resistance and so a direct comparison between the two can be made. As expected, there is significant temperature variation through the device. In the center of the device the emitter–base junction temperature rise is 21.0 K but at the edge of the emitter the increase in junction temperature rise is higher (29.5 K). This can also be seen in Fig. 3. This temperature difference

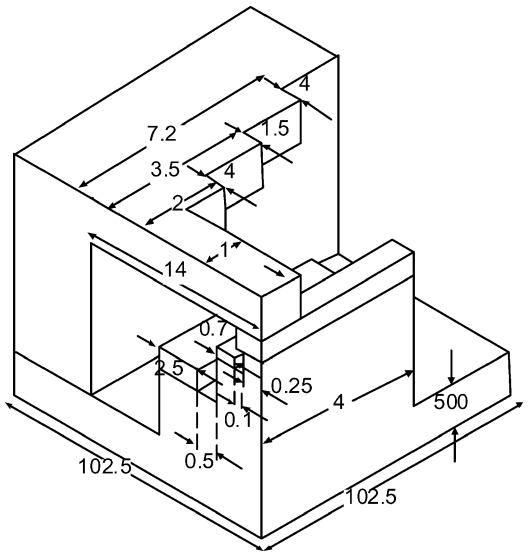

Fig. 1. Simulated device structure used for the verification of the thermal model. (Symmetry allows quarter of the device to be used). All measurements are in micrometers. In order to show the detail, the diagram is not drawn to scale. The thickness of the collector, base and emitter metallization are 0.3, 0.1, and 0.4 μm. The layer structure is given in Table II.

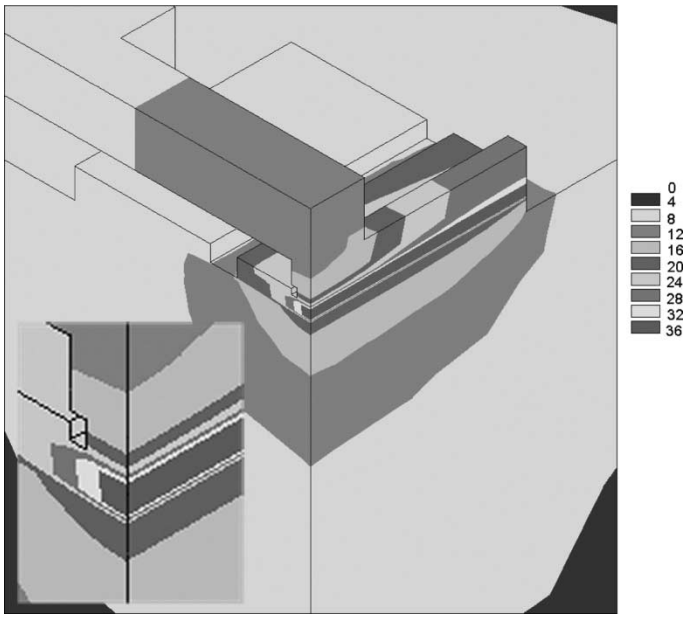

Fig. 2. Temperature rise profile inside the simulated device when the power dissipation was 10 mW. The lower surface of the substrate was fixed at 300 K. The contours are shown as alternating light and dark gray. The collector is the hottest part of the device. (Inset) Central region magnified.

is caused by the limited size of the emitter interconnect. The emitter interconnect is 2 μm wide, while the length of the emitter is 8 μm. So the thermal resistance from the center of the device to the emitter interconnect is less than from the edge of the device to the interconnect. This results in a temperature profile where the edge is hotter than the center. If the emitter interconnect connects to the full length of the emitter contact, then the center of the emitter strip will instead be hotter than its ends [8]. The average temperature rise of the junction is 26.2 K, which corresponds to a thermal resistance of 2620 K/W. This is in good agreement with experimental value 2600 K/W.

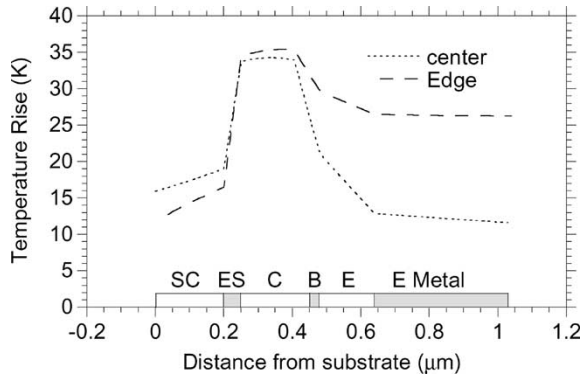

Fig. 3. Temperature profile through the center and edge of the device. The different parts of the device are shown at the bottom of the figure and the labels are given in Table II. The power dissipation was 10 mW.

The collector is the hottest part of the device with a temperature 60% higher than the average temperature of the emitter–base junction. The temperature rise will increase the transit time of the electrons traveling through the collector because of the reduction in the saturated velocity ($v_{\rm sat}$). For a 50 K temperature rise, $v_{\rm sat}$ will reduce by 10%. [14]. From (1), this change in $v_{\rm sat}$ will also reduce the Kirk current density limit by the same amount.

In Fig. 3, the temperature through the center of the device and at the edge is shown. There is a large temperature gradient on both sides of the collector caused by the poor thermal conductivity of the InGaAs used in the base and the subcollector etch-stop layers. Reduction of the thickness of the InGaAs etch-stop layers will significantly reduce the temperature of the collector. This will be discussed in Section VI. The observation of the edge of the emitter being hotter than the center needs further investigation by solving both carrier transport and heat diffusion self consistently to take into account the two effects not included in the model used in this work. If the temperature at the edge increases, the current flowing through this part of the device will increase leading to further increases in current and higher power dissipation. Counteracting this positive feedback effect is the parasitic emitter resistance. Any increase in current will increase the voltage drop across the parasitic resistance thereby reducing the base–emitter voltage and, hence, the current.

As the device speed increases, the thickness of the base decreases and the control of the base metallization diffusion becomes important both during manufacture (yield) and during operation (reliability). The diffusion rate increases with temperature. Therefore if the temperature of the base metallization is higher than expected, this may cause the lifetime of the devices to be below the expected value. In some parts of the device, especially near the ends, the base metallization is higher than the average emitter–base junction temperature. For reasons given above this will have an adverse effect on reliability. Improving the heat sinking of the emitter at the edge of the device by increasing the width of the emitter interconnects will reduce the maximum temperature of the base metallization and so improve the reliability. This will slightly increase the parasitic capacitance between the emitter interconnect and the base contact

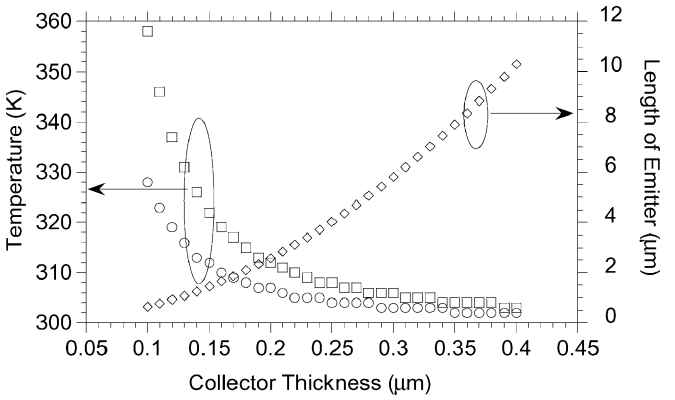

Fig. 4. Circles: variation of junction temperature. Squares: maximum device temperature. Diamonds: emitter length with the collector thickness.

metal. Circuit simulations using Agilent ADS2001 show that the effect on device performance is minimal.

V. Variation of Collector Thickness

As detailed in the introduction speed improvements can be achieved by reducing the collector thickness. In this section the effect of reducing the collector thickness has been investigated. The structure of the device was similar to that shown in Fig. 1 with the exception of the width of the emitter interconnection which was chosen to be the same as the emitter length.

To generate a ΔV of 300 mV across a 50-Ω load impedance requires a 6-mA bias current, and so, in generating Fig. 4, the current flowing through the device was assumed to be 6 mA with a 50% switching duty cycle. Furthermore, when the device was conducting, V_{CE} was assumed to be 1 V. This equates to an average power dissipation of 3 mW. The length of the emitter was chosen so that the device was operating at the Kirk limit given by (1), and the emitter junction width (Fig. 1) remains constant at 0.5 μm. The length is also given in Fig. 4. As expected from (4) the operating temperature of the device increases when the collector thickness reduces. The difference between the junction temperature and the maximum temperature also increases. At a collector thickness of 1000 Å the maximum temperature rise is nearly 60 K. For a 100% duty cycle the temperature rise would be approximately 120 K. Clearly this temperature rise is unacceptable. Increasing the width of emitter interconnect to the full length of the emitter contact also reduces the temperature variation along the length of the emitter with the hottest part of the device now, as expected, at the center.

VI. Devices for 80 and 160 Gbit/s Applications

Results of the previous section show that the operating temperature of the device rapidly increases as the collector thickness is reduced, given that the device is operated at Kirk-effect-limited current density so as to obtain the highest feasible circuit speed. It is therefore important to consider the thermal performance of devices suitably scaled for use in 80 and 160 Gb/s applications. Before these simulations can be performed the key physical parameters for 80 and 160 Gb/s ICs need to be examined. Master-slave latch speed is an important figure of merit because these circuits are heavily used in fiber transceivers. In

TABLE III
Road Map of Key Device Parameters for 80 Gbit/s and 160 Gbit/s InP HBT Circuits

Speed	(Gbit/s)	40	80	160
Collector Thickness	(Å)	3000	2000	1000
Collector Doping	(cm^{-3})	$2\ 10^{16}$	$3\ 10^{16}$	$1\ 10^{17}$
Base doping	(cm^{-3})	$4\ 10^{19}$	$6\ 10^{19}$	$8\ 10^{19}$
Base Sheet resistance	($\Omega\square$)	750	700	700
Base contact resistance	($\Omega\mu m^2$)	150	20	10
Base Thickness	(Å)	400	300	250
Base Mesa width	(μm)	3	1.6	0.4
Current Density	(mA/μm^2)	1	2.3	9.8
Emitter. Junction Width	(μm)	1	0.8	0.2
Emitter Parasitic resistivity	($\Omega\mu m^2$)	50	20	5
Emitter Length	(μm)	6	3.3	3.2
Predicted MS-DFF	(GHz)	62	125	237
f_t	(GHz)	170	260	500
f_{max}	(GHz)	170	440	1000

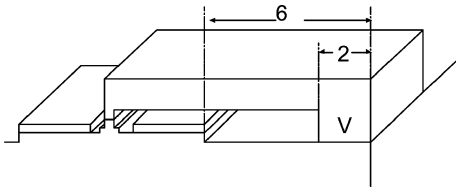

Fig. 5. Physical device structure used in the assessment of the thermal performance of a current switch. Two lines of symmetry are assumed: one midway between the devices and the second through the middle of the devices so that only half of the emitter is simulated. *V* marks a thermal via connecting the emitter interconnects with the InP substrate. All dimensions are in microns.

conservative system-level designs the maximum clock rate is 1.5 times the operating bit rate. To determine the physical parameters of the devices, stated in Table III, the methodology of [1] was used. The base contact resistance and base sheet resistivity are all consistent with values obtained in our laboratory [3]. The 160 Gb/s devices have a very small base–emitter separation as well as a small base mesa. Devices with dimensions similar to the proposed devices have already been manufactured in the GaAs system. (e.g., [15]). Note that the current densities are 1, 2.3, and 9.8 mA/μm^2 at the three bit rates and this drives the thermal design.

High-speed digital circuits have either emitter coupled or current mode topology. In both of these, a bias current is switched between two transistors of a differential pair. These transistors need to be in close proximity to each other for high speed. The second structure models one of the devices in such a differential pair. Under normal operating conditions the heat dissipation in each device is the same and so there is a line of symmetry, modeled using an adiabatic plane midway between the devices. The simulated structure is shown in Fig. 5.

Table IV gives the temperatures at the base–emitter junction and the maximum temperature with and without the collector etch-stop layer. In calculating the device temperatures, the same assumptions as in the previous section were used and so the total power dissipated in the device was set to 3 mW. The temperature rise for the 40- and 80-Gb/s devices is clearly within acceptable bounds even when the etch-stop layer was used. The 80-Gb/s device would benefit thermally by a reduction in the thickness of the etch-stop layer. With the etch-stop layer the temperature rise in the 160-Gb/s device is 49 K and 23% of the heat flows through the emitter. Under idle conditions, the dissipated power will be doubled and to the first approximation the temperature

TABLE IV
PREDICTED TEMPERATURE RISE

Speed	(Gbit/s)		40	80	160
Predicted MS-DFF	(GHz)		62	125	237
Temperature Rise (Etch Stop)	(K)	Junction	7.5	14.0	28.0
		Maximum	10.0	20.0	49.0
Temperature Rise (No sub collector etch stop)	(K)	Junction	5.5	13.0	12.5
		Maximum	7.5	9.0	20.5

rise will be 98 K. This value is too high for long-term operation of the device. With no etch-stop layer the maximum temperature rise within the device is significantly lower (20.5 K). Under these conditions the flow of heat out of the emitter is reduced to only 0.3 mW (i.e., 10% of the total). Under idle conditions, the temperature rise becomes 41 K, which is acceptable. Note, the etch-stop layer is used to control the base mesa process and so to get a device operating at these low temperatures will require the development of an alternative base mesa process or etch-stop layer. The InGaAs etch-stop layer also provides an additional benefit. The resistance of contacts on n+ InGaAs is smaller than on n+ InP. Therefore, the removal of the etch-stop layer will increase the collector resistance and the effect of this on circuit performance needs to be considered. If no alternative etch-stop layer with high thermal conductivity can be found then the etch process needs to be carefully characterized so that the thickness of the InGaAs etch-stop layer can be minimized whilst maintaining device yield. Our experiments to date at UCSB indicate that 12.5-nm-thick InGaAs layers are effective both to stop the base mesa etch and to provide low-resistance $\sim 20\ \Omega$-μm^2 collector contacts. For further reductions in HBT thermal resistance, we are presently investigating 5-nm-thick layers.

When driven with a constant base voltage, thermal runaway of the collector current can occur [8]. Independent of the base drive impedance, thermal instability within a multifinger device will result in one emitter finger carrying a large proportion of the current, while thermal instability within a single emitter finger will result in a local concentration of the current density within the emitter finger, usually at the fingers center. Thermal stability [8] is ensured when the stability factor K is less than unity, with K given by

$$K = \frac{\left(\frac{-\partial V_{be}}{\partial T}\right)\Theta \cdot V_{\mathrm{CE}}}{R_{\mathrm{ballast}} + R_{\mathrm{ex}} + \frac{kT}{qI_E}} \tag{8}$$

where Θ is the device thermal resistance, $(\partial V_{be}/\partial T)$ the rate of change of V_{be} with temperature at constant I_E, and R_{ex} the parasitic emitter resistance. In power HBTs ballast emitter resistances R_{ballast} are often used to stabilize the device. In the devices discussed here, R_{ex} is approximately 8 Ω, which is sufficient for thermal stability at $V_{\mathrm{CE}} = 1.0$ V used in these simulations.

VII. CONCLUSION

An experimentally validated thermal model of InP HBT has been presented, and has been used to demonstrate that operation of devices for 80- and 160-Gb/s applications are thermally possible. To achieve this, the etch-stop layer in the subcollector needs to be removed. The parasitic emitter resistance of 8 Ω is sufficient to prevent thermal runaway.

The model also shows that the maximum temperature within the device is higher than the measured value at the emitter–base junction. This observation needs to be taken into account when the reliability of devices is considered.

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