Device Research Conference 2006

250 nm InGaAs/InP DHBT with 650 GHz f_{max} and 420 GHz f_t, operating above 30 mW/μm^2

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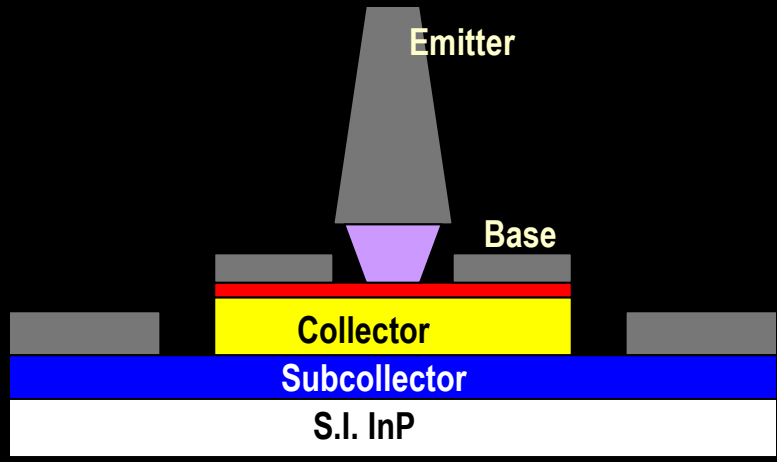
InP/InGaAs Double Heterostructure Bipolar Transistor

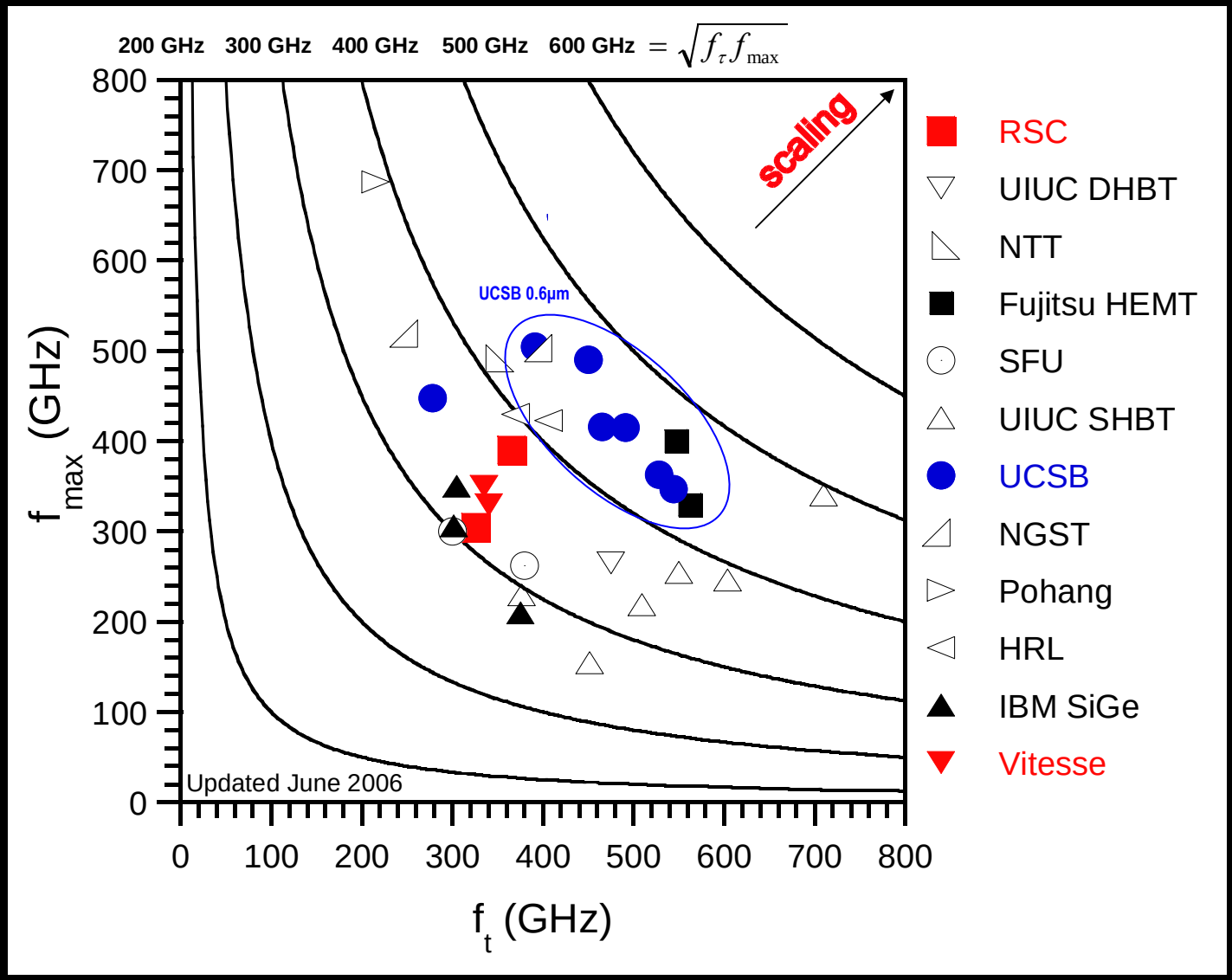
- Mesa DHBTs for high speed applications



- Abrubt InP-InGaAs emitter base junction
- InGaAs base provides good hole mobility
- Setback and Grade used for BC junction
- InP collector

• Objective: Improve DHBT performance by lateral scaling of emitter-base junction!

Fast bipolar transistors



Standard figures of merit / Effects of Scaling

Small signal current gain cut-off frequency (from H_{21})

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{nk_B T}{qI_c}\left(C_{je} + C_{bc}\right) + \left(R_{ex} + R_c\right)C_{bc}$$

Thinning epitaxial layers (*vertical scaling*) reduces base and collector transit times… But increases capacitances

Increase current density and reduce resistances.

Power gain cut-off frequency (from U)

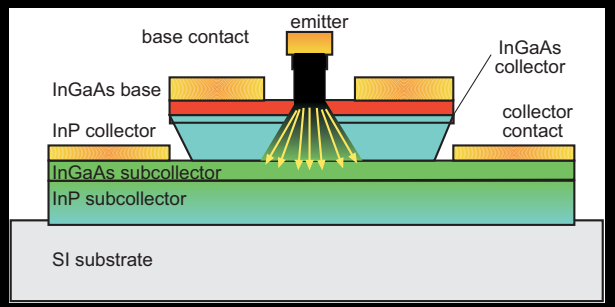
$$f_{\max} \cong \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cb,i}}}$$

Reduce R_{bb} and $C_{cb,i}$ through *lateral* scaling

Charging time for digital logic

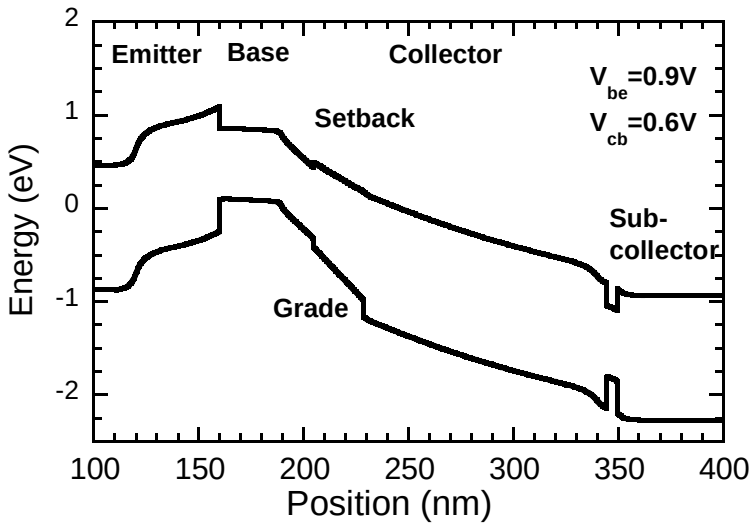
$$\tau \propto \frac{C_{cb}}{I_c}\Delta V$$

Higher J_{kirk}, dimished self-heating due to current increased current spreading



Fabrication I – Epitaxial Stack: 150 nm Collector

- 150 nm collector
- 30 nm base, graded carbon doping
- Thin, 6.5nm InGaAs subcollector
- High f_{max} device with moderate f_T
- *High V_{ceo}*
- Investigate J_{max} increase due to improved thermal capabilities and current spreading – increase in f_T

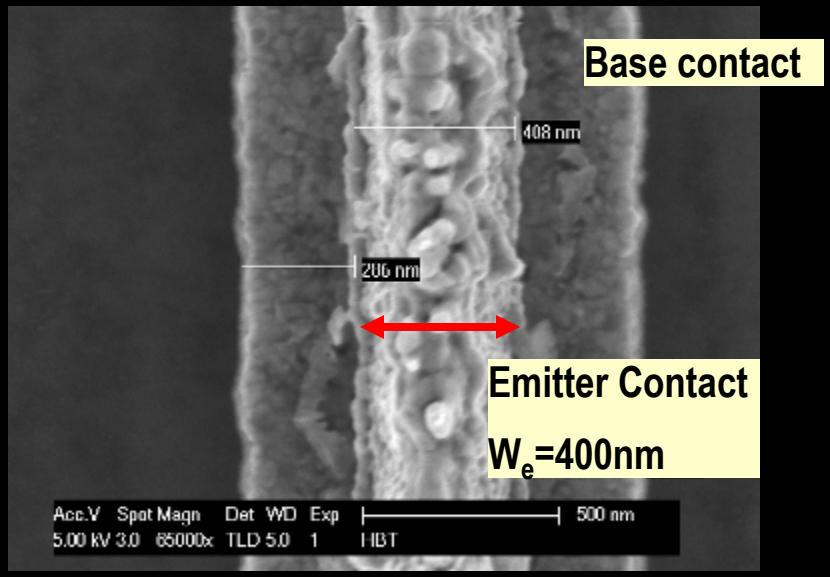


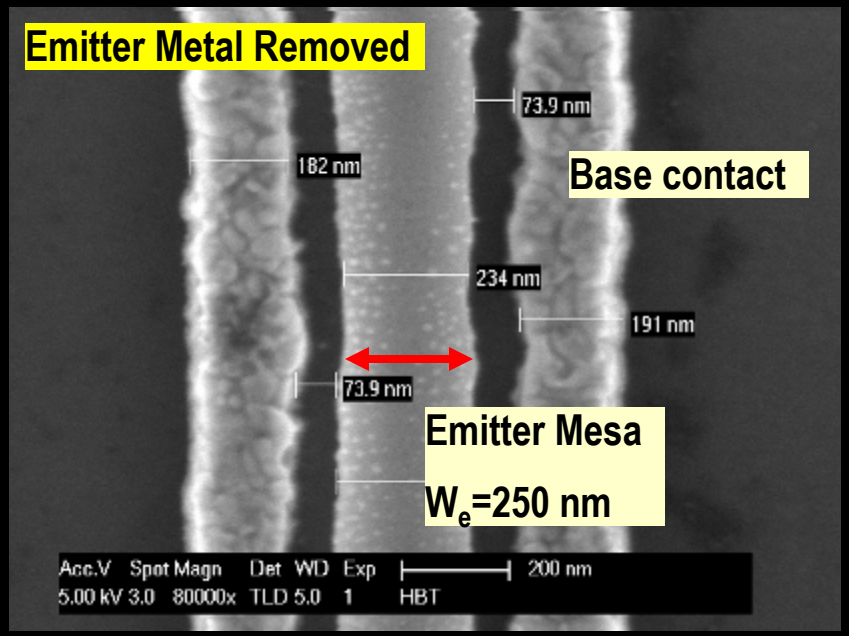
Thickness (nm)	Material	Doping cm^{-3}	Description
5	$In_{0.85}Ga_{0.15}As$	$5{\cdot}10^{19}$: Si	Emitter cap
15	$In_xGa_{1-x}As$	> $4{\cdot}10^{19}$: Si	Emitter cap grading
20	$In_{0.53}Ga_{0.47}As$	$4{\cdot}10^{19}$: Si	Emitter
80	InP	$3{\cdot}10^{19}$: Si	Emitter
10	InP	$8{\cdot}10^{17}$: Si	Emitter
40	InP	$8{\cdot}10^{17}$: Si	Emitter
30	InGaAs	$7\text{-}4{\cdot}10^{19}$: C	Base
15	$In_{0.53}Ga_{0.47}As$	$3.5{\cdot}10^{16}$: Si	Setback
24	InGaAs / InAlAs	$3.5{\cdot}10^{16}$: Si	B-C Grade
3	InP	$2.75{\cdot}10^{18}$: Si	Pulse doping
108	InP	$3.5{\cdot}10^{16}$: Si	Collector
5	InP	$1{\cdot}10^{19}$: Si	Sub Collector
6.5	$In_{0.53}Ga_{0.47}As$	$2{\cdot}10^{19}$: Si	Sub Collector
300	InP	$2{\cdot}10^{19}$: Si	Sub Collector
Substrate	SI : InP		

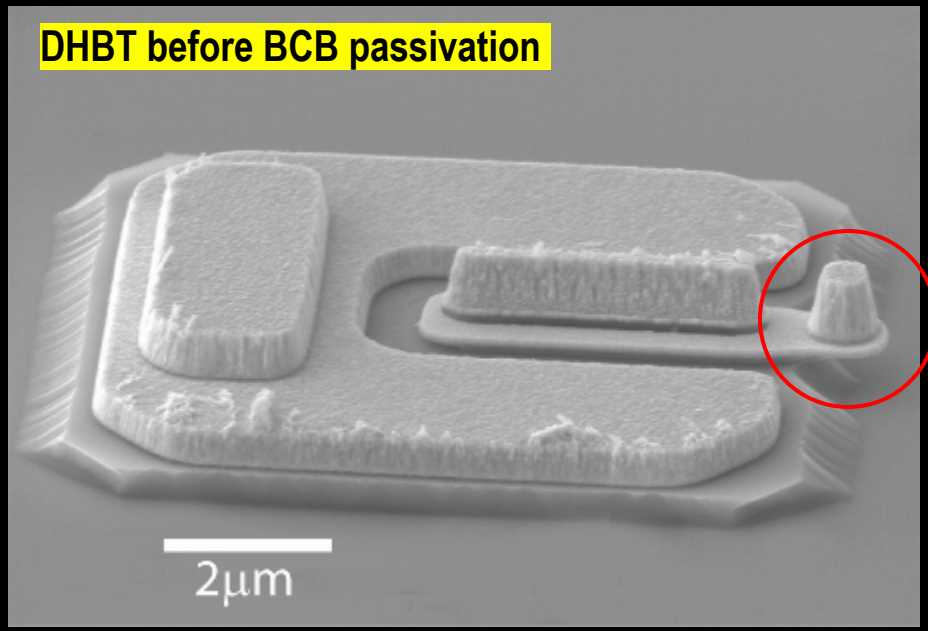
Fabrication II – Lateral Scaling

Fabrication Details:

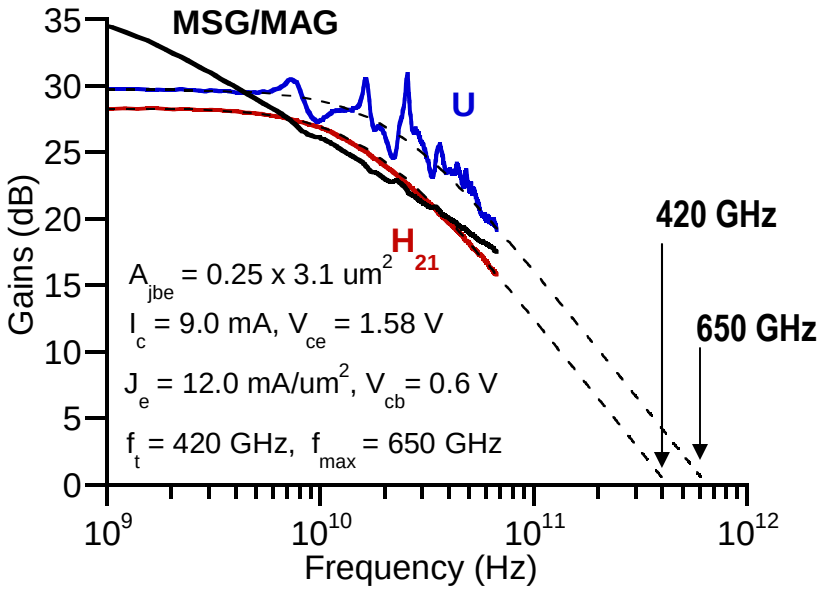
- I-line optical lithography
- All wet etch, lift-off based process
- 250 nm emitter / base junction
- Reduction in C_{bc} by removing semiconductor under base pad
- BCB passivation

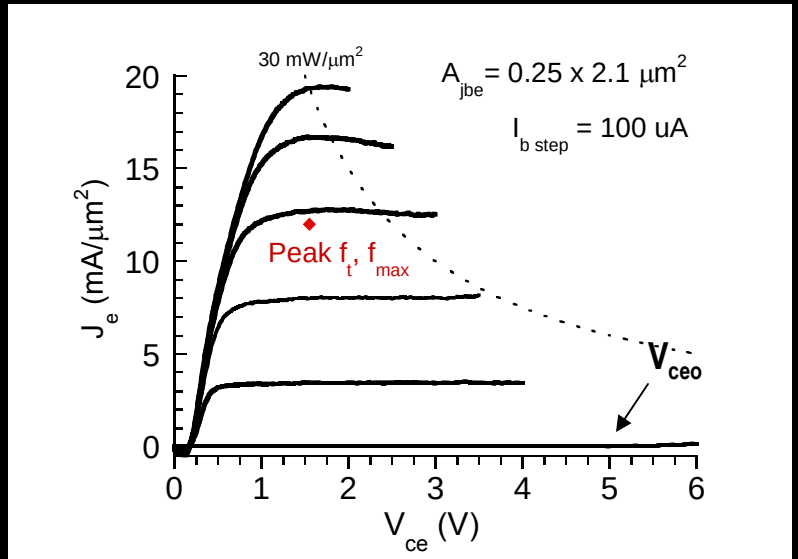


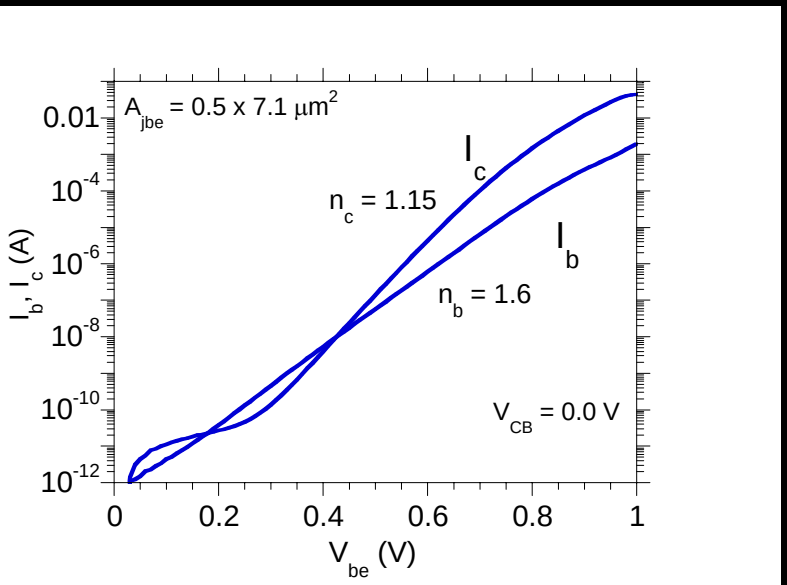




RF and DC performance

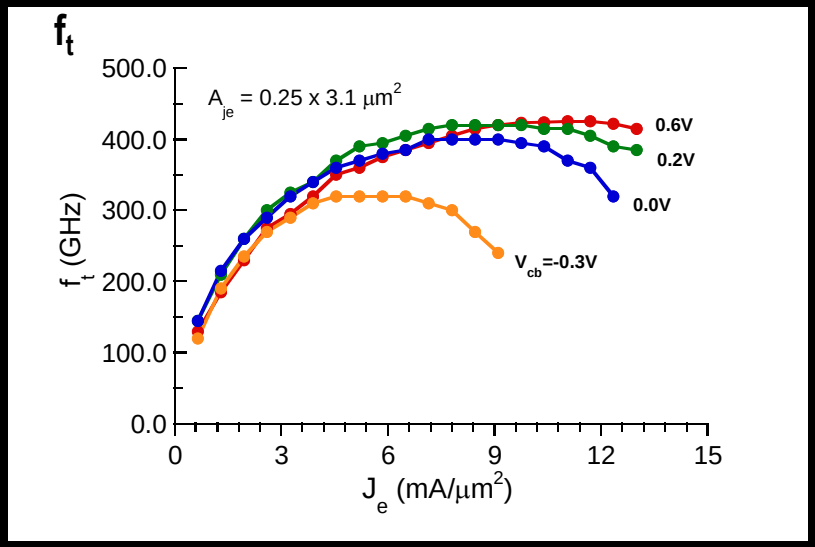


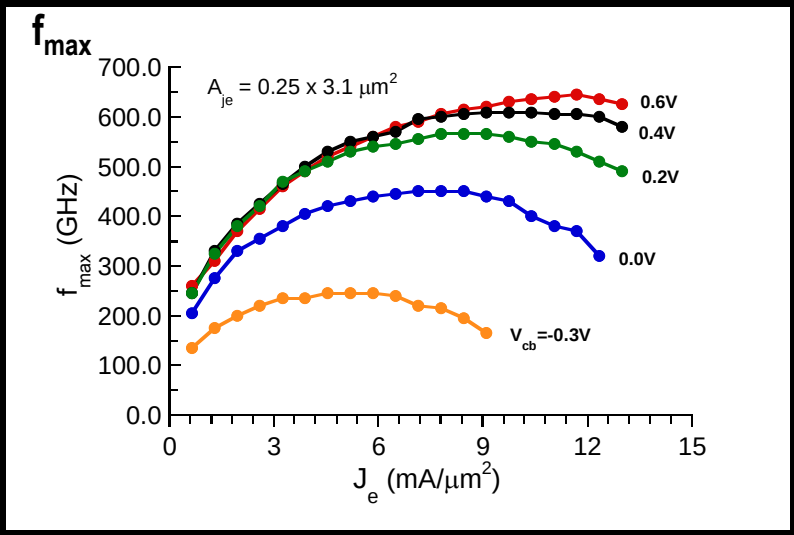




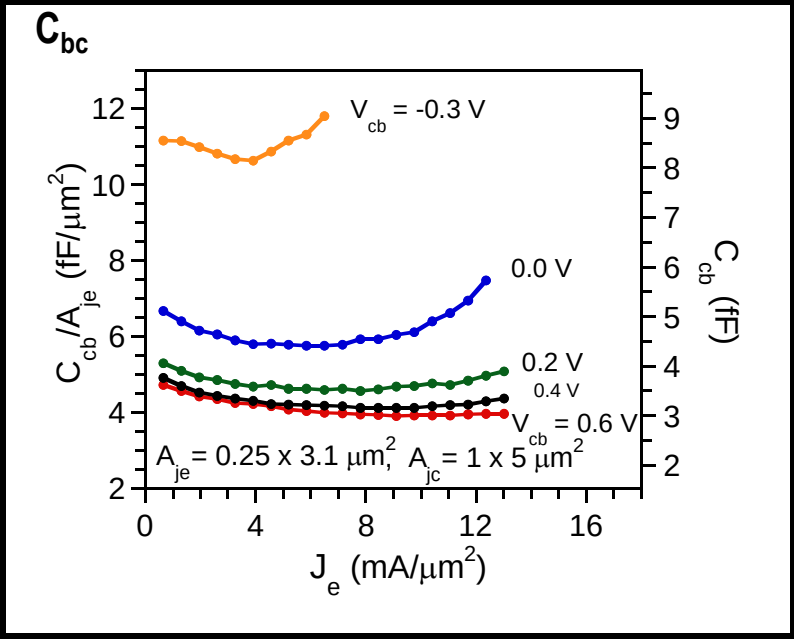
- Summary of device parameters—
- Average $\beta \approx 25$, $V_{BR,\,CEO} \sim 5$ V (@ 1kA/μm²)
- f_{max}=650 GHz
- f_t=420 GHz
- Operates at power densities above 30mW/μm²

f_t, f_{max} and C_{cb} variation

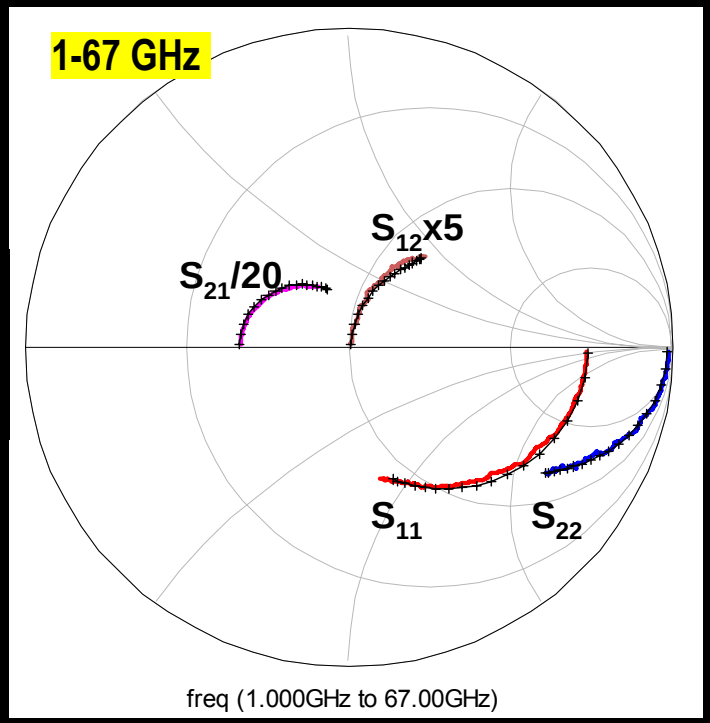


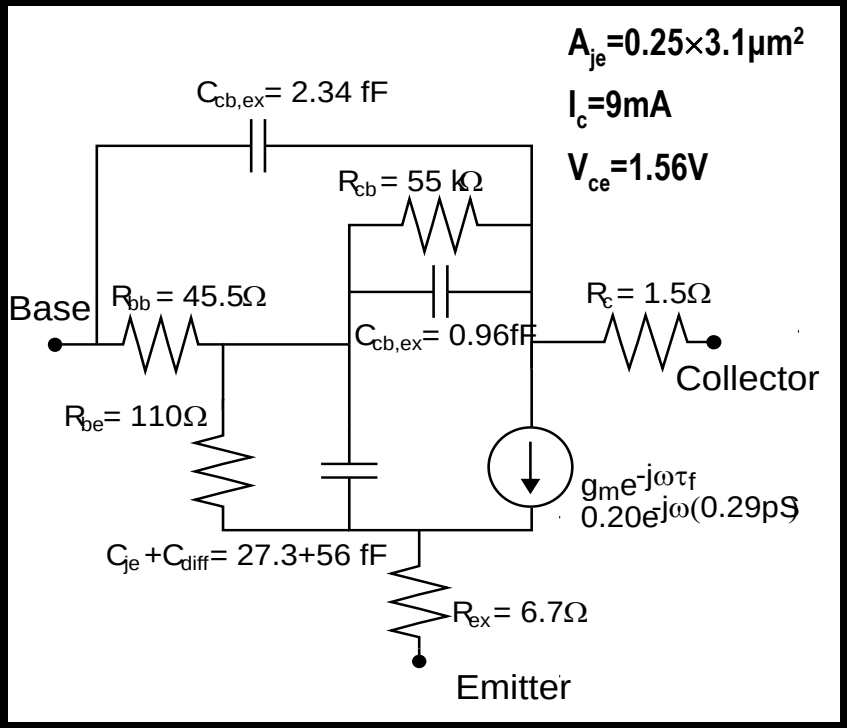


- $J_{kirk} \approx 12$ mA/μm^2 (@ V_{cb}=0.6V)
  - Limited by collector doping and thermal effects
- C_{cb}/I_c=0.30 pS



Small signal equivivalent circuit at maximum f_t, f_{max}



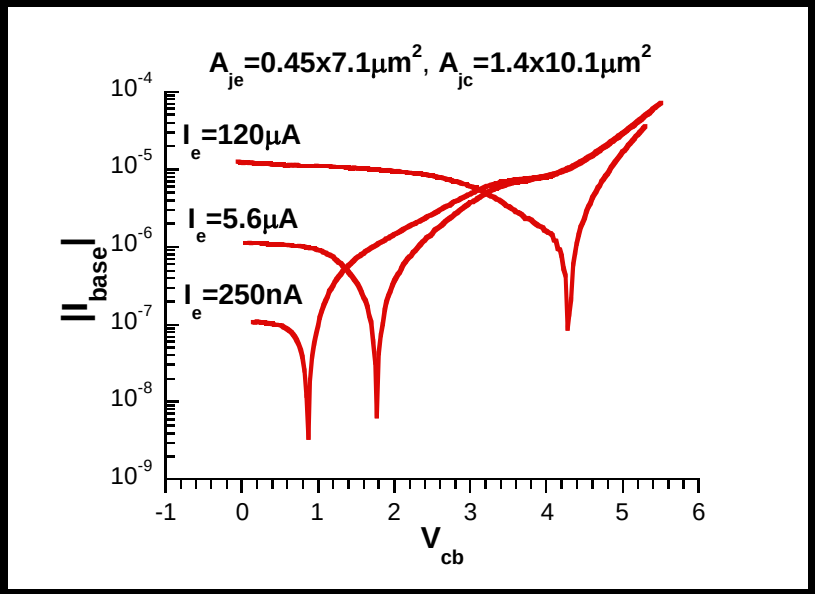


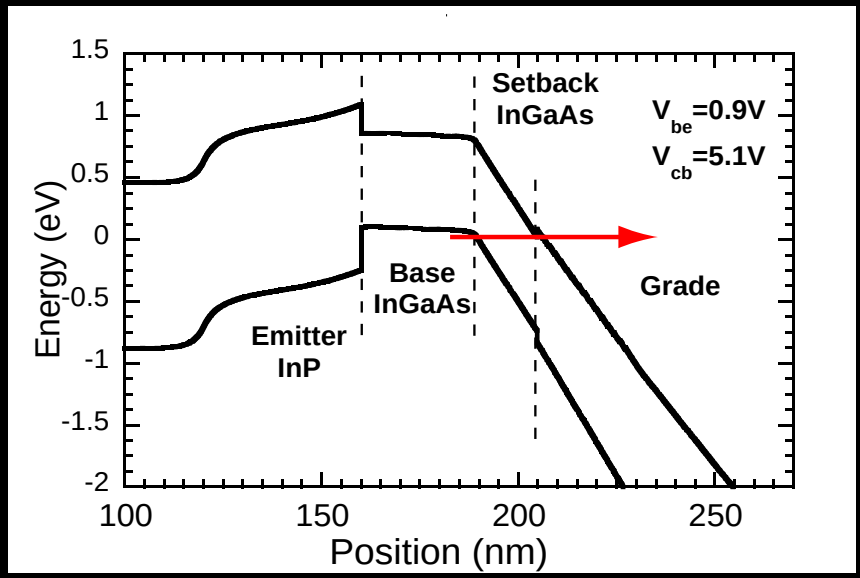
- Total delay time: $1/2\pi f_T$= 0.38 pS
- Base and collector transit times = 0.29pS
- Terms related to C_{cb} = 38 fS
- Larger bandwidth through vertical scaling

Summary resistive elements

- Emitter contact (from RF extraction), $R_{cont} \approx 5.0\ \Omega\cdot\mu m^2$
- Base (from TLM) : R_{sheet} = 635 Ω/sq, $R_{cont} < 5.0\ \Omega\cdot\mu m^2$
- Collector (from TLM) : R_{sheet} = 12.7 Ω/sq, R_{cont} = 10.0 $\Omega\cdot\mu m^2$

Breakdown mechanism for Type-I InP DHBTs



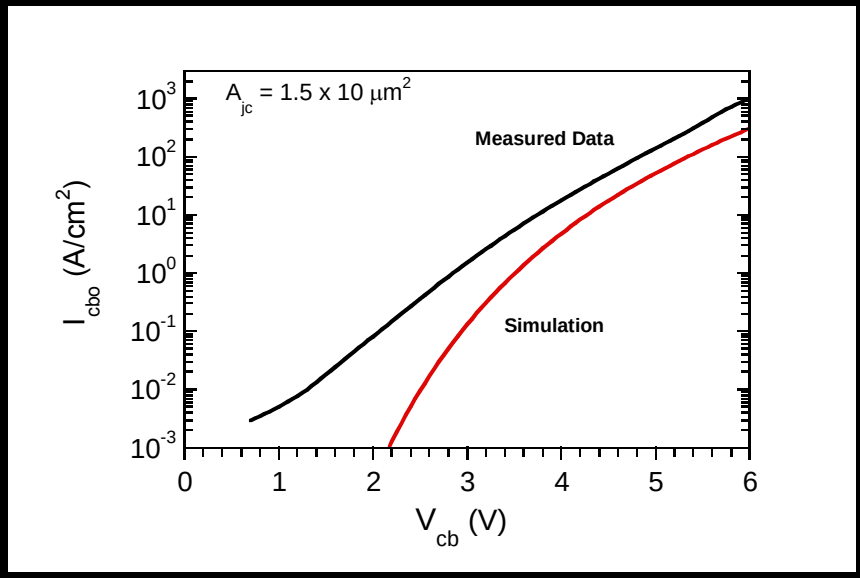


Impact Ionization

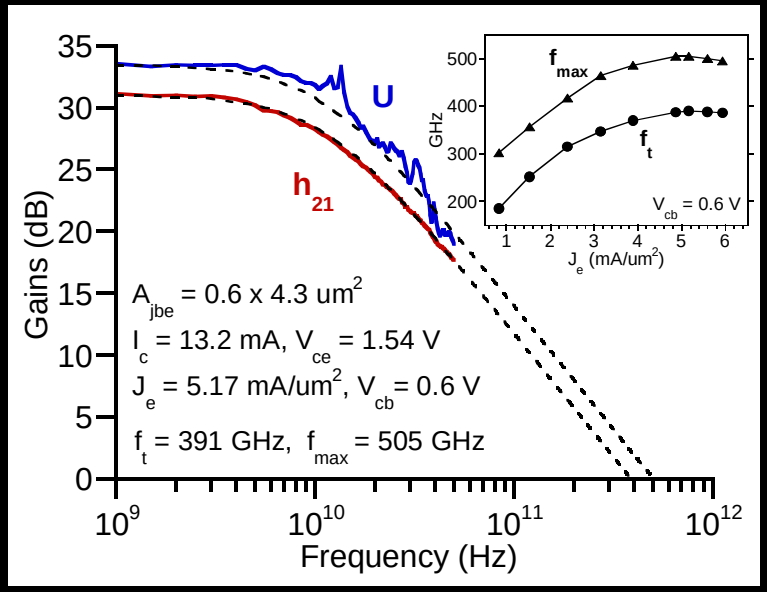
$$I_b = I_b(V_{cb}=0) - (M-1) \times \alpha I_e - I_{zener}$$

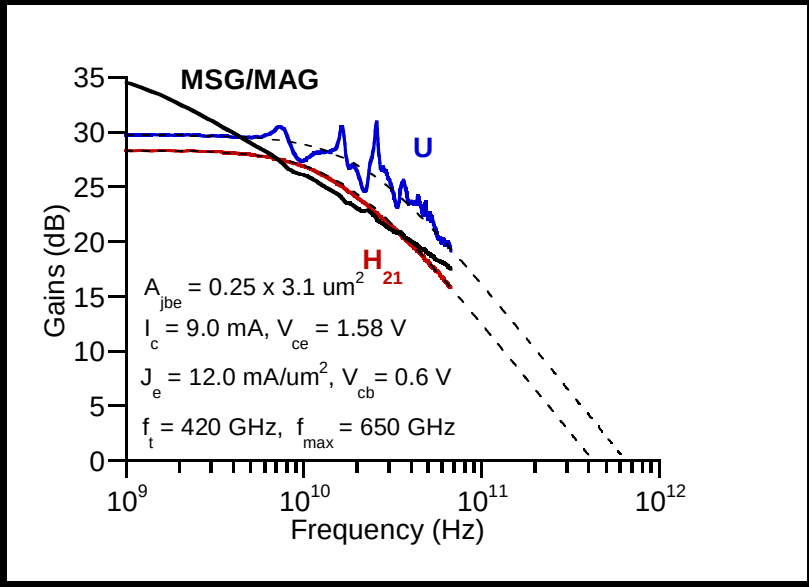
Band to band tunneling

- Breakdown essentially set by tunneling through setback region
- BV_{ceo} ~ 5V
- Proper design of setback and grade is needed for vertical scaling of the collector



Comparison with 0.6μm 150nm T_c UCSB DHBT





2004

- Emitter Width – 0.6 μm
- Emitter contact - $R_{cont} \approx 10.1\ \Omega\cdot\mu m^2$
- Base Contact - $R_{cont} \approx 9.6\ \Omega\cdot\mu m^2$
- $J_{kirk} \sim 5.5\ mA/\mu m^2$ ($P_{max} \sim 15\ mW/\mu m^2$)
- $f_\tau / f_{max} = 391{,}505$ GHz

Griffith et al., IEEE Electron Device Letters, Vol. 26, Jan 2005

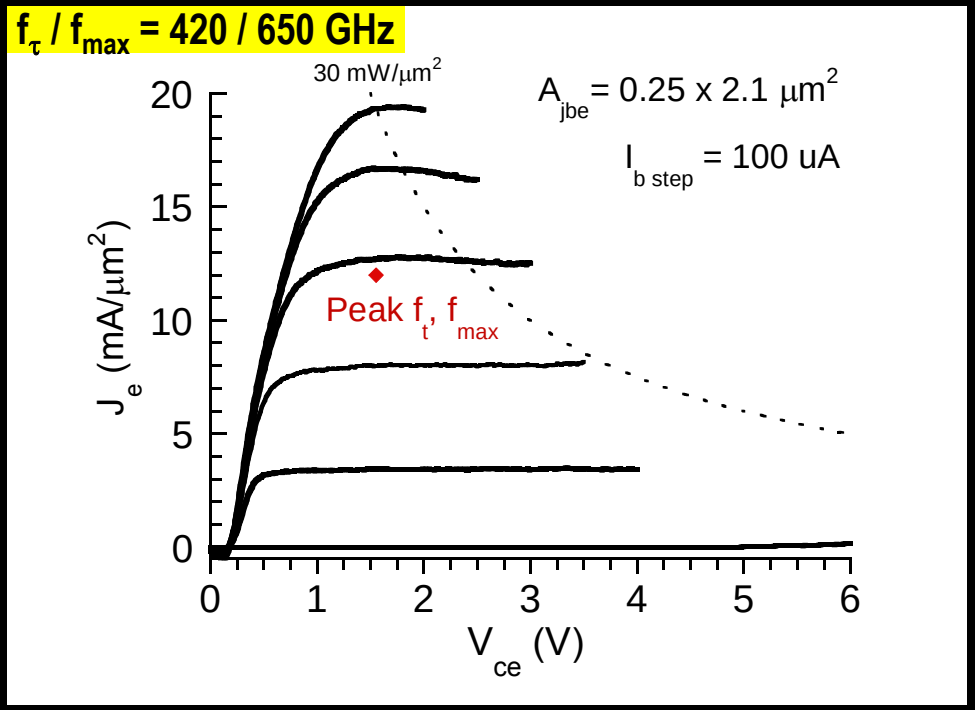
2006

- Emitter Width – 0.25 μm
- Emitter contact - $R_{cont} \approx 5.0\ \Omega\cdot\mu m^2$
- Base Contact - $R_{cont} < 5.0\ \Omega\cdot\mu m^2$
- $J_{kirk} \sim 12\ mA/\mu m^2$ ($P_{max} \sim 30\ mW/\mu m^2$)
- $f_\tau / f_{max} = 420{,}650$ GHz

Comparison with SHBT and GaAsSb technologies

Type-I DHBT—InGaAs base, InP collector, ternary B-C grading

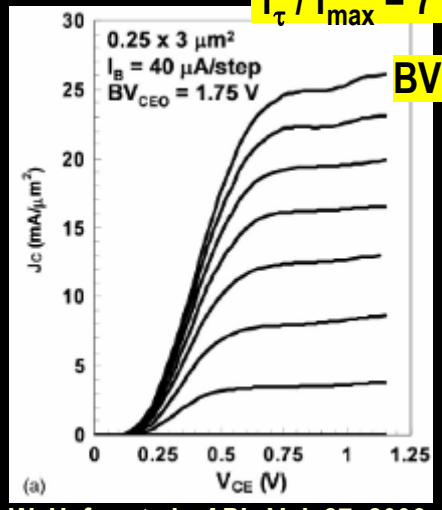
f_τ / f_{max} = 420 / 650 GHz



- Type I InP DHBTs combines high f_τ / f_{max} with high power densities and breakdown voltages
- InP SHBTs (utilizing InGaAs collector) have very high f_t and f_{max}, but low breakdown voltages.
- InP Type-II DHBTs (InP/GaAsSb/InP) have high breakdown, but f_{max} is low due to base resistance.

InP SHBT—InGaAs base and collector (55nm)

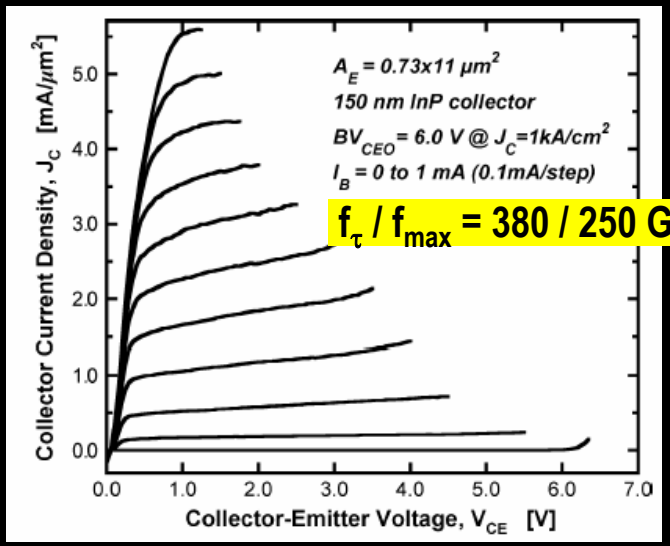
f_τ / f_{max} = 710 / 340 GHz



BV_{ceo} ~ 1.75V

W. Hafez et al., *APL*, Vol. 87, 2006

Type-II DHBT—GaAsSb base, InP collector (150nm)



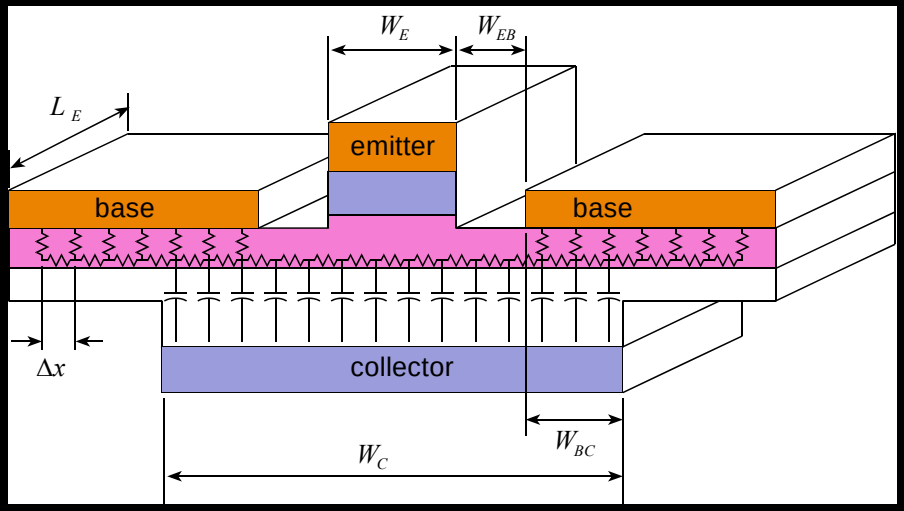
f_τ / f_{max} = 380 / 250 GHz

H.G. Liu et al., *IEEE TED*, Vol. 53, No. 3, 2006

Bipolar Transistor Scaling Laws & Scaling Roadmaps

Scaling Laws:
design changes required
to double transistor bandwidth

key device parameter	required change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter resistance per unit emitter area	decrease 4:1
current density	increase 4:1
base contact resistivity (if contacts lie above collector junction)	decrease 4:1
base contact resistivity (if contacts do not lie above collector junction)	unchanged



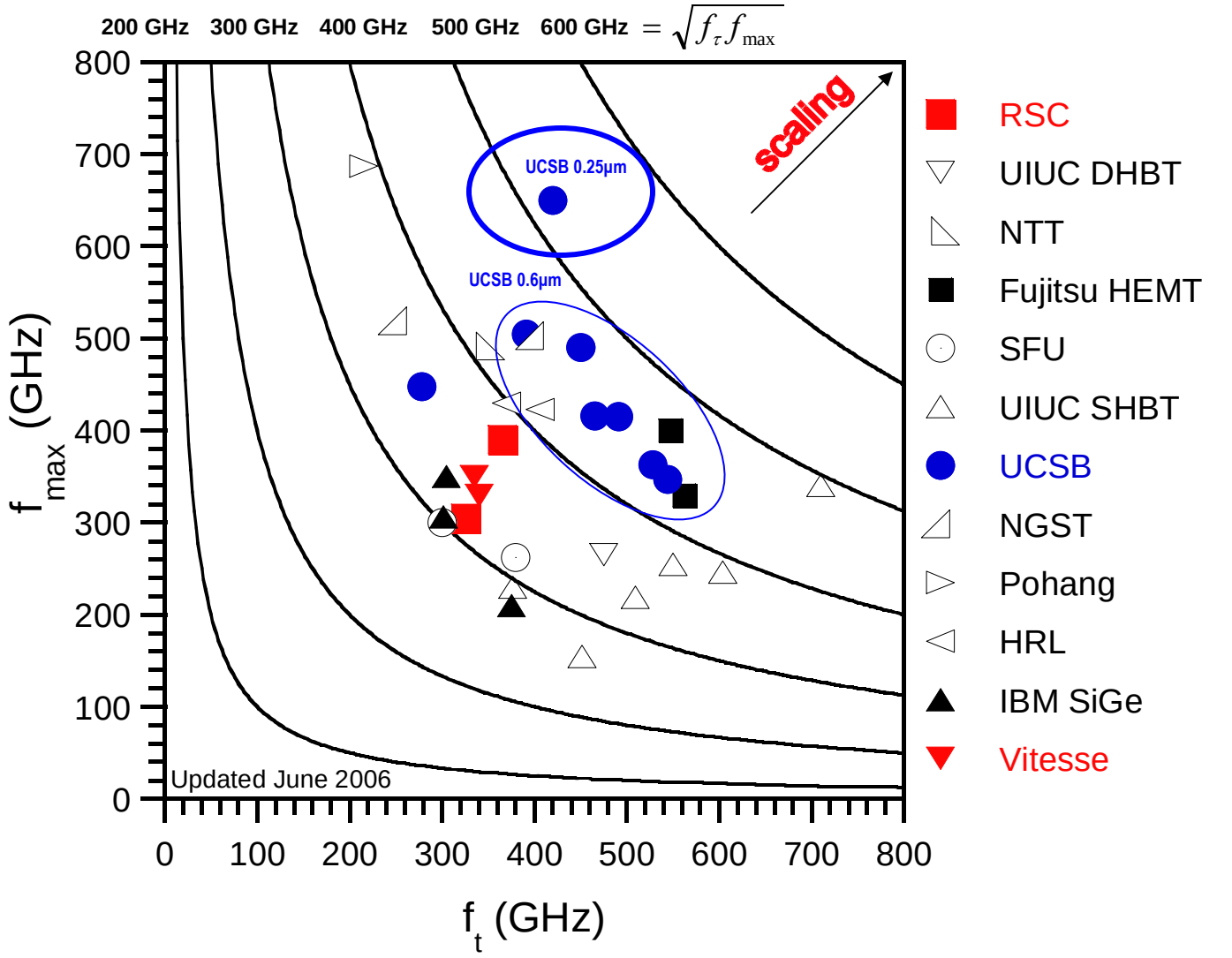
Technology Roadmap through 330 GHz digital clock rate

Parameter	scaling law	Gen. 2	Gen. 3	Gen. 4
MS-DFF speed	γ^1	158 GHz	230 GHz	330 GHz
Emitter Width	$1/\gamma^2$	500 nm	250 nm	125 nm
Resistivity	$1/\gamma^2$	15 Ω-μm^2	7.5 Ω-μm^2	5 Ω-μm^2
Base Thickness	$1/\gamma^{1/2}$	300Å	250 Å	212 Å
Doping	γ^0	7 10^{19}/cm^2	7 10^{19}/cm^2	7 10^{19}/cm^2
Sheet resistance	$\gamma^{1/2}$	500 Ω	600 Ω	707 Ω
Contact ρ	$1/\gamma^{1/2}$	20 Ω-μm^2	10 Ω-μm^2	5 Ω-μm^2
Collector Width	$1/\gamma^2$	1.1 μm	0.54 μm	0.27 μm
Thickness	$1/\gamma$	1500 Å	1060 Å	750 Å
Current Density	γ^2	5 mA/μm^2	10 mA/μm^2	20 mA/μm^2
$A_{collector}/A_{emitter}$	γ^0	2.8	2.8	2.8
f_τ	γ^1	371 GHz	517 GHz	720 GHz
f_{max}	γ^1	483 GHz	724 GHz	1.06 THz
I_E / L_E	γ^0	2.4 mA/μm	2.4 mA/μm	2.4 mA/μm
τ_f	$1/\gamma$	340 fs	250 fs	170 fs
C_{cb} / I_c	$1/\gamma$	440 fs/V	310 fs/V	220 fs/V
$C_{cb}\Delta V_{logic} / I_c$	$1/\gamma$	130 fs	94 fs	66 fs
$R_{bb} /(\Delta V_{logic} / I_c)$	γ^0	0.66	0.51	0.41
$C_{je}(\Delta V_{logic} / I_C)$	$1/\gamma^{3/2}$	350 fs	250 fs	180 fs
$R_{ex} /(\Delta V_{logic} / I_c)$	γ^0	0.24	0.24	0.24

key figures of merit for logic speed

- **The current device is Gen 2.5.**
- **Key enabling technologies for the THz transistor**

Present Status of Fast Transistors



popular metrics :

f_τ or f_{max} alone

$(f_\tau + f_{max})/2$

$\sqrt{f_\tau\, f_{max}}$

$(1/f_\tau + 1/f_{max})^{-1}$

much better metrics :

power amplifiers :

PAE, associated gain, $mW/\mu m$

low noise amplifiers :

F_{min}, associated gain,

digital :

f_{clock}, hence

$(C_{cb}\Delta V / I_c)$,

$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

$(\tau_b + \tau_c)$

Conclusion

- First generation of UCSB 250nm DHBT device
- f_t/f_{max} = 420/650 GHz
- Record f_{max} for a DHBT
- High power density ~ 30 mW/ μm^2
- High Kirk threshold ~ 12 mA/ μm^2
- High BV_{eco} ~ 5V
- Further scaling is feasible

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