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Selectively implanted subcollector DHBTs

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Abstract

$In_{0.53}Ga_{0.47}As$/InP double heterojunction bipolar transistors with implanted subcollectors have been designed and fabricated to eliminate the base access pad capacitance. A blanket Fe implant eliminates the interface charge and a patterned Si implant creates an isolated N^{++} subcollector. The extrinsic base-collector capacitance C_{cb} associated with the base interconnect pad (~25% of the total C_{cb}) is thus eliminated. These implanted subcollector DHBTs have 363GHz f_t and 410GHz f_{max}. The DC current gain β ~ 40, BV_{ceo} = 5.6V, BV_{cbo} = 6.9V (I_C = 1 mA).

I. Introduction

Development of digital logic and mixed-signal systems operating at higher clock speeds and bandwidth require continued improvement in transistor performance [1]. Projected HBT performance for 160 Gb/s systems include an f_τ and f_{max} > 450 GHz, a breakdown voltage $V_{BR,CEO}$ > 3 V, operating current density J_e > 10 mA/μm^2 at V_{cb} = 0 V, and low base-collector capacitance (C_{cb}/I_c < 0.5 ps/V) [2]. When designing an HBT for use in a digital IC, it should be done with emphasis on minimizing the major delay terms associated with $\tau = C_{cb}\Delta V_{logic}/I_c$. The base collector capacitance C_{cb}, thus contributes significantly to analog bandwidth and digital delay. The parasitic capacitance under the base access pad is non scaleable and is a significant fraction of the total base collector capacitance, especially for shorter length devices used in high speed, low power logic circuits. A popular approach to eliminate this base access pad capacitance is through the use of micro air-bridges [3]. Typically in such processes, the subcollector under the feed lines from the base pad is removed by anisotropic wet etching. The base feed lines therefore are very narrow ~0.6-0.8 μm and these thin lines can present a large access resistance, and poses a reliability issue.

Selective ion implantation is a viable alternative to eliminate the base access pad capacitance. Si can be implanted selectively to form the N^{++} subcollector. However, the InP growth interface has an N-type charge (10^{12} – 10^{13} cm^{-2}) associated with it [4] which is also present under the base access pad. The access pad capacitance is not eliminated unless this charge is depleted or suppressed. Earlier results have used process and growth techniques [4, 5], to eliminate this interface charge. Here a shallow Fe implant, a mid gap acceptor in InP, is used to compensate the interface charge. We report here an InP double heterojunction bipolar transistor employing Fe and selective Si implant to eliminate the parasitic base collector capacitance associated with the base access pad area, which is ~25% of the total C_{cb}. These devices exhibit 361 GHz f_τ and 404 GHz f_{max} . In addition to the elimination of C_{cb} in the base interconnect pad area, this process provides the following enhancements over existing implanted InP HBT processes: compensation by the Fe implant of charge at the epitaxial growth interface, a single MBE growth and increased wafer planarity. In the first demonstration of this process, the f_τ and f_{max} are the highest reported for DHBTs with such implanted subcollectors. Prior to this work, the highest f_τ and f_{max} reported for InP HBTs with similarly implanted subcollectors are 252 GHz and 283 GHz respectively [6].

II. Process details

The process flow of the implanted subcollector HBT with Fe is shown in Fig. 1. A semi-insulating InP substrate is implanted with Fe at 10 keV, at a fluence of 2x10^{13} ions-cm^{-2} (Fig. 1a) and annealed at 700^{o}C for 5 minutes. The Fe implant conditions are selected to fully compensate the N-type charge at the growth interface between the substrate and collector epitaxial layers over the observed 1 – 5 x10^{12} cm^{-2} range of regrowth interface charge densities. The sample is then selectively implanted (Fig. 1b), using SiN_x as the implant mask, with Si at 200 keV/4x10^{14} ions-cm^{-2}, 40 keV/7x10^{13} ions-cm^{-2} and 10 keV/ 3x10^{13} ions-cm^{-2}, and then activated by annealing at 800^{o}C for10s. The Si implant dose is much larger then the Fe acceptor density (n_{Fe}) in the selectively implanted region. This ensures that a highly N^{++} doped, isolated subcollector region (Fig 1b) is formed. The active InP HBT layers are then grown by MBE. The device N^- drift collector, base, and emitter layers are identical to that reported in [7]. Growth is initiated with a 3.5nm undoped InGaAs etch-stop layer between the InP collector and the InP substrate. The N^- drift collector, base, and emitter layers are grown, and devices are formed by wet-etching the emitter and base mesas. With the selectively implanted subcollector, HBT isolation does not require a mesa etch, reducing the HBT mesa height and hence improving planarity by ~500 nm. As seen in Fig. 2, the base

access pad lies outside the subcollector implant boundary and does not contribute to C_{cb}.

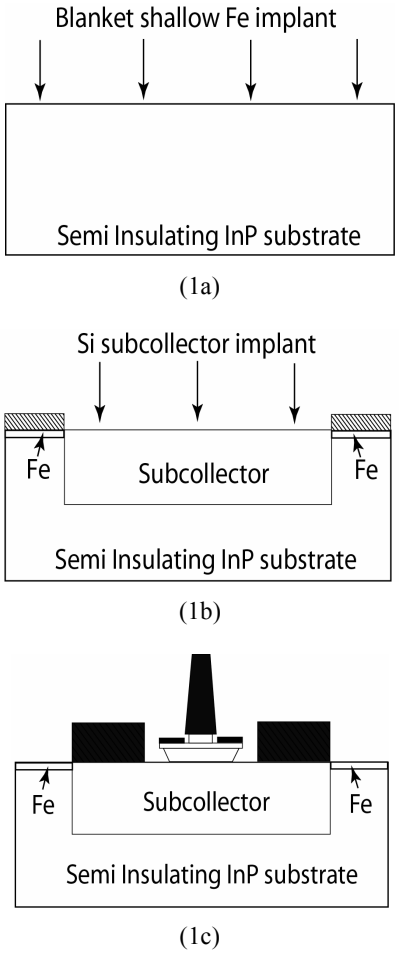

Figure 1: Process flow of the implanted subcollector DHBT

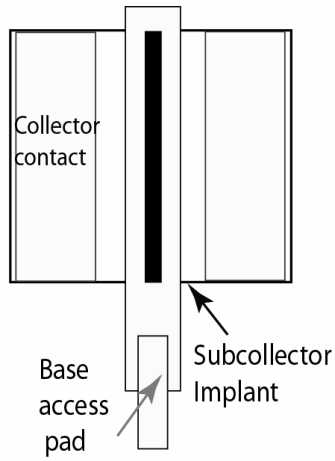

Figure 2: Top view of the Implanted Subcollector DHBT

III. Measurements and Results

Hall measurements indicate that the activation of the implanted Si dopants in the subcollector is ≈ 65% and the electron mobility is ≈ 900 cm^2/V-s. AFM scans of the implanted surface after anneal show a mean roughness of ≈ 1 nm, which is comparable to virgin InP substrate. The isolation between devices is = 10 pA/μm. Standard transmission line measurements (TLM) were performed to extract the sheet resistance ρ_s and contact resistance ρ_c for the base and collector layers. The base sheet resistance ρ_s 1050 Ω and contact resistance, $\rho_c \cong 50\ \Omega\ \mu m^2$. The sheet resistance of the implanted subcollector, ρ_s 25 Ω. The collector contact (Ni/Ge/Au/Ni/Au) is made to InP and partially annealed (320 C / 60s). The anneal temperature was kept low because higher temperature anneals increased the base ρ_c on test samples. Consequently, the collector $\rho_c \approx 500\ \Omega\ \mu m^2$. From RF parameter extraction, emitter ρ_c is $\approx 10\ \Omega\ \mu m^2$. Fig. 3 is a plot of the leakage currents, I_{CBO} and I_{CEO}. From this, V_{CBO} = 6.8 V and V_{CEO} = 5.6V at I_C = 1 mA .

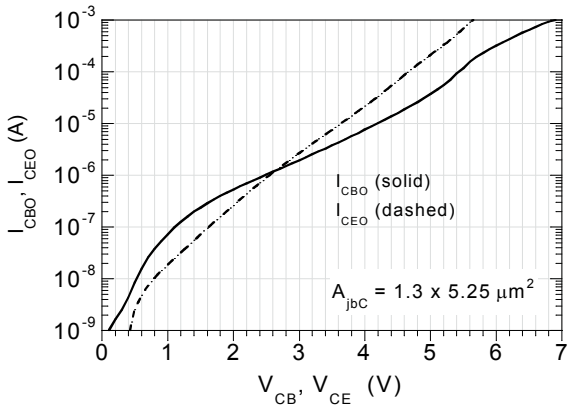

Figure 3: Device leakage currents I_{CEO} and I_{CBO}

The DC I_C-V_{CE} characteristics are in Fig. 4 and the Gummels in Fig. 5. The maximum DC current gain β is 40. The collector and base ideality factors are, η_c = 1.18 and η_b = 1.58. These, and the device leakage currents are consistent with those measured for the equivalent triple mesa DHBT [7].

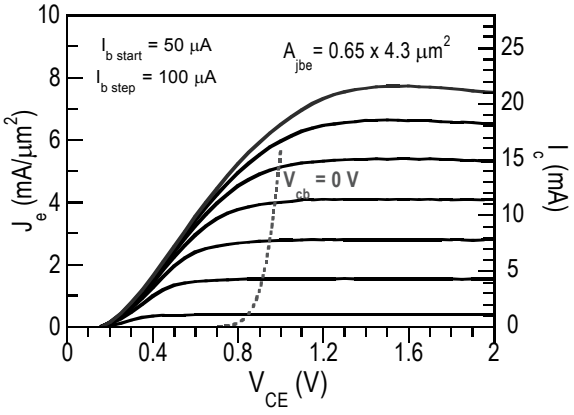

Figure 4: DC I_C - V_{CE} characteristics

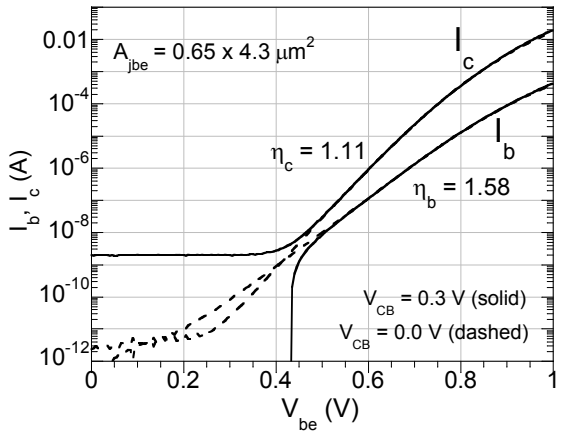

Figure 5: DC Gummel characteristics at V_{CB}= 0V and 0.3V

DC-45 GHz RF measurements were carried out after performing an off wafer Line-Reflect-Reflect-Match (LRRM) calibration on an Agilent 8510C network analyzer. An on-wafer open circuit pad structure identical to the one used by the devices was measured after calibration to de-embed the associated parasitics from the device measurements. Peak f_τ and f_{max} were determined from extrapolation through a least-square-fit to the measured microwave gains $|h_{21}|$ and $|U|$, at measured frequencies. This DHBT has a 0.65 × 4.3 μm^2 emitter s/c junction area A_{jbe} and 1.3 μm collector mesa width.

These first generation implanted subcollector DHBTs have a maximum 361 GHz f_τ and 404 GHz f_{max} (Fig. 6) at I_c = 17 mA and V_{ce} = 1.96 V (J_e = 6.1 mA/μm^2). The f_τ and f_{max} are lower than the standard mesa-DHBT [7]. We attribute this to the higher base sheet resistance and very high collector series resistance due to the poor ohmic contacts to N^{++} InP.

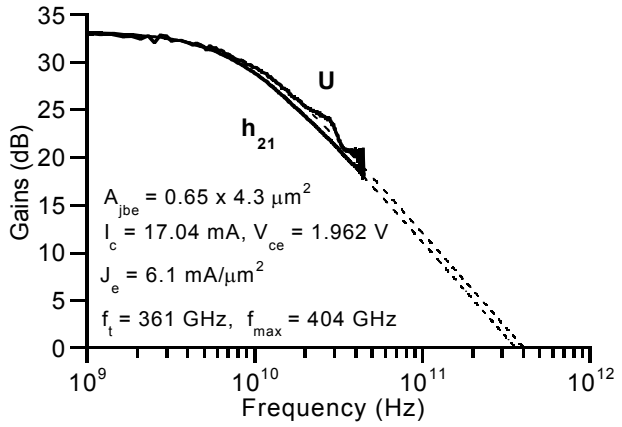

Figure 6: Measured microwave gains

Fig. 5 compares the variation of the total C_{cb} with V_{cb} between the selectively implanted subcollector DHBT and a triple mesa DHBT, both with similar 120 nm collectors and device dimensions identical [7]. The compensation of interface charge is evident, as seen by the reduction in C_{cb} over the entire measured range of bias voltages. For the implanted subcollector DHBTs, C_{cb} is reduced by ~25% corresponding to the elimination of the base access pad capacitance.

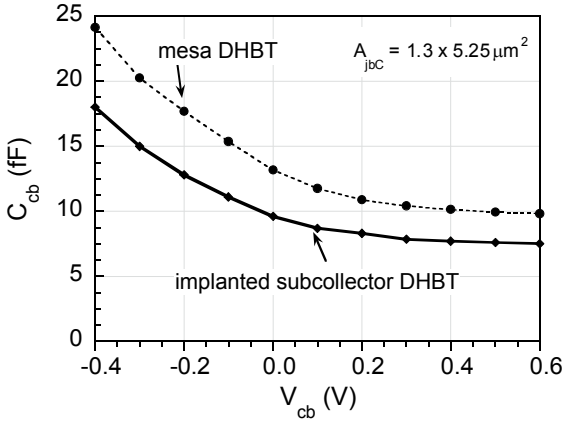

Figure 7: Capacitance Voltage characteristics

Table 1 lists the expected vs. measured reduction in C_{cb} for devices of various dimensions. The slightly lower than expected reduction in capacitance is due to lithographic alignment errors and the lateral implant straggle.

$A_{j,BC}$ on mask (𝕞m^2)	A_{pad} on mask (𝕞m^2)	Effective $A_{pad,}$ isolated (𝕞m^2)	Actual (Expected) reduction in C_{cb} (%)
1.1 x 5.25	2.55	2.07	25 (30)
1.5 x 5.25	2.15	1.66	17 (21)
1.5 x 7.25	2.75	2.73	20 (20)
1.2 x 5.25	2.6	2.15	25 (29)
1.2 x 7.25	2.6	2.43	21 (23)
1.6 x 7.25	2.8	3.13	22 (19)
2.1 x 5.25	2.85	2.13	16 (17)

Table 1: Expected and measured reduction in C_{cb}

The hybrid pi-model extracted from RF and DC measurements is shown in Fig. 8. The thermal resistance is extracted from the Gummel curves and is ~ 2.2 K/mW at J_e = 5.5 mA/μm^2.

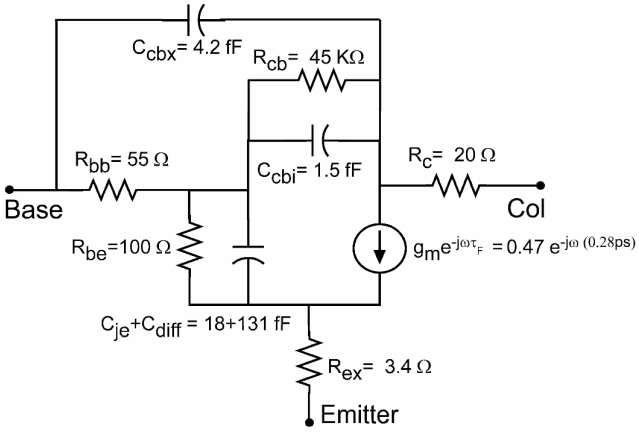

Figure 8: Hybrid-π device model- Peak f_τ , f_{max}

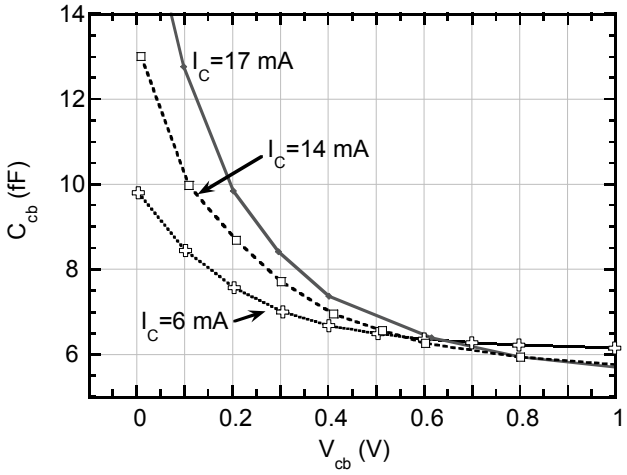

Figure 9: C_{cb} variation w/ bias

Fig. 9 plots C_{cb} as a function of both V_{cb} and I_c for the implanted subcollector DHBT. At peak f_τ, $C_{cb}/I_c \approx 0.3$ ps/V. At higher current levels and low bias voltages C_{cb} increases, caused by the forward biasing of the collector base junction due to the high collector resistance.

V. Discussion

The implanted subcollector DHBTs with Fe and Si implants, have current gain β 40, $\eta_c = 1.18$, $V_{CBO} = 6.8$V, $V_{CEO} = 5.6$V. The device β, ideality factors, leakage currents and breakdown voltages are consistent with those measured from the equivalent triple-mesa HBT [3]. When comparing C_{cb} (V_{cb}) of the two DHBTs with 120 nm collectors, the standard triple mesa DHBT and the implanted subcollector DHBT, a reduction in C_{cb} is seen over the entire measured range of bias voltages. The interface charge is shown to be compensated by the Fe implant and the capacitance associated with the base access pad is eliminated. The hybrid-π model indicates a high collector resistance and higher base resistance, as compared to the triple mesa DHBT [7], which are responsible for lower f_t and f_{max}. The higher base resistance is due to process and growth variations and the high collector resistance is due to insufficient annealing of the alloyed collector ohmic contacts to N^{++} InP. The collector ohmic contact process steps are being revised so that the collector ohmic is formed prior to base contact formation, by recess etching the base and the collector layers. Experiments on test samples indicate that a high temperature anneal (365 C/60 seconds) reduces the contact resistivity of the alloyed collector ohmic contact (Ni/GeAu/Ni/Au) to ≈ 25 Ω μm^2. In this first demonstration of implanted subcollector DHBTs with Si and Fe implants, the cut-off frequencies are the best reported for implanted collector DHBTs. C_{cb} due to the base access pad is eliminated and the lower C_{cb}/I_c should enable reduced charging constants for high speed digital logic. This technology requires no additional growths, improves device planarity and is hence feasible for large scale ICs.

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