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Interface charge compensation in InP based heterojunction bipolar transistors with implanted subcollectors

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We report $InP/In_{0.53}Ga_{0.47}As/InP$ double heterojunction bipolar transistors (DHBTs) with implanted subcollectors. We demonstrate the compensation of charge at the regrowth interface by the use of a blanket Fe implant. An isolated N^{++} subcollector is then formed by a patterned Si implant. With the compensation of the interface charge, this patterned subcollector eliminates the extrinsic base-collector capacitance C_{cb} associated with the base interconnect pad over the entire range of bias voltages. These implanted subcollector DHBTs with the shallow Fe implant have 363 GHz f_τ and 410 GHz f_{max}. The dc current gain $\beta \sim 40$, $BV_{ceo}=4.9$ V, $BV_{cbo}=5.4$ V, and $I_{cbo}<70$ pA at $V_{cb}=0.3$ V. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2221512]

While InP based double heterojunction bipolar transistors (HBTs) benefit from high carrier mobilities and saturated velocities,[1] SiGe HBTs have smaller junction dimensions and smaller extrinsic parasitics. Consequently, digital circuit speed in SiGe and InP has been comparable,[2] with SiGe offering higher integration scales. Further reduction of parasitics in InP HBTs is therefore important. The base-collector capacitance C_{cb} contributes significantly to analog bandwidth and digital delay and must be reduced as InP HBTs are scaled. In small-junction-area HBTs used in low-power logic, the parasitic base interconnect pad capacitance becomes a significant fraction of the total C_{cb}. Several approaches have been pursued for eliminating this access pad capacitance.[3–7]

InP HBTs with implanted collectors are very promising as a manufacturable, high yield process and have demonstrated reduced C_{cb}.[5–7] In these processes, Si is selectively implanted into an undoped or SI InP layer to form a N^+ pedestal link[5,6] or a buried subcollector, respectively.[7] Outside the implanted regions, the depletion depth is increased and the extrinsic capacitance is reduced. The active HBT layers are then grown. However, exposed InP surfaces have donor-like charge states attributed to Si impurities.[8,9] HBTs reported in Ref. 5 also suffer from this process-dependent charge at the regrowth interface. This charge, if left uncompensated, results in incomplete depletion and hence no reduction in extrinsic C_{cb} at low bias voltages. Several methods have been utilized for reduction of this interface charge, including process related techniques,[9] annealing in a phosphine ambient,[8] and overgrowth of a p^+ charge compensation layer.[5] This interface charge is process dependent, and full compensation might not be possible with process techniques or a p^+ compensation layer.

To alleviate these problems, we demonstrate InP HBTs with implanted subcollectors wherein Fe implantation eliminates this interface charge and a selective, patterned Si implant forms the N^{++} subcollector. In addition to the reduced extrinsic C_{cb} associated with the elimination of the base access pad capacitance and compensation of charge at the epitaxial growth interface, this process provides increased wafer planarity and hence potentially improved yield in the fabrication of large circuits.

In the first demonstration of this double implanted process, the device gain, collector leakage current, and ideality factors are similar to a fully epitaxial standard mesa HBT.[10] The f_τ and f_{max} of 363 and 410 GHz, respectively, are the best reported for HBTs with implanted subcollectors. Prior to this work, the highest simultaneous f_τ and f_{max} reported for an InP HBT employing implantation to reduce C_{cb} were 240 and 310 GHz,[7] respectively.

The process flow of the implanted subcollector HBT with Fe is shown in Fig. 1. A semi-insulating InP substrate is implanted with Fe at 10 keV at a fluence of 2×10^{13} ions cm^{-2} [Fig. 1(a)]. The wafer is annealed at 700 °C for 5 min to activate the Fe, which is a midgap acceptor in InP.[11] The Fe implant conditions are selected to fully compensate the N-type charge at the growth interface between the substrate and collector epitaxial layers over the observed $(1-5)\times10^{12}$ cm^{-2} range of regrowth interface charge densities. In order to ensure complete charge depletion at the regrowth interface in the region under the base pad contact area,

$$n_{Fe} \geqslant n_s + \frac{N_c T_c}{2} - \frac{(V_{cb}+V_{bi})\varepsilon}{qT_c}, \quad (1)$$

where n_{Fe} is the density of Fe in cm^{-2}, n_s is the regrowth interface charge density, N_c is the doping in the drift collector, T_c is the thickness of the drift collector, V_{bi} is the built-in potential of the basecollector junction, and V_{cb} is the base-collector reverse bias voltage.

The sample is then selectively implanted [Fig. 1(b)], using SiN_x as the implant mask, with Si at 200 keV/4×10^{14} ions cm^{-2}, 40 keV/7×10^{13} ions cm^{-2}, and 10 keV/3×10^{13} ions cm^{-2}, and then activated by annealing at 800 °C/30 s.[12] The Si implant dose is much larger than the Fe acceptor density (n_{Fe}) in the selectively implanted region. This ensures that a highly N^{++} doped, isolated sub-

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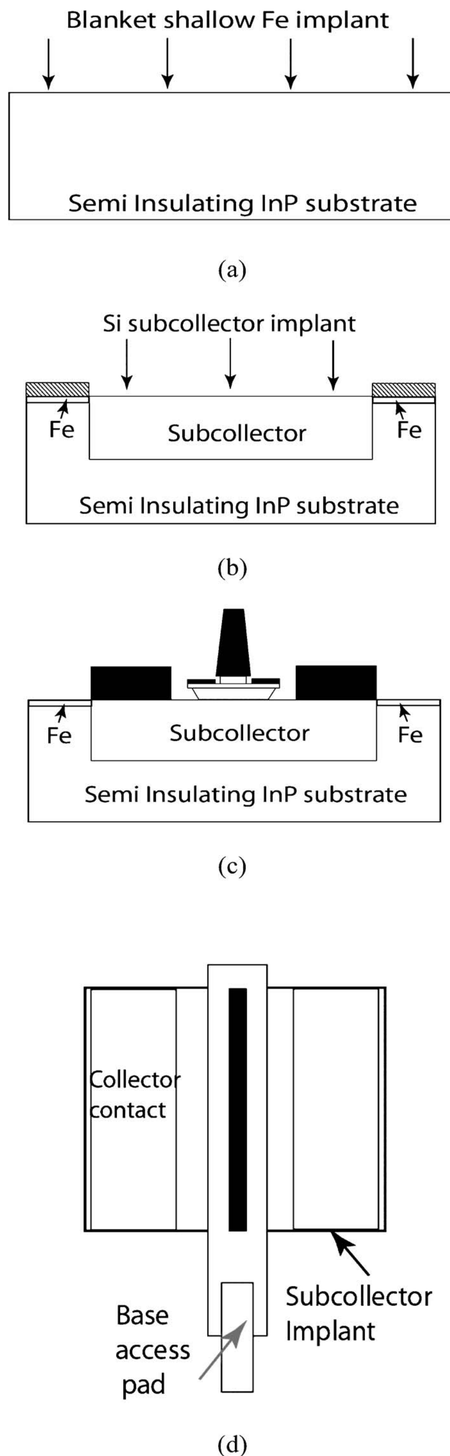

FIG. 1. Implanted subcollector process cross section: (a) blanket shallow Fe implant to suppress interface, (b) Si implant to form the subcollector, (c) active HBT layers are grown and device is formed, and (e) top view of implanted subcollector DHBT.

collector region [Fig. 1(b)] is formed. The base access pad [Fig. 1(d)] lies outside the subcollector implant boundary and, in the absence of interface charge, does not contribute to C_{cb}.

A test wafer is coprocessed without the blanket Fe implant to observe the effect of uncompensated charge. This process is otherwise identical to the one described above.

The active InP HBT layers are then grown by molecular-beam epitaxy (MBE). The device N^- drift collector, base, and emitter layers for both wafers are identical to that reported in Ref. 10. Growth is initiated with a 3.5 nm undoped InGaAs etch-stop layer between the InP collector and the InP substrate. The N^- drift collector, base, and emitter layers are grown, and devices are formed[10] by wet etching the emitter and base mesas. With the selectively implanted subcollector, HBT isolation does not require a mesa etch, reducing the HBT mesa height by ~500 nm.

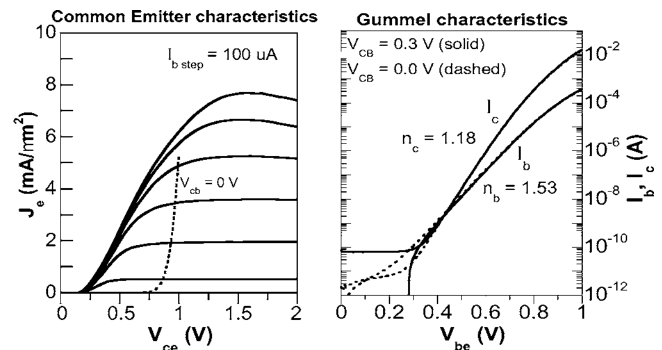

FIG. 2. Common-emitter *I-V* and forward Gummel characteristics. Device dimensions: $A_{je}=0.65\times4.3\ \mu\text{m}^2$.

For the implanted HBT with the blanket Fe implant, standard transmission line measurements (TLM) show the base sheet resistivity $\rho_s\approx1050\ \Omega/\text{sq}$ and contact resistivity $\rho_c\approx30\ \Omega\ \mu\text{m}^2$. The emitter contact resistivity ρ_c determined from RF parameter extraction is $\approx15\ \Omega\ \mu\text{m}^2$. From TLMs and Hall measurements, the subcollector sheet resistance ρ_s is $\approx25\ \Omega/\text{sq}$. The collector contact is made to N^{++} InP and partially annealed (Ni/Ge/Au/Ni/Au, 320 °C/60 s). The anneal temperature was kept low because higher temperature anneals greatly increased the base ρ_c on test samples. Consequently, the collector ρ_c is very high at $\approx300\ \Omega\ \mu\text{m}^2$. The HBTs have dc current gain $\beta\approx40$, common-emitter and common-base breakdown voltages $BV_{ceo}=4.9$ V and $BV_{cbo}=5.4$ V (at $I_c=50\ \mu$A), collector and base ideality factors $n_c=1.18$ and $n_b=1.53$, and low collector leakage current $I_{cbo}<70$ pA (at an applied $V_{cb,offset}=0.3$ V). Figure 2 shows the common-emitter DC and Gummel characteristics. The device β, ideality factors, and collector leakage current are consistent with those measured from the triple mesa HBT equivalent.[10] Leakage between adjacent HBTs at 5 μm separation was ~10 pA/μm at 3 V bias, indicating good device isolation.

DC 45 GHz *S*-parameter measurements are carried out after performing an off wafer line-reflect-reflect-match calibration on an Agilent 8510C network analyzer. Device data

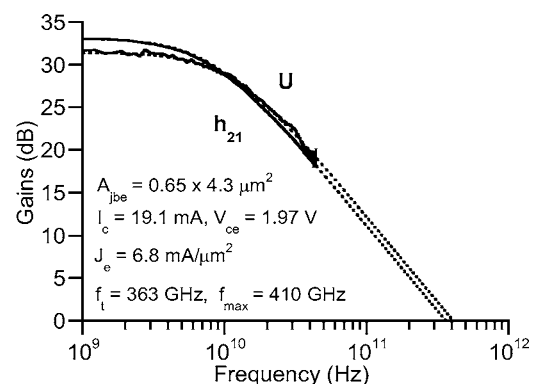

FIG. 3. Measured microwave gains H_{21} and Mason's unilateral power gain U at a bias associated with peak f_τ and f_{max}.

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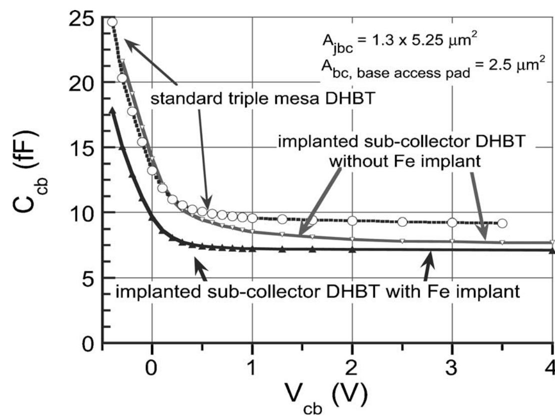

FIG. 4. Variation of C_{cb} with V_{cb} at I_c=0 mA for standard triple mesa HBT,[10] implanted subcollector HBTs with shallow Fe implant, and implanted subcollector HBTs without Fe. Junction areas and epitaxial layer structures (drift collector, base, and emitter) of the HBTs are identical.

are deembedded from probe pad parasitics. A maximum 363 GHz f_τ and 410 GHz f_{max} (Fig. 3) is demonstrated at I_c=19.1 mA and V_{ce}=1.97 V (J_e=6.83 mA/μm^2). The f_τ and f_{max} are determined from an extrapolation through a least-squares fit between the single-pole transfer functions for H_{21} and U to the measured data at the frequencies measured.[10] This HBT has a 0.6×4.3 μm^2 emitter semiconductor junction area and 1.3 μm base mesa width. The subcollector stripe as defined on the photomask extends ~0.5 μm beyond the length of the emitter junction.

Figure 4 compares the variation of C_{cb} vs V_{cb} (at J_e =0 mA/μm^2) between the implanted subcollector HBT with shallow Fe implant, the implanted subcollector HBT without Fe implant, and a standard triple mesa HBT,[10] all with a similar 120 nm thick drift collector. At low bias voltages, the C_{cb} of the implanted subcollector HBT without the Fe implant is similar to that of the triple mesa HBT. This suggests the presence of an undepleted sheet charge at the regrowth interface in the contact pad region. The implanted subcollector HBT with shallow Fe implant exhibits lower C_{cb} over the entire measured range of bias voltages bias. The compensation of interface charge by the shallow Fe implant is thus evident. At ~0.6 V reverse bias the collector is fully depleted and C_{cb} is ~23% smaller than that measured for the mesa HBT. This capacitance reduction corresponds well to the fractional area of the base access pad. From Eq. (1), the regrowth interface charge is depleted when

$$V_{cb} + V_{bi} \geqslant \frac{qT_c(n_s - n_{Fe})}{\varepsilon} + \frac{qN_cT_c^2}{2\varepsilon}.$$

The above equation indicates that larger bias voltage (V_{cb}) is required to fully deplete the interface charge under the base pad when this charge is not compensated. This is evident from Fig. 4 where a high base-collector bias voltage (>3 V) is required to fully deplete the uncompensated interface charge on the implanted subcollector HBT without the Fe implant.

The f_τ and f_{max} are lower than the triple mesa HBT.[10] We attribute this to higher base resistance and larger collector series resistance of ~20 Ω. The high collector resistance which is also evident from the I_C-V_{CE} characteristics is due to insufficient annealing of the alloyed collector ohmic contacts to N^{++} InP. The collector ohmic contact process is being revised to reduce the collector contact resistivity.

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