Indium Phosphide and Related Materials - 2006

Selectively implanted subcollector DHBTs

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Outline

- Motivation
- InP HBTs: solutions towards the future
    1. ***Implanted Subcollector HBTs***
    2. ***Pedestal-Subcollector HBTs***
- Conclusions

Why are fast transistors required?

Fiber Optic Communication Systems

40 Gb/s commercially available
80 and 160 Gb/s(?) long haul links

High speed Instrumention

mixed-signal ICs with large dynamic range

mm-Wave Wireless Transmission

high frequency communication links,
atmospheric sensing, military and commercial radar

Some common figures of merit

f_t is the unity current gain frequency

$$\frac{1}{2\pi f_t} = \tau_{base} + \tau_{collector} + RCs\ldots$$

f_{max} is the power gain cut-off frequency

$$f_{\max} \cong \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cbi}}}$$

Digital delay not well correlated with τ_F

$(V_{LOGIC}/I_c)\ (C_{cb})$ is a major delay

$$\Rightarrow \frac{C_{cb}}{I_C} \propto \left(\frac{A_{\text{COLLECTOR}}}{A_{\text{EMITTER}}}\right) T_c$$

Collector Base capacitance
must be reduced

InP vs Si/SiGe HBTs

InP system has inherent material advantages over Si/SiGe

20x lower base sheet resistance,
5x higher electron velocity,
4x higher breakdown-at same f_t.

but…

today's SiGe HBTs are fast catching up due to 5x smaller scaling and offer much higher levels of integration due to the Si platform

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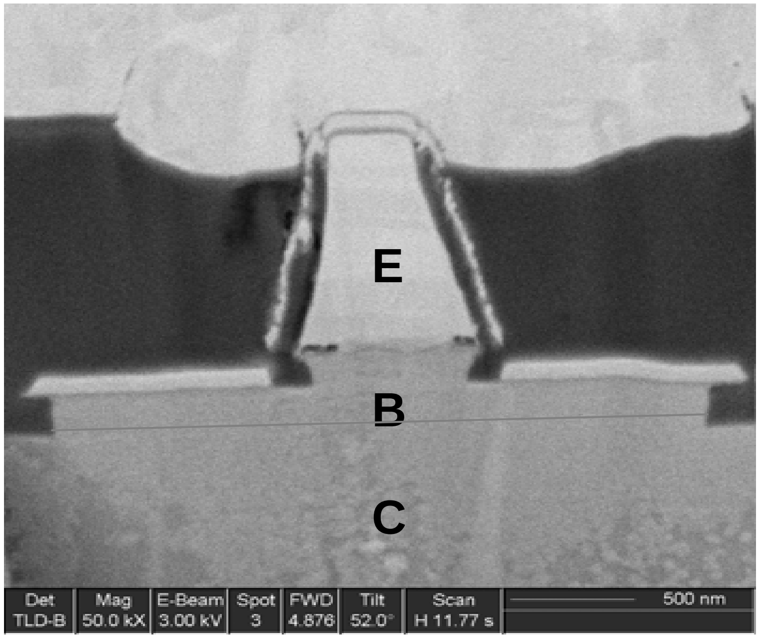
Scaling Laws for HBTs

Reduce vertical dimensions to decrease transit times

Reduce lateral dimensions to decrease RC time constants

Increase current density to decrease charging time

InP HBTs today… and tomorrow?



- Parasitic base collector capacitance under base contacts
- Base ohmic transfer length limits collector scaling
- Non-planar device

Key Challenges for InP HBTs

- *Scaling of collector-base junction*
- *Planar, manufacturable process for high levels of integration*
- *Narrow base-emitter junction formation and also low R_{ex}*

A Radical approach is necessary

The end goal: SiGe-like highly scaled InP HBT

Objectives:

Extreme parasitic reduction: speed

Planar Geometry: yield

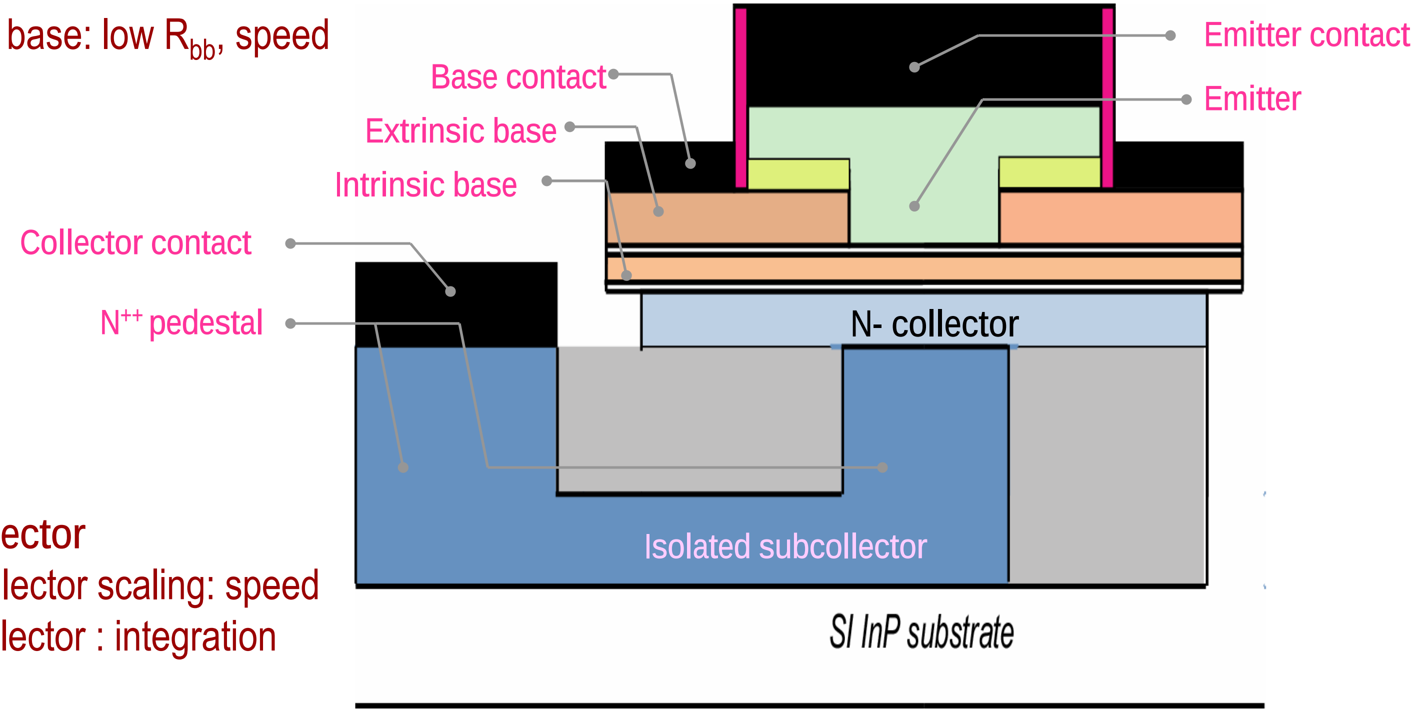
Regrown submicron emitter

submicron emitter scaling: speed

large emitter contact: low R_{ex}, speed

Extrinsic base

thick extrinsic base: low R_{bb}, speed



Pedestal collector

submicron collector scaling: speed

One sided collector : integration

MODULE 2

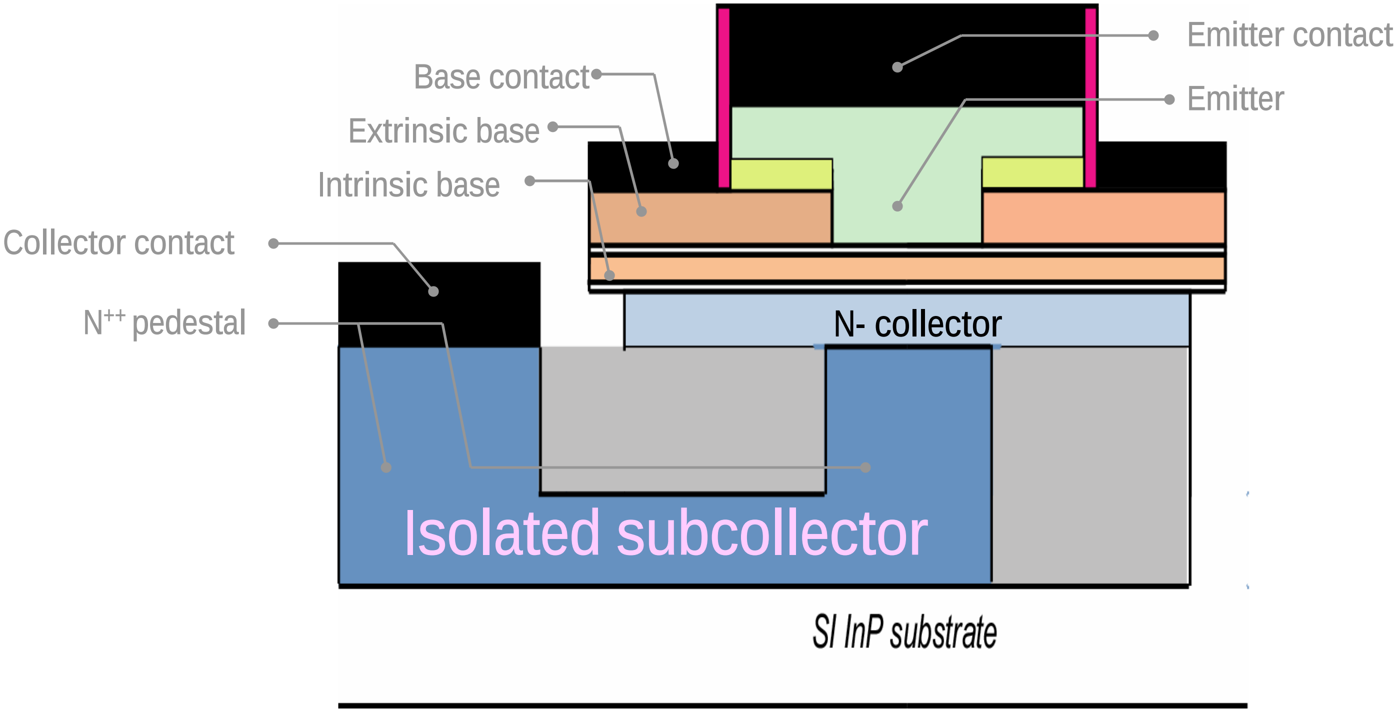
Isolated subcollector

large base pad: yield

zero base pad capacitance: speed

MODULE 1

The end goal: SiGe-like highly scaled InP HBT

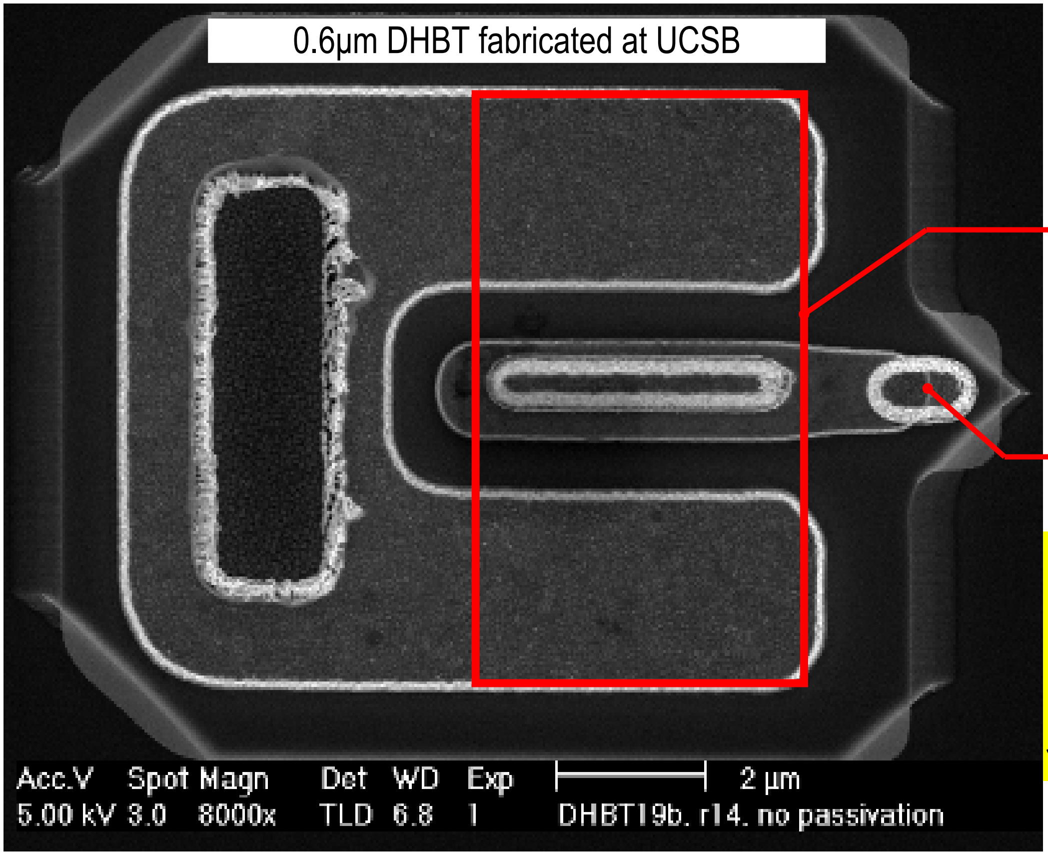


Isolated subcollector

zero base pad capacitance: speed

← **MODULE 1**

Module 1: Access Pad Capacitance in InP HBTs



Subcollector boundary

Parasitic Base access pad

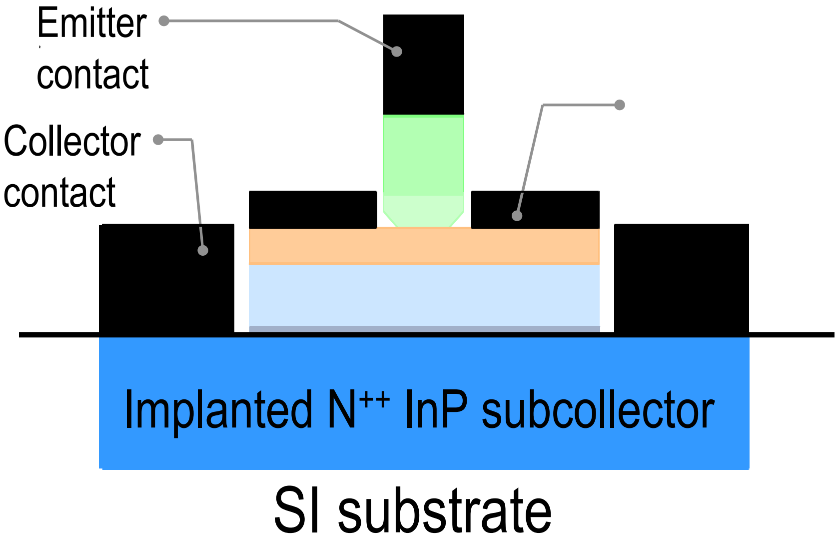
- *$C_{cb,\ pad}$ ~30% of overall C_{cb}*
- *Increasingly significant for short emitter lengths*

IMPORTANT FOR FAST, LOW POWER LOGIC

Implanted subcollector InP DHBTs

Approach

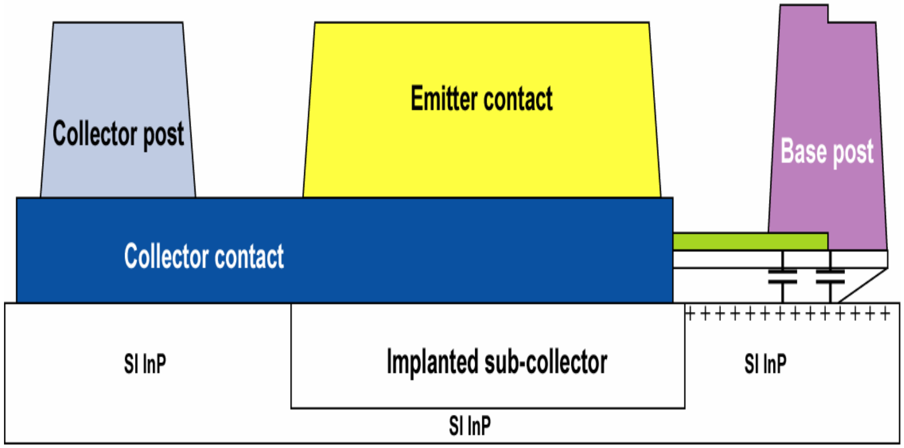
- Selectively implanted N^{++} subcollector
- Growth of drift collector, base & emitter
- Device formation



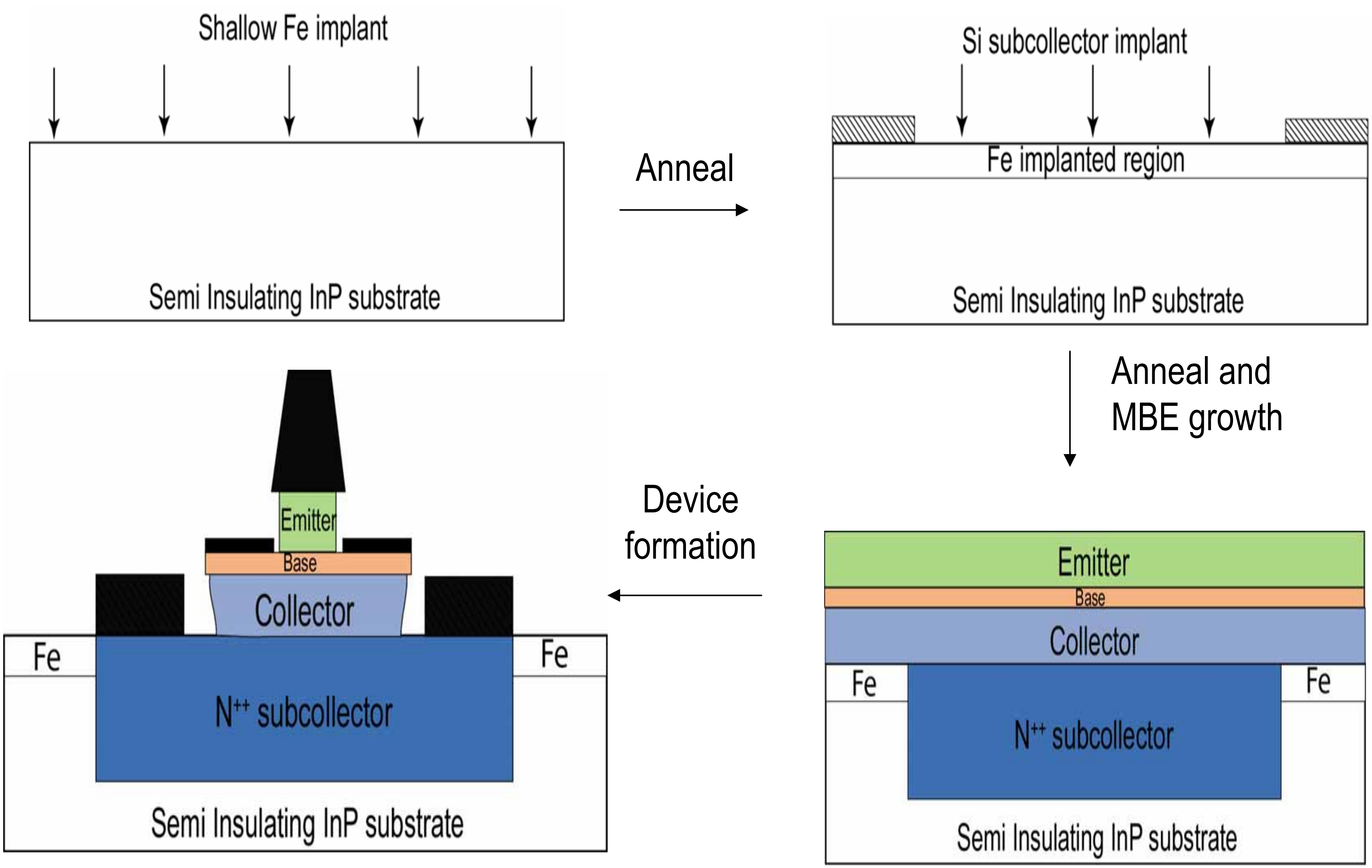
Side View

Interface charge compensation

- N^{++} charge present on exposed InP surface
- Fe implant suppresses interface charge



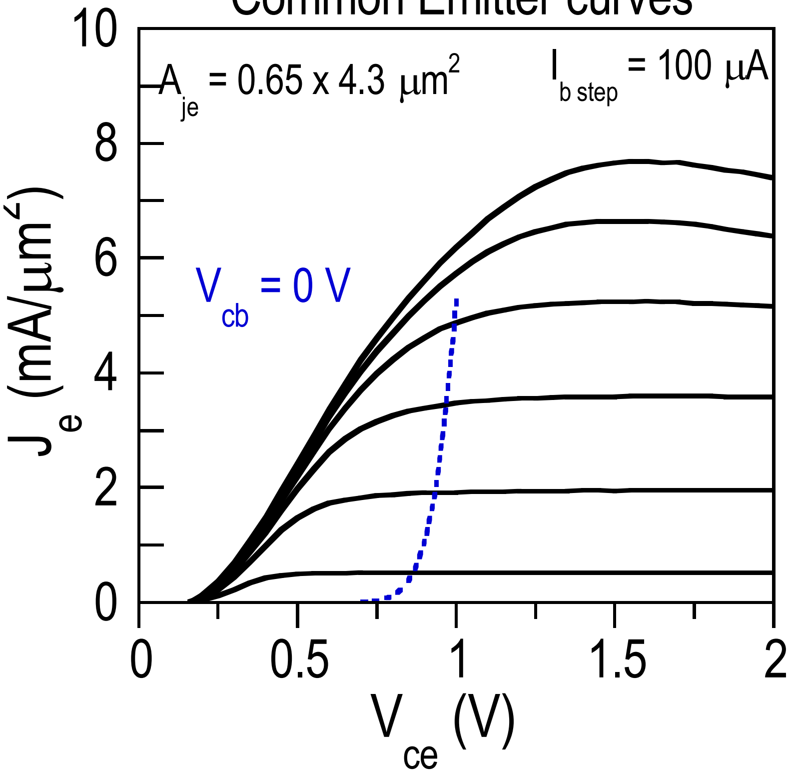
Implanted subcollector DHBT with Fe : The Process



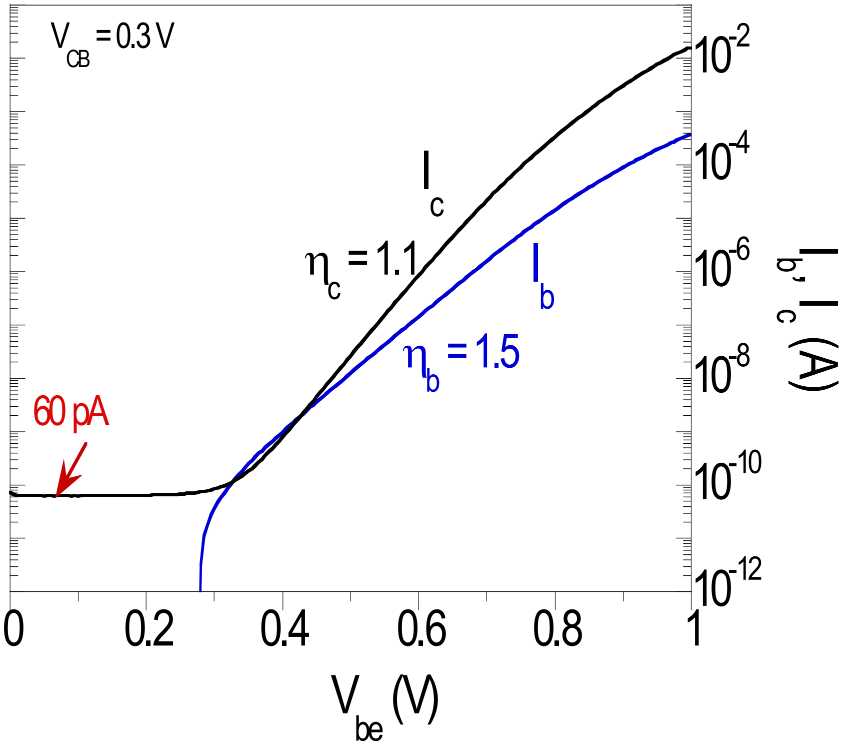
Implanted subcollector DHBTs with Fe – DC results

DC characteristics - Gain, Ideality factors, Leakage currents…are similar to fully epitaxial device

Common Emitter curves



Gummel characteristics



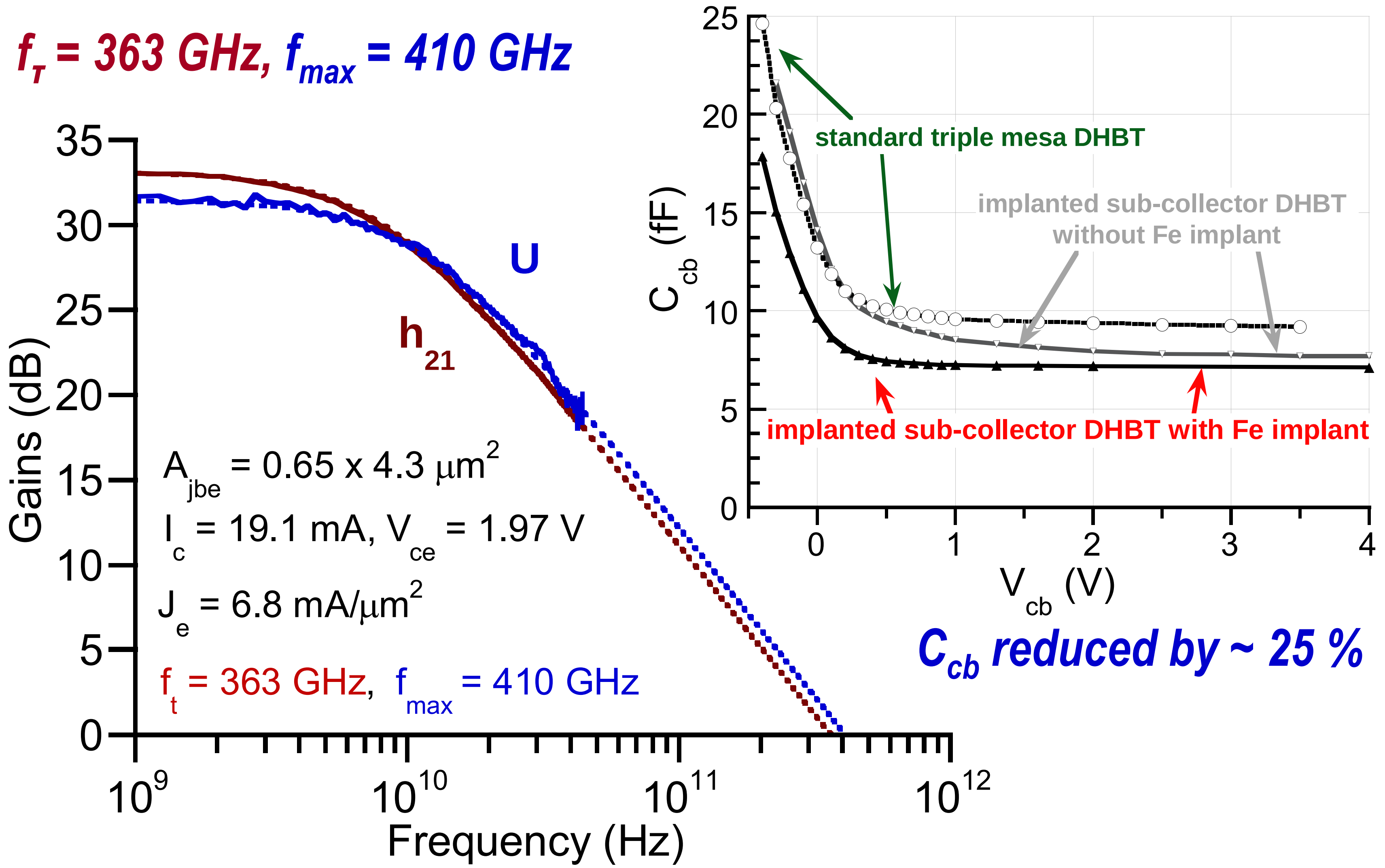
Peak β ≈ 35, BV_{CBO} = 5.31V (I_c=50 μA)

Base (from TLM) : R_{sheet} = 1050 Ω/sq, R_{cont} = 50 Ω·μm^2

Collector (from TLM) : R_{sheet} ~ 25.0 Ω/sq, R_{cont} ~ 110 Ω·μm

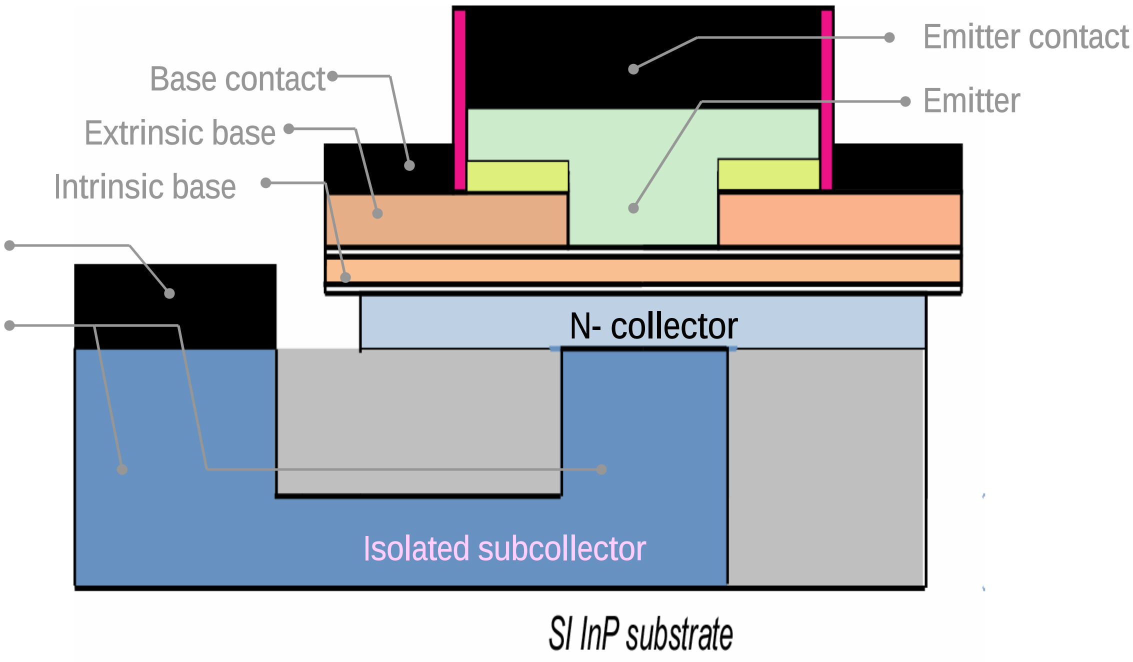
Implanted subcollector DHBTs with Fe – RF results

f_T = 363 GHz, f_{max} = 410 GHz



C_{cb} reduced by ~ 25 %

Module 2: Submicron collector scaling



Pedestal collector
submicron collector
scaling: speed

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MODULE 2

Isolated subcollector
large base pad: yield
zero base pad capacitance: speed

← ***MODULE 1***

An elegant approach to collector scaling

The triple implanted subcollector-pedestal HBT

Approach

1. deep N^{++} InP subcollector by selective Si implant

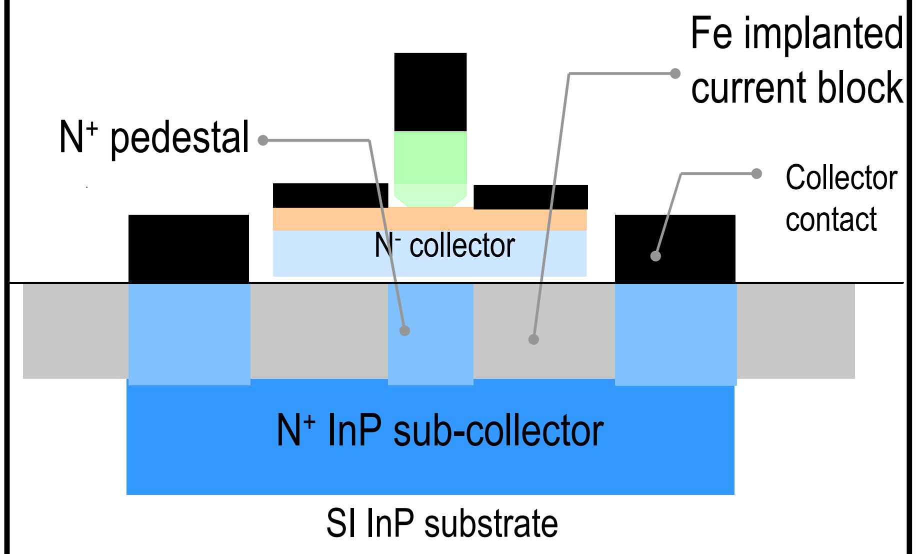
   → isolate base pad (Module 1)

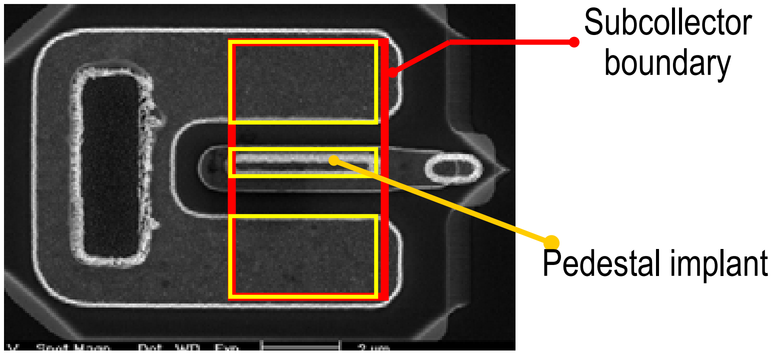
2. SI layer ~0.2µm, by Fe implant

   → decrease extrinsic C_{cb}

3. Second Si implant creates N^{++} pedestal for current flow
4. Growth of drift collector, base & emitter and device formation

N. Parthasarathy et al., Electron Device Letters, Vol. 27(5), May 06



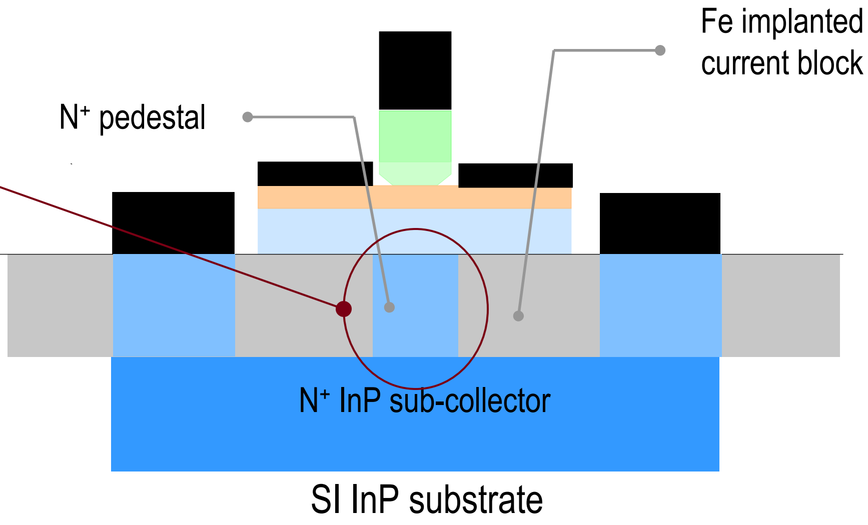


An elegant approach to collector scaling

The triple implanted subcollector-pedestal HBT

Advantages over standard mesa device

1. Collector Base junction can be independently scaled
2. Pad capacitance eliminated
3. Increased Breakdown voltages

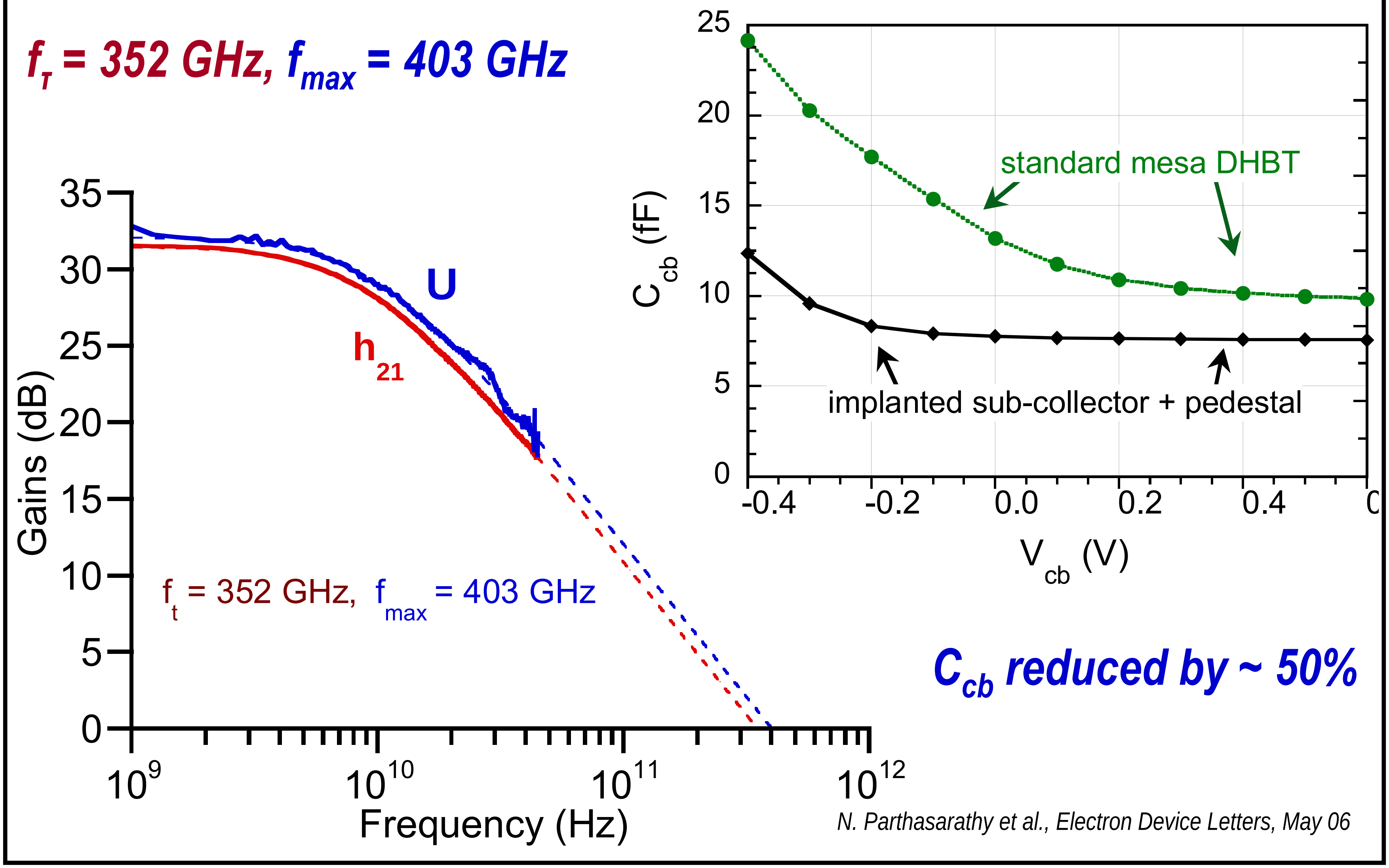


More benefits....

4. Highly planar, fully implanted process, no regrowth required → manufacturability
5. Implants before growth endless variations in subcollector-pedestal layers without compromising device planarity
6. Fe compensates interface charge → reliability and repeatability

RF performance: fully implanted subcollector-pedestal HBT

f_T = 352 GHz, f_{max} = 403 GHz



C_{cb} reduced by ~ 50%

N. Parthasarathy et al., Electron Device Letters, May 06

Conclusion

Implanted collector InP HBTs at 500 nm scaling generation ~ 400 GHz f_t & f_{max}

- Implanted subcollector DHBTs – eliminate pad capacitance
- Implanted pedestal-subcollector DHBTs – independent collector scaling

InP HBT future: 125 nm scaling generation with implanted pedestal-subcollectors

~1 THz f_t & f_{max}, 400 GHz digital latches & 600 GHz amplifiers?

Applications

160+ Gb/s fiber ICs, 300 GHz MMICs for communications, radar, & imaging

& applications unforeseen & unanticipated

"The principal applications of any sufficiently new and innovative technology always have been – and will continue to be – applications created by that technology."

-Kroemer's Lemma of New Technology