G-Band (140–220 GHz) and W-Band (75–110 GHz) InP DHBT Medium Power Amplifiers

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Abstract—We report common-base medium power amplifiers designed for G-band (140–220 GHz) and W-band (75–110 GHz) in InP mesa double HBT technology. The common-base topology is preferred over common-emitter and common-collector topologies due to its superior high-frequency maximum stable gain (MSG). Base feed inductance and collector emitter overlap capacitance, however, reduce the common-base MSG. A single-sided collector contact reduces C_{ce} and, hence, improves the MSG. A single-stage common-base tuned amplifier exhibited 7-dB small-signal gain at 176 GHz. This amplifier demonstrated 8.7-dBm output power with 5-dB associated power gain at 172 GHz. A two-stage common-base amplifier exhibited 8.1-dBm output power with 6.3-dB associated power gain at 176 GHz and demonstrated 9.1-dBm saturated output power. Another two-stage common-base amplifier exhibited 11.6-dBm output power with an associated power gain of 4.5 dB at 148 GHz. In the W-band, different designs of single-stage common-base power amplifiers demonstrated saturated output power of 15.1 dBm at 84 GHz and 13.7 dBm at 93 GHz.

Index Terms—InP heterojunction bipolar transistor, millimeterwave amplifier, monolithic microwave integrated circuit (MMIC) amplifiers.

I. INTRODUCTION

PAND (75–110 GHz) and G-band (140–220 GHz) amplifiers have applications in wide-band communication systems, atmospheric sensing, and automotive radar. The high mobility of InGaAs, high electron saturation velocity of InP, and submicrometer scaling result in wide-bandwidth transistors with high available gain in this frequency band. In a transferred substrate InP HBT process, 6.3-dB gain is reported at 175 GHz with a single-stage amplifier [1]. State-of-the-art results in InP high electron-mobility transistor (HEMT) technologies include a three-stage amplifier with 30-dB gain at 140 GHz [2], a three-stage amplifier with 12–15-dB gain from 160 to 190 GHz [3], and a three-stage power amplifier with 10-dB gain from 144 to 170 GHz [4].

Manuscript received April 21, 2004; revised July 24, 2004. This work was supported in part by the Office of Naval Research under Grant N00014-04-1-0071. A portion of this work was carried out at the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, under a contract with the National Aeronautics and Space Administration.

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Digital Object Identifier 10.1109/TMTT.2004.840662

Recent research in a scaled InP/InGaAs/InP mesa double HBT (DHBT) with a 30-nm carbon-doped InGaAs base with a graded base doping and 150 nm of total depleted collector thickness achieved wide-bandwidth transistors with 370 GHz f_t and 459 GHz $f_{\rm max}$ [5], [6]. In this paper, we describe how this technology is used to realize several power amplifiers in the 75–220-GHz frequency range.

II. InP DHBT PROCESS

The transistors in the circuit are formed from a molecular beam epitaxy (MBE) layer structure with a highly doped 35-nm InGaAs base and a 210-nm collector and are fabricated in a triple-mesa process with both active junctions defined by selective wet etch chemistry. The increased collector thickness over [5] and [6] is intended to maintain high $f_{\rm max}$ despite increases in device critical dimensions, motivated by the desire for improved transistor yield. Polyimide passivates and planarises the devices. One level of deposited metal forms circuit interconnects and electrical contacts to transistors and resistors. SiN metal-insulator-metal (MIM) capacitors and coplanar-waveguide (CPW) transmission lines are employed to synthesize the tuning elements. Plated air bridges bridge the ground planes and suppress the CPW slot-line modes.

III. AMPLIFIER DESIGN

A. Models and Simulations

The transistor SPICE model parameters used in the simulations are extracted from the measured two-port S-parameters. The amplifiers are simulated using the Advanced Design System software of Agilent Technologies, Palo Alto, CA. A planar method-of-moments electromagnetic (EM) simulator (Momentum) modeled the CPW structures and the MIM capacitors.

B. Transistor Characteristics

The dc common-base characteristics of a two-finger 0.7 μ m × 11 μ m InP common-base power DHBT is shown in Fig. 1. The common-base breakdown voltage $(V_{\rm br,cb0})$ is more than 7 V (Fig. 2). The feasible $(I_c,V_{\rm ce})$ load line is, however, constrained by the device safe operating area (Fig. 1), as determined by both breakdown voltage and thermal resistance. The devices have shown 240 GHz f_t and 290 GHz $f_{\rm max}$ when biased at 3 mA/ μ m² current density and 1.7 V $V_{\rm ce}$ (Fig. 3). The degradation in $f_{\rm max}$ relative to [5] is

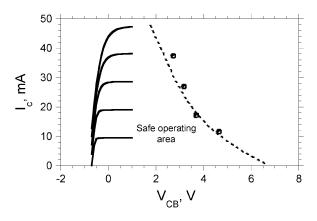


Fig. 1. Common-base dc characteristics of a two-finger 0.7 $\mu\,\mathrm{m}\times11~\mu\,\mathrm{m}$ common-base DHBT.

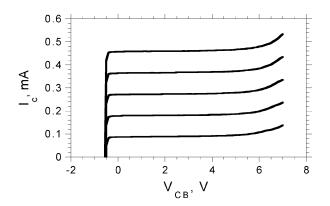


Fig. 2. Common-base dc characteristics of a two-finger 0.7 $\mu\,\mathrm{m}\times11~\mu\mathrm{m}$ common-base DHBT.

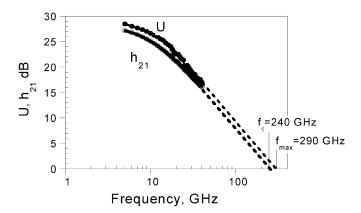


Fig. 3. Short-circuit current gain and Mason's gain as a function of frequency of a single-finger 0.7 μ m \times 7 μ m common-emitter DHBT.

due to a wider base mesa intended to improve yield and due to relatively poor base ohmic contacts in this process run.

C. Transistor Layout Parasitics

The common-base topology is chosen as it has higher maximum stable gain (MSG) in this band when compared to the common-emitter and common-collector topologies (Fig. 4). At present, however, we ignore both base feed inductance L_b and collector–emitter overlap capacitance $C_{\rm ce}$. At 180 GHz, the common-base topology exhibits 10-dB MSG, while the common-emitter and common-collector topologies exhibit 4

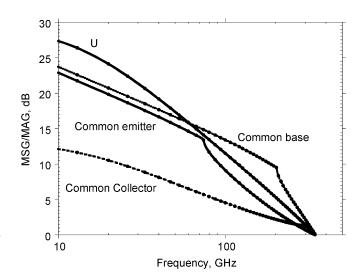


Fig. 4. Comparison of MSG/MAG of common-base, common emitter, and common collector configuration of an InP DHBT. L_b and $C_{\rm ce}$ are omitted.

and 3 dB, respectively. Since power amplifiers use large-signal load match, rather than a small-signal output match, the gain falls below the MSG.

The above comparison between different configurations ignores the effect of L_b and C_{ce} . While these parasitics reduce the common-base MSG, in the G-band, the common-base topology still provides the highest gain when compared to the common-emitter and common-collector configurations. If not modeled in the designs, L_b and C_{ce} could potentially cause instability. Base inductance is due to the long thin base contact metal stripes on either side of the emitter [see Fig. 5(a)]. Loop inductance depends upon the current return path; this is difficult to identify in the transistor geometry, hence, L_b is not readily modeled with accuracy. This creates uncertainty in the stability analysis. S-parameter extractions indicate approximately 3-pH base feed inductance per 12- μ m-long emitter finger having 0.8- μ m base contact width. The collector-to-emitter overlap capacitance (C_{ce}) also reduces MSG. C_{ce} is the capacitance between the emitter interconnect metal and the collector ohmic contact metal [see Fig. 5(a) and (b)]. These metals are separated by ~400-500-nm polyimide. This thickness varies in our process, rendering C_{ce} variable. Degradation in MSG/maximum available gain (MAG) of a common-base topology due to layout parasitics L_b and C_{ce} of an InP DHBT with double-sided collector contacts is shown in Fig. 6. Potential instability in the small-signal characteristics due to L_b and C_{ce} was observed in the first-generation amplifiers fabricated. In second-generation designs, the collector-to-emitter overlap capacitance was significantly reduced by employing single-sided collector contacts as opposed to double-sided collector contacts (Fig. 7). In addition to reducing C_{ce} , this also increases the collector resistance and, thus, further improves circuit stability. NiCr resistors provide additional resistive stabilization in some designs.

D. Circuit Design

Fig. 8 shows a single-stage amplifier circuit schematic. Shunt capacitors are either SiN_x MIM capacitors or CPW open-circuit stubs. Two-stage amplifiers (Fig. 9) are formed by cascading

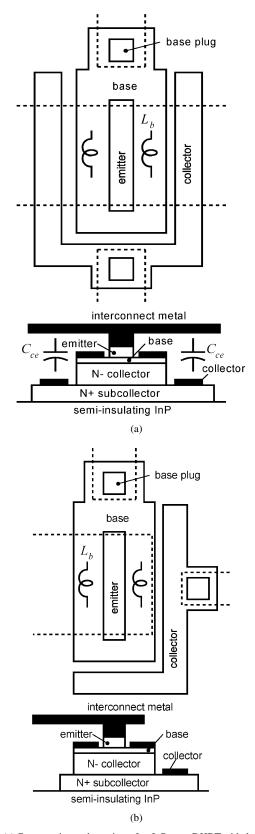


Fig. 5. (a) Cross section and top view of an InP mesa DHBT with double-sided collector contacts. (b) Cross section and top view of an InP mesa DHBT with single-sided collector contacts.

two identical single-stage designs. The output of the first stage is large-signal matched to the second stage input, avoiding first-stage premature power gain compression.

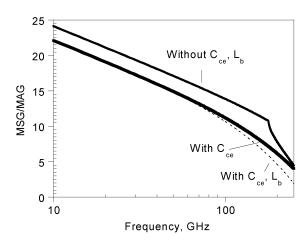


Fig. 6. Comparison of common-base MSG/MAG with and without layout parasitics. The InP DHBT has a double-sided collector contact.

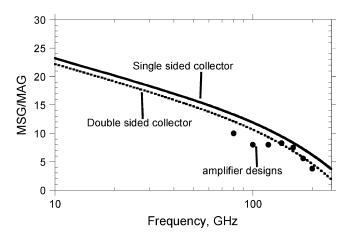


Fig. 7. Comparison of MSG/MAG of common-base HBT with single-sided collector contact and double-sided collector contacts. The design values of the power-amplifier gains are also shown.

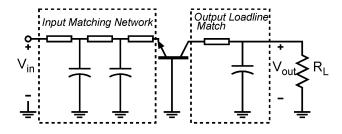


Fig. 8. Single-stage common-base amplifier.

IV. MEASUREMENTS

A. Small-Signal Measurements

G-band amplifiers are measured on wafer using an HP 8510C vector network analyzer (VNA) with Oleson Microwave Laboratories' Millimeter Wave VNA extensions. The test-set extensions are connected to GGB Industries coplanar wafer probes via WR-5 waveguides. The amplifier measurements are calibrated using off-wafer thru-reflect line (TRL) calibration standards. W-band amplifier small-signal gains and return losses were measured on-wafer using a W-band Agilent 8510 network analyzer calibrated with an off-wafer calibration using TRL calibration standards.

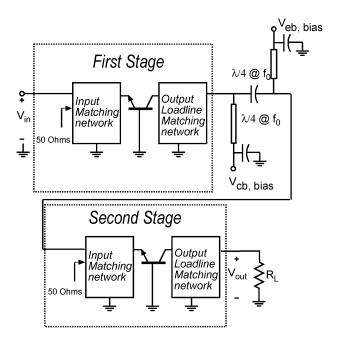


Fig. 9. Two-stage common-base amplifier.

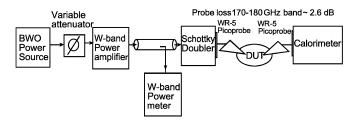


Fig. 10. 170-180-GHz power measurement setup.

B. 172–180-GHz Power Measurements

G-band power measurements were performed at the Jet Propulsion Laboratory (JPL), California Institute of Technology, Pasadena. The 170–180-GHz power measurement setup is shown in Fig. 10. W-band power from a backward wave oscillator (BWO) power source is amplified and is doubled in frequency using a Schottky diode frequency doubler. The frequency-doubler output drives the input of the device-under-test (DUT). The DUT output power is measured using a calorimeter. Since the input and output power are measured at separate times, the saturated power-gain measurements are subject to approximately ± 1 -dB drift in gain. The saturated output power measurement is not subject to this drift, and we estimate the output power data is accurate to ± 0.5 dB. Data is corrected for measured probe attenuation.

C. 148–152-GHz Power Measurements

The 148–152-GHz measurement setup is shown in Fig. 11. A 150-GHz Gunn oscillator drives the DUT. A variable attenuator adjusts the input power.

D. 75–110-GHz Power Measurements

The 75–110-GHz power measurement setup is shown in Fig. 12. The output of a dc–40-GHz frequency synthesizer is

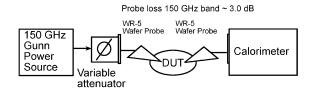


Fig. 11. 148–152-GHz power measurement setup.

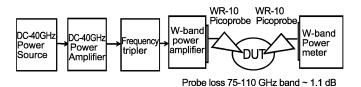


Fig. 12. 75-110-GHz power measurement setup.

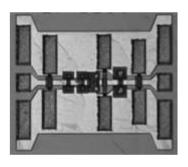


Fig. 13. Die photograph of the single-stage common-base monolithic-microwave integrated-circuit (MMIC) amplifier centered at 176 GHz. This measures $0.36~\text{mm} \times 0.3~\text{mm}$.

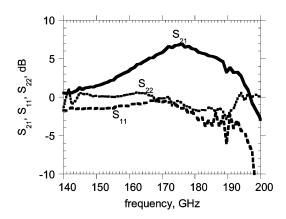


Fig. 14. Measured S-parameters of the 176-GHz single-stage amplifier.

amplified and tripled in frequency to 75–110 GHz. This signal is further amplified to drive the DUT input. The DUT output power is measured using a W-band power sensor.

V. RESULTS

A. 176-GHz Single-Stage Amplifier

A die photograph is shown in Fig. 13. The transistor has two separate 0.8 $\mu \rm m \times 12~\mu m$ fingers. The amplifier bandwidth is limited by the output tuning network. The transistor output is large-signal load-line matched for maximum saturated output power, as opposed to a small-signal match for maximum gain. This amplifier exhibited 7-dB small-signal gain at 176 GHz when biased at $I_c=30~\rm mA$ and $V_{\rm cb}=1.0~\rm V$ (Fig. 14).

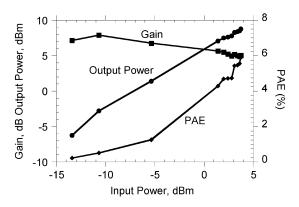


Fig. 15. Output power, power-added efficiency (PAE) versus input power of the 176-GHz single-stage amplifier at 172 GHz.

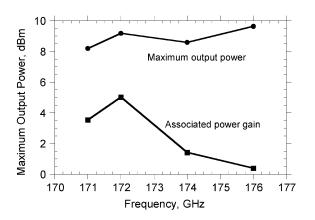


Fig. 16. 176-GHz amplifier saturated output power as a function of frequency.

This medium power amplifier is designed to obtain 16.5-dBm saturated output power at 180 GHz when biased at $I_c=30~\rm mA$ and $V_{\rm cb}=2.5~\rm V$. The output power versus input power characteristic is shown in Fig. 15. The amplifier exhibited a saturated output power of 8.77 dBm with an associated power gain of 5 dB at 172 GHz when biased at $I_c=40~\rm mA$ and $V_{\rm cb}=2.06~\rm V$. This medium power amplifier demonstrated >8-dBm saturated output power between 172–176 GHz (Fig. 16). The circuit exhibited 7.9-dB uncompressed gain under the above conditions at 172 GHz. Measured S-parameter data exhibits potential instability in the 140–170-GHz range due to feedback parasitics L_b and $C_{\rm ce}$.

B. 165-GHz Single-Stage Amplifier

A second single-stage common-base amplifier (Fig. 17) exhibited 6.5-dB small-signal gain at 165 GHz (Fig. 18) when biased at $I_c=31$ mA and $V_c=1.0$ V. This amplifier's small-signal gain is >3 dB between 152–180 GHz. The transistor has two separate 0.8 μ m \times 12 μ m fingers.

This medium power amplifier exhibited 8.3 dBm saturated output power with 4.5-dB associated power gain at 172 GHz (Fig. 19) when biased at $I_c = 47$ mA and $V_c = 2.1$ V.

C. 176-GHz Two-Stage Amplifier

A die photograph is shown in Fig. 20. This amplifier is a cascaded version of two individual amplifiers designed for $50-\Omega$

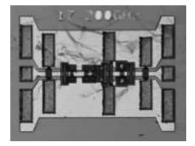


Fig. 17. Die photograph of a 165-GHz amplifier.

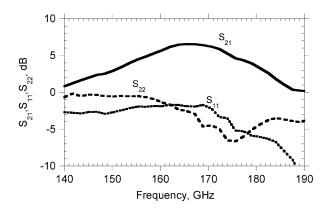


Fig. 18. S-parameters of a 165-GHz single-stage amplifier.

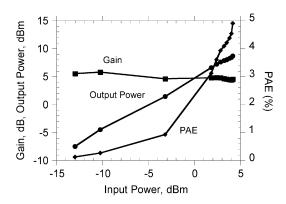


Fig. 19. Output power: PAE versus input power of the 165-GHz single-stage amplifier.

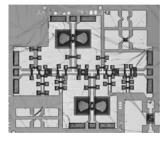


Fig. 20. Die photograph of a 176-GHz two-stage MMIC amplifier. This measures 1 mm $\times\,0.7$ mm.

input resistance and 50- Ω load. Each stage employs two separate 0.8 μ m \times 12 μ m HBT fingers. The small-signal measurements are performed with the first stage biased at $I_c=25$ mA and $V_{\rm cb}=1.0$ V and the second stage biased at $I_c=30$ mA and $V_{\rm cb}=1.0$ V. Small-signal measurements indicate 7-dB gain at

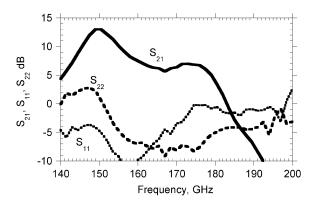


Fig. 21. Small-signal measurements of the 176-GHz two-stage amplifier.

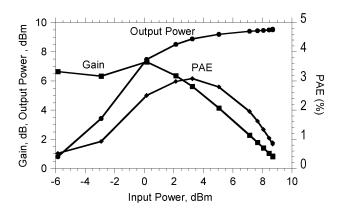


Fig. 22. Power measurements of the 176-GHz two-stage amplifier.

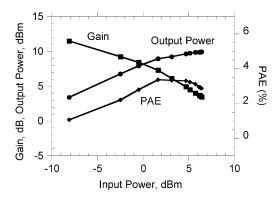


Fig. 23. Power measurements of the 176-GHz two-stage amplifier at $150.2\,\mathrm{GHz}$.

176 GHz and 13-dB gain at 150 GHz. There is a potential instability in S_{22} in 140–150-GHz range (Fig. 21).

This amplifier exhibited 8.1-dBm output power with 6.35-dB associated power gain at 176 GHz and demonstrated 9.1-dBm saturated output power (Fig. 22). These measurements are performed with the first stage is biased at $I_c=45~\rm mA$ and $V_{\rm cb}=2.05~\rm V$ and the second stage biased at $I_c=49~\rm mA$ and $V_{\rm cb}=1.84~\rm V$. At 150.2 GHz, the medium power amplifier exhibited 10.3-dBm output power with 3.4-dB associated power gain (Fig. 23). The first stage is then biased at $I_c=40~\rm mA$ and $V_{\rm cb}=2.04~\rm V$ and the second stage is biased at $I_c=51~\rm mA$ and $V_{\rm cb}=2.11~\rm V$. Uncompressed gain at 150.2 GHz is 9.2 dB.

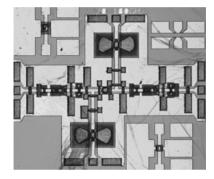


Fig. 24. Die photograph of a 150-GHz two-stage MMIC amplifier.

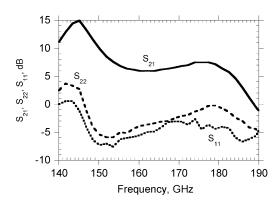


Fig. 25. Small-signal measurements of the 150-GHz two-stage amplifier.

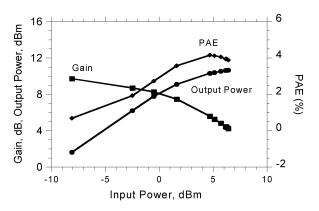


Fig. 26. Power measurements of the 150-GHz two-stage amplifier.

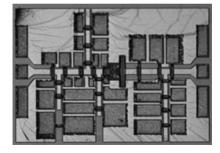


Fig. 27. Die photograph of a 84-GHz single-stage amplifier.

D. 150-GHz Two-Stage Amplifier

A second two-stage amplifier (Fig. 24) exhibited 10-dB gain at 150 GHz with the first stage is biased at $I_c=30$ mA and $V_{\rm cb}=1.0$ V and the second stage biased at $I_c=20$ mA and

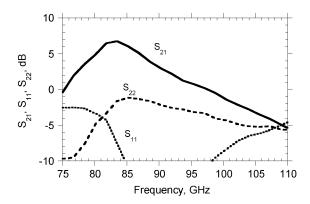


Fig. 28. Small-signal measurements of the 84-GHz amplifier.

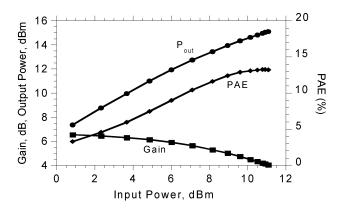


Fig. 29. Power measurements of a 84-GHz amplifier.

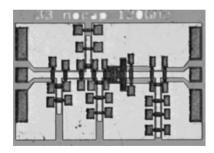


Fig. 30. Die photograph of a 92-GHz amplifier.

 $V_{\rm cb}=1.0$ V (Fig. 25). This two-stage amplifier demonstrated 11-dBm output power at 150.2 GHz with 4.2-dB associated power gain (Fig. 26). At 148 GHz, a 11.6-dBm saturated output power is obtained with an associated power gain of 4.5 dB. These power measurements are performed with the first stage biased at $I_c=43$ mA and $V_{\rm cb}=2.0$ V, and the second stage biased at $I_c=49$ mA and $V_{\rm cb}=2.07$ V.

E. 84-GHz Single-Stage Amplifier

A single-stage amplifier (Fig. 27) exhibited 5.6-dB small-signal gain at 84 GHz (Fig. 28) when biased at $I_c=37$ mA and $V_{\rm cb}=1.0$ V. The transistor has four separate 0.8 μ m \times 12 μ m fingers. This circuit demonstrated 15.1-dBm saturated output power at 84 GHz with >4-dB associated power gain (Fig. 29).

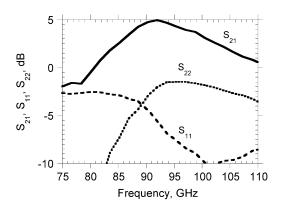


Fig. 31. Small-signal measurements of 92-GHz amplifier.

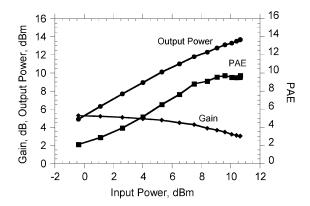


Fig. 32. Power measurements of the 92-GHz amplifier at 93 GHz.

F. 92-GHz Single-Stage Amplifier

A second common base amplifier (Fig. 30) exhibited 5-dB small signal gain at 92 GHz when biased at $I_c=39~\mathrm{mA}$ and $V_\mathrm{cb}=1.0~\mathrm{V}$ (Fig. 31). This amplifier demonstrated 13.7-dBm saturated output power at 93 GHz (Fig. 32) when biased at $I_c=46~\mathrm{mA}$ and $V_\mathrm{cb}=2.25~\mathrm{V}$.

VI. CONCLUSION

Common-base high-gain G-band and W-band medium power amplifiers in InP mesa DHBT technology have been presented. A single-stage common-base tuned amplifier with 7-dB small-signal gain at 176 GHz exhibited 8.7-dBm output power with 5-dB associated power gain at 172 GHz. The common base topology provides the largest MSG. This configuration requires careful layout to minimize C_{ce} and L_b or the MSG will be reduced. Despite large-signal load-line matching, the design values of gain remain high at 180 GHz, and close to the MSG. Power levels, efficiency, and center frequency are below design values, an effect we attribute to modeling errors. Recent DHBTs have been reported at 459 GHz f_{max} [6], suggesting feasibility of power amplifiers at 250 GHz. Increasing the number of HBT fingers should result in power amplifiers with output power over 100 mW. The results presented here have demonstrated the potential of InP DHBT technology for high-performance ultrahigh-frequency millimeter-wave circuit applications.

REFERENCES

- [1] M. Urteaga et al., "G-band (140–220-GHz) InP-based HBT amplifiers," IEEE J. Solid-State Circuits, vol. 38, no. 9, pp. 1451–1456, Sep. 2003.
- [2] C. Pobanz et al., "A high-gain monolithic D-band InP HEMT amplifier," IEEE J. Solid-State Circuits, vol. 34, no. 9, pp. 1219–1224, Sep. 1999.
- [3] R. Lai *et al.*, "InP HEMT amplifier development for *G*-band (140–220 GHz) applications," in *Int. Electron Devices Meeting Tech. Dig.*, San Francisco, CA, Dec. 2000, pp. 175–177.
- [4] L. Samoska et al., "A 20 mW, 150 GHz InP HEMT MMIC power amplifier module," *IEEE Microwave Wireless Compon. Lett.*, vol. 14, no. 2, pp. 56–58, Feb. 2004.
- [5] Z. Griffith *et al.*, "InGaAs/InP mesa DHBTs with simultaneously high f_t and $f_{\rm max}$ and low $C_{\rm cb}/I_c$ ratio," *IEEE Trans. Electron Devices*, vol. 25, no. 5, pp. 250–252, May 2004.
- [6] M. Dahlstrom *et al.*, "InGaAs/InP DHBT's with >370 GHz f_{τ} and $f_{\rm max}$ using a graded carbon-doped base," presented at the IEEE Device Research Conf., Salt Lake City, UT, Jun. 23–25, 2003.

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