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Developing Bipolar Transistors for Sub-mm-Wave Amplifiers and Next-Generation (300 GHz) Digital Circuits

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Our Specific Focus :

Present III-V transistors have enabled

- *300 GHz amplifiers.*
- *150 GHz clock rate digital ICs.*

So, how can we build next-generation ICs ?

- *600 GHz amplifiers.*
- *300 GHz digital clock rate.*

More Generally :

Can we build THz transistors ?

What do we mean by THz transistors ?

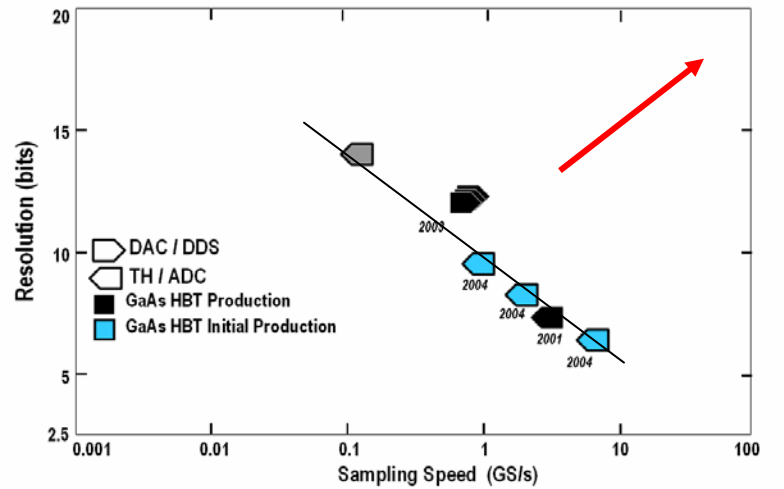
What are they for ?

How do we make them ?

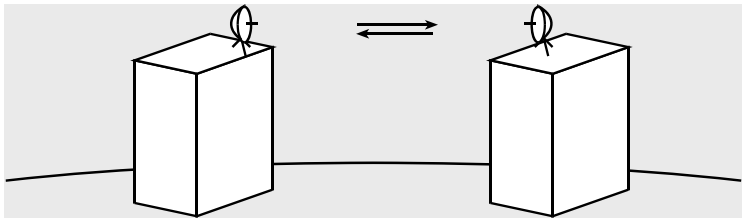
What are the frequency limits
of bipolar integrated circuits ?

THz Transistors: What Are They For ?

High-Resolution Microwave ADCs and DACs

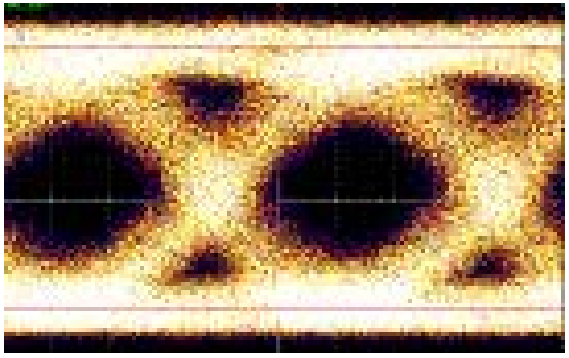


mm-wave radio:
40+ Gb/s on 250 GHz carrier



320 Gb/s fiber optics

& adaptive equalizers for 40 Gb/s ...



340 GHz & 600 GHz imaging systems

Why develop transistors for mm-wave & sub-mm-wave applications ?
→ compact ICs supporting complex high-frequency systems.

THz Transistors: What does this mean ?

A 1 THz current-gain cutoff frequency (f_τ) alone has little value

a transistor with 1000 GHz f_τ and 100 GHz f_{max} cannot amplify a 101 GHz signal.

RF-ICs & MIMICs need high power-gain cutoff frequency (f_{max})

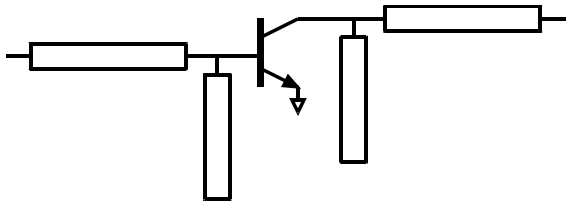
impedance matching is hard if f_τ is low.

100+ GHz digital also needs

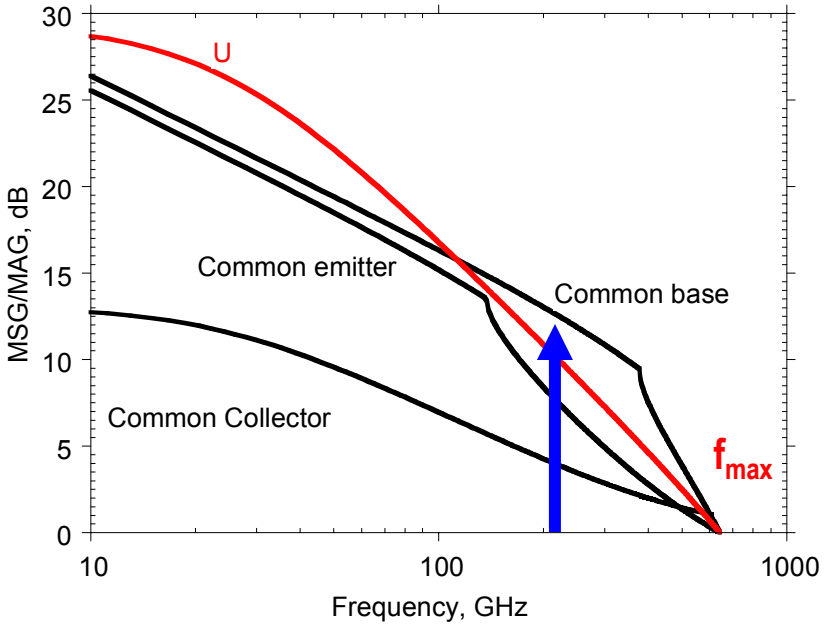
low ($C_{depletion}\,\Delta V / I$) and low ($I * R_{parasitic} / \Delta V$) .

So, how do we make a transistor with
>1 THz f_τ
>1 THz f_{max}
<50 fs $C\Delta V / I$ charging delays ?

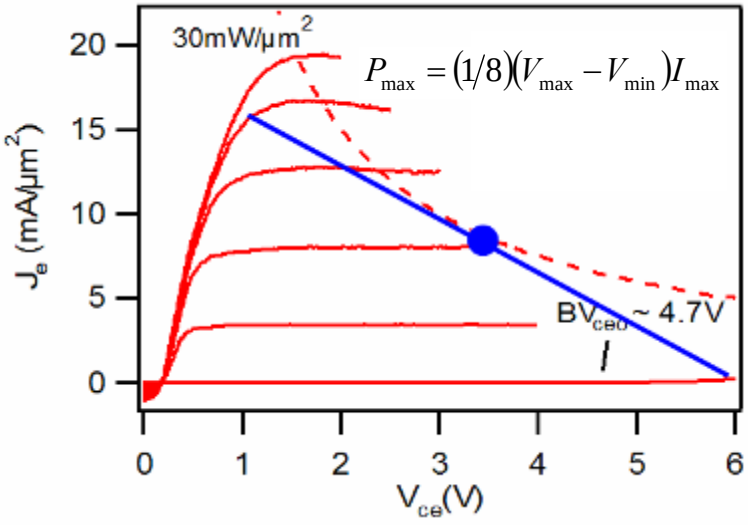
Key Performance Parameters for MMICs / RF-IC's



MIMIC / RF-ICs need gain ---hence f_{max}



Power amplifiers need breakdown voltage & power density



Low-Noise amplifiers need moderate associated gain and low noise

$$F_{\min,HEMT} \approx 1 + 2 \cdot \left(\frac{f}{f_\tau}\right) \cdot \sqrt{g_{mi}(R_S + R_g + R_i)\Gamma}$$

Key Performance Parameters for Fast Logic

Gate Delay Determined by :

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C}\right)\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Depletion capacitance charging through the base resistance

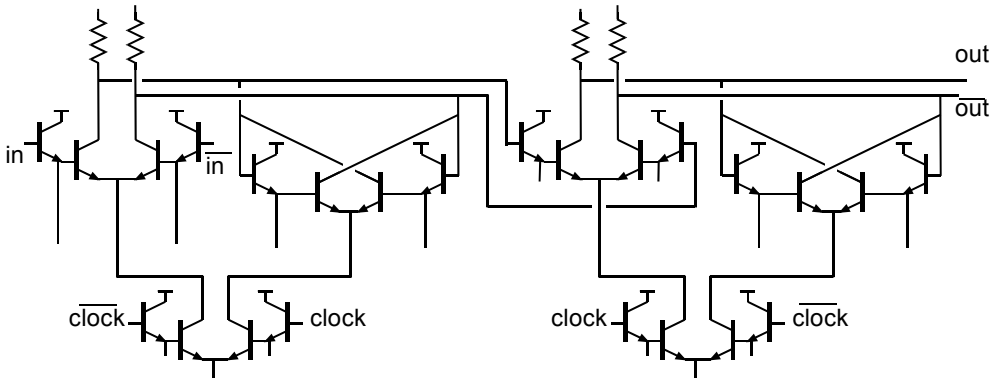
$$R_{\text{bb}}\left(C_{cbi}+C_{be,\text{depletion}}\right)$$

Supplying base + collector stored charge through the base resistance

$$R_{\text{bb}}\left(\tau_b+\tau_c\right)\left(\frac{I_C}{\Delta V_{LOGIC}}\right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 4\cdot\left(\frac{kT}{q}+R_{ex}I_c\right)$$



$(\tau_b+\tau_c)$ typically 10 - 25% of total delay;
Delay not well correlated with f_τ

$\left(\Delta V_{LOGIC}/I_C\right)\left(C_{cb}+C_{be,\text{depl}}\right)$ is 55% - 80% of total.

High $\left(I_C/C_{cb}\right)$ is a key HBT design objective.

$$J_{\max,Kirk}=2\varepsilon\bar{v}_{electron}\left(V_{ce,\text{operating}}+V_{ce,\text{full depletion}}\right)/T_c^2$$

$$\Rightarrow \frac{C_{cb}\Delta V_{LOGIC}}{I_C}=\frac{\Delta V_{LOGIC}}{2V_{CE,\min}}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2\bar{v}_{electron}}\right)$$

R_{ex} must be very low for low ΔV_{logic} at high J

Design HBTs for fast logic, not for high f_t & f_{max}

HBT Scaling Laws

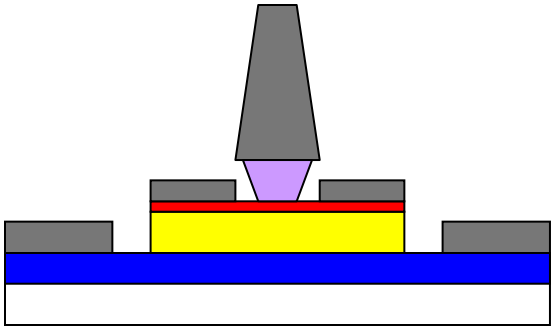
HBT Scaling Roadmaps

Bipolar Transistor Scaling Laws

*Goal: double transistor bandwidth when used in **any** circuit*

→ keep constant all resistances, voltages, currents

→ reduce 2:1 all capacitances and all transport delays



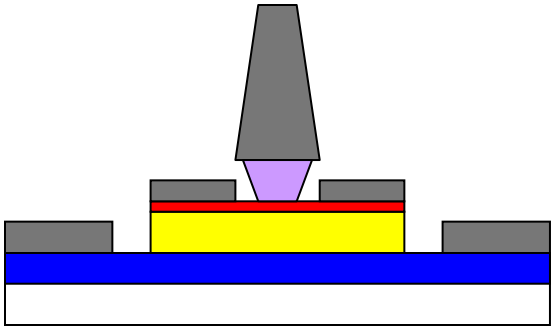
key device parameter	required change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter resistance per unit emitter area	decrease 4:1
current density	increase 4:1
base contact resistivity (if contacts lie above collector junction)	decrease 4:1
base contact resistivity (if contacts do not lie above collector junction)	unchanged

Epitaxial scaling: layer thicknesses

Lithographic scaling: junction dimensions

Resistance scaling: contact resistance and thermal resistance

InP HBT Scaling Roadmaps

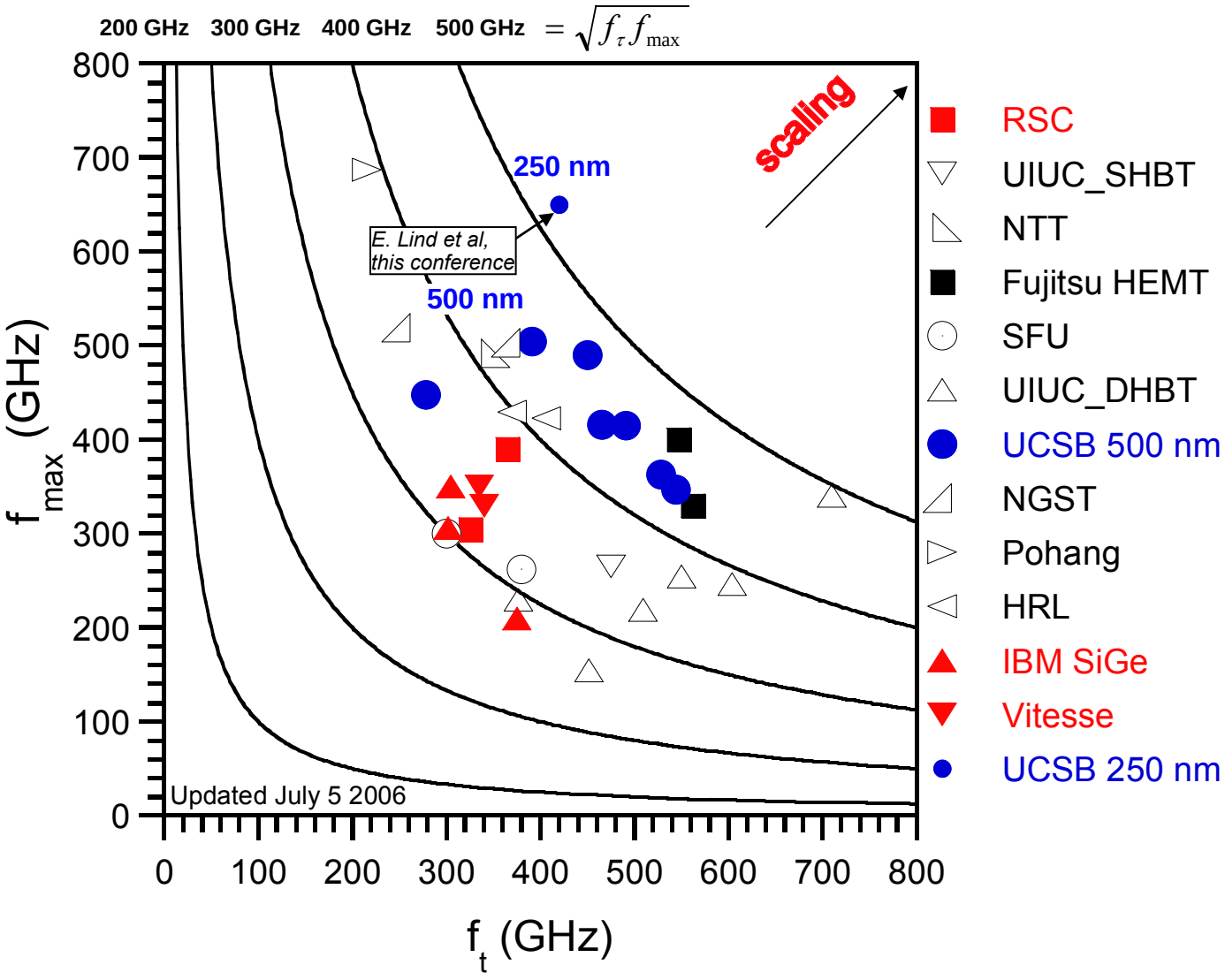


Parameter	scaling law	Gen. 2 (500 nm)	Gen. 3 (250 nm)	Gen. 4 (125 nm)	Gen 5 (62.5nm)
MS-DFF speed	γ^1	150 GHz	235 GHz	330 GHz	440 GHz
Amplifier center frequency	γ^1	245 GHz	400 GHz	650 GHz	750 GHz
Emitter Width	$1/\gamma^2$	500 nm	250 nm	125 nm	62.5 nm
Resistivity	$1/\gamma^2$	16 Ω-μm²	9 Ω-μm²	4 Ω-μm²	2 Ω-μm²
Base Thickness	$1/\gamma^{1/2}$	300Å	250 Å	212 Å	180 Å
Contact width	$\sim 1/\gamma^2$	300 nm	175 nm	120 nm	70 nm
Doping	γ^0	7 10^{19} /cm²	7 10^{19} /cm²	7 10^{19} /cm²	7 10^{19} /cm²
Sheet resistance	$\gamma^{1/2}$	500 Ω	600 Ω	707 Ω	830 Ω
Contact ρ	$1/\gamma^{1/2}$	20 Ω-μm²	10 Ω-μm²	5 Ω-μm²	5 Ω-μm²
Collector Width	$1/\gamma^2$	1.2 μm	0.60 μm	0.37 μm	0.20 μm
Thickness	$1/\gamma$	1500 Å	1060 Å	750 Å	530 Å
Current Density	γ^2	4.5 mA/μm²	9 mA/μm²	18 mA/μm²	36 mA/μm²
$A_{collector}/A_{emitter}$	γ^0	2.4	2.4	2.9	2.8
f_τ	γ^1	370 GHz	530 GHz	730 GHz	1.0 THz
f_{max}	γ^1	490 GHz	801 GHz	1.30 THz	1.5 THz
I_E / L_E	γ^0	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm
τ_f	$1/\gamma$	340 fs	240 fs	180 fs	130 fs
C_{cb} / I_c	$1/\gamma$	400 fs/V	280 fs/V	250 fs/V	190 fs/V
$C_{cb}\Delta V_{logic} / I_c$	$1/\gamma$	120 fs	85 fs	74 fs	57 fs
$R_{bb} / (\Delta V_{logic} / I_c)$	γ^0	0.76	0.54	0.34	0.39
$C_{je} (\Delta V_{logic} / I_C)$	$1/\gamma^{3/2}$	380 fs	180 fs	94 fs	50 fs
$R_{ex} / (\Delta V_{logic} / I_c)$	γ^0	0.24	0.24	0.24	0.24

key figures of merit for logic speed

Key scaling challenges →
emitter & base contact resistivity
current density→ device heating
collector-base junction width scaling
& Yield !

Present Status of Fast III-V Transistors



popular metrics :

f_τ or f_{max} alone

$(f_\tau + f_{max})/2$

$\sqrt{f_\tau\, f_{max}}$

$(1/f_\tau + 1/f_{max})^{-1}$

much better metrics :

power amplifiers :

PAE, associated gain, mW/μm

low noise amplifiers :

F_{min}, associated gain,

digital :

f_{clock}, hence $(C_{cb}\Delta V / I_c)$, $(R_{ex} I_c / \Delta V)$, $(R_{bb} I_c / \Delta V)$, $(\tau_b + \tau_c)$

Red = manufacturable technology for 10,000- transistor ICs

Scaling Generations

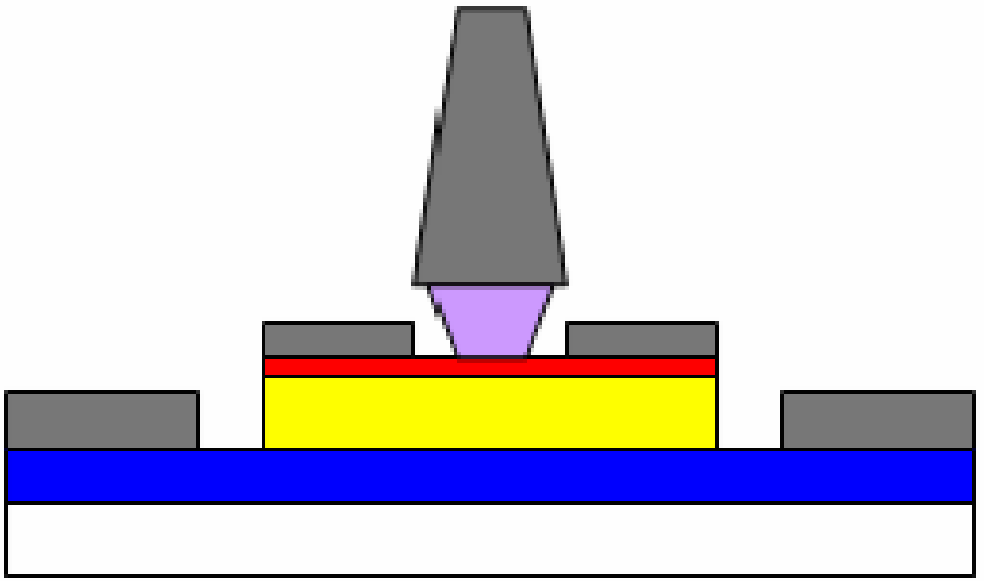
2005: InP DHBTs @ 500 nm Scaling Generation

emitter **500** nm width
16 $\Omega \cdot \mu m^2$ contact ρ

base **300** width,
20 $\Omega \cdot \mu m^2$ contact ρ

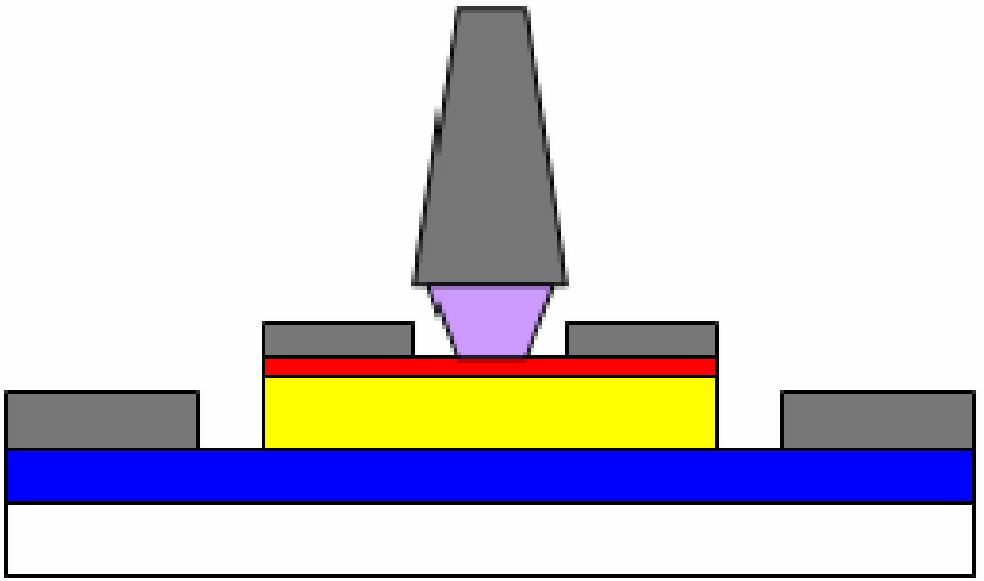
collector **150** nm thick,
5 $mA/\mu m^2$ current density
5 Vbreakdown

f_τ **400** GHz
f_{max} **500** GHz
power amplifiers **250** GHz
digital clock rate **160** GHz
(static dividers)



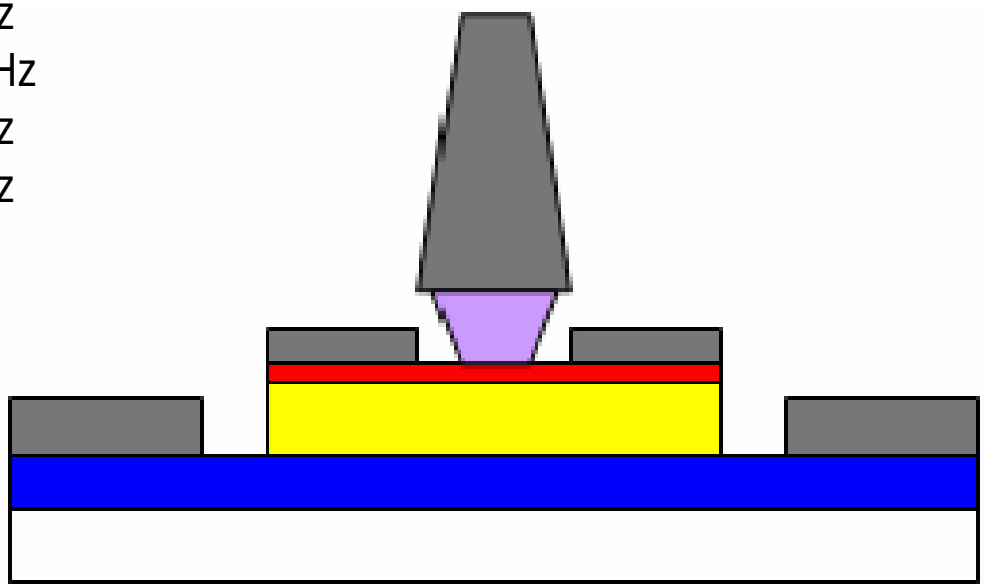
2006: 250 nm Scaling Generation, 1.414:1 faster

emitter	500	**250** nm width
	16	**9** $\Omega \cdot \mu m^2$ contact ρ
base	300	**150** width,
	20	**10** $\Omega \cdot \mu m^2$ contact ρ
collector	150	**100** nm thick,
	5	**10** $mA/\mu m^2$ current density
	5	**3.5** Vbreakdown
f_τ	400	**500** GHz
f_{max}	500	**700** GHz
power amplifiers	250	**350** GHz
digital clock rate (static dividers)	160	**230** GHz



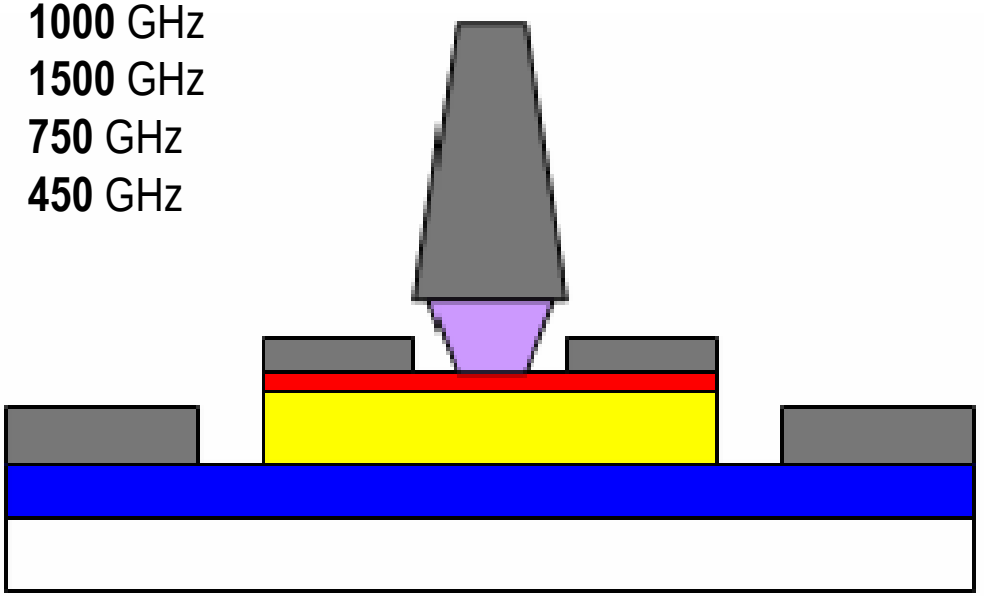
125 nm Scaling Generation→ almost-THz HBT

emitter	500	250	**125** nm width
	16	9	**4** $\Omega\cdot\mu m^2$ contact ρ
base	300	150	**75** width,
	20	10	**5** $\Omega\cdot\mu m^2$ contact ρ
collector	150	100	**75** nm thick,
	5	10	**20** $mA/\mu m^2$ current density
	5	3.5	**3** V breakdown
f_τ	400	500	**700** GHz
f_{max}	500	700	**1000** GHz
power amplifiers	250	350	**500** GHz
digital clock rate (static dividers)	160	230	**330** GHz



65 nm Scaling Generation→beyond 1-THz HBT

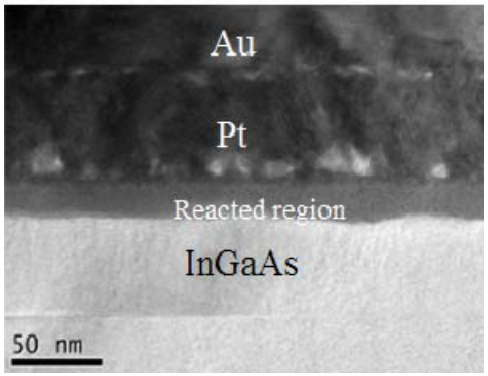
emitter	500	250	125	**63** nm width
	16	9	4	**2.5** $\Omega\cdot\mu m^2$ contact ρ
base	300	150	75	**70** nm width,
	20	10	5	**5** $\Omega\cdot\mu m^2$ contact ρ
collector	150	100	75	**53** nm thick,
	5	10	20	**35** $mA/\mu m^2$ current density
	5	3.5	3	**2.5** V breakdown
f_τ	400	500	700	**1000** GHz
f_{max}	500	700	1000	**1500** GHz
power amplifiers	250	350	500	**750** GHz
digital clock rate (static dividers)	160	230	330	**450** GHz

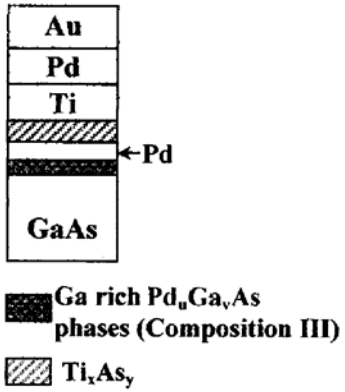


Scaling Challenges

Reducing Contact Resistivity

Pd or Pt solid-phase-reaction contacts

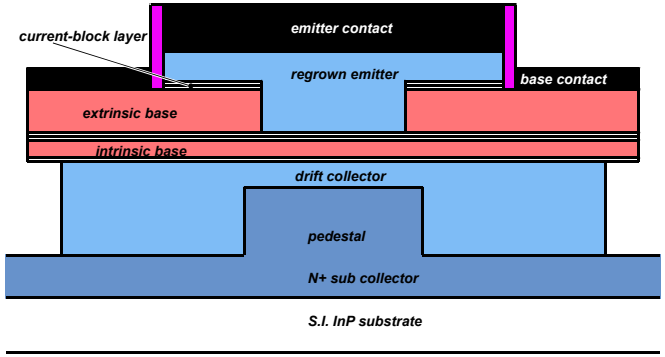




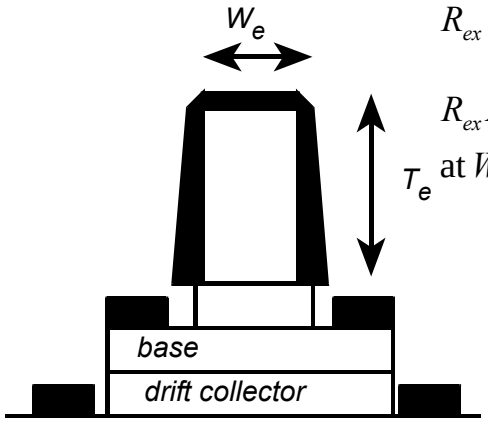
TEM : Lysczek, Robinson, & Mohney, Penn State
Sample: Urteaga, RSC

E. F. Chor et al , JAP 2000

Regrowth for wider emitter contacts



Wrap-around emitter contact



$$R_{ex} = \frac{1}{L_e} \cdot \sqrt{\frac{\rho_{contact}\rho_{bulk}}{2W_e}}$$

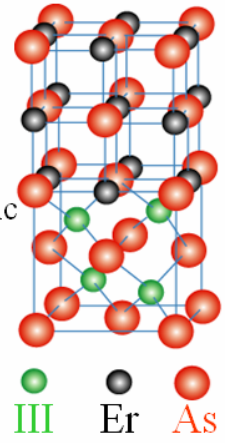
$$R_{ex}A_e = 1\Omega\text{-}\mu\text{m}^2$$

T_e at $W_e = 200$ nm

ErAs **in-situ MBE emitter contacts**

ErAs: Rocksalt structure

III-V: Zinc blend structure



Zimmerman, Gossard & Brown

grown in-situ by MBE
- no oxides,
- no contaminants

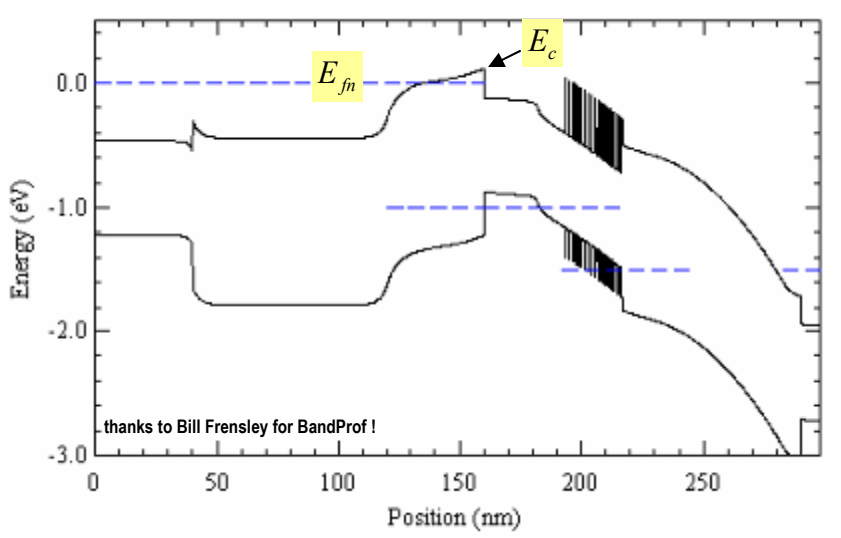
Lattice matched
- few defect states
- no Fermi level pinning

Thermodynamically stable
- little intermixing

*A. Guivarc'h, Electron. Lett.(1989)
**C.J.Palmstrøm Appl. Phys. Lett. (1990)

Q. G. Sheng, J. Appl. Phys. (1993)
A Guivarc'h, J. Appl. Phys. (1994)

Emitter-Base Degeneracy → 1.5 Ω–μm² Effective Junction Resistance



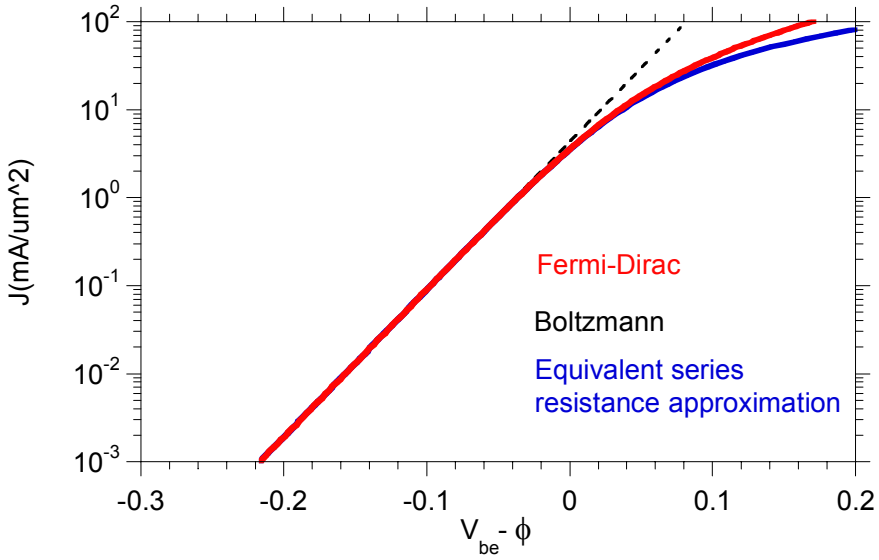
$10\ \text{mA}/\mu\text{m}^2 \rightarrow$ near degeneracy in emitter - base junction

Back of envelope : $qN_c v_{thermal} = 22\ \text{mA}/\mu\text{m}^2$

Better Approach : ballistic model, Fermi - Dirac integral

$$J \cong \frac{qm_e^*(kT)^2}{4\pi^2\hbar^3} F_1((E_{fn} - E_c)/kT)$$

[Liang & Lundstrom, unpublished]



Approximate series resistance model

$$V_{be} - \phi_{built-in} \cong (kT/q)\ln(J_e/J_o) + J_e\rho_{eq} + O(J_e^2)$$

$\rho_{eq} = 1.5\,\Omega - \mu\text{m}^2$ for InP, $\rho_{eq} \propto 1/m_e^*$

Degeneracy contributes ~ 1-2 Ω-μm² to observed emitter resistivity (?).

Solutions:

higher mass emitter ?

superlattice emitter ?

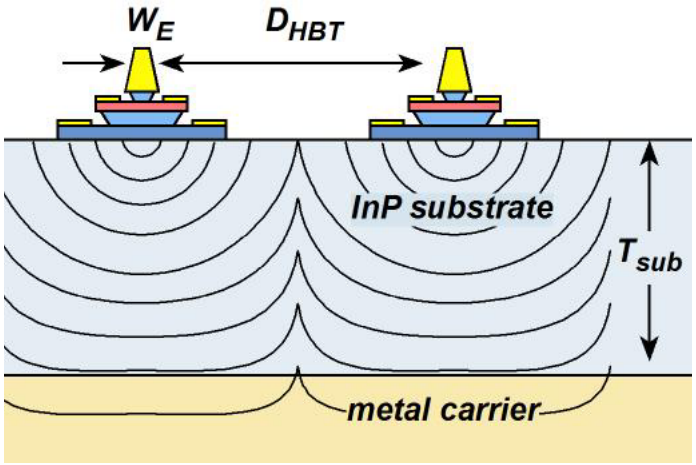
Temperature Rise Within Transistor & Substrate

For each doubling in digital clock rate

emitter width W_e decreases 4 : 1

transistor spacing D_{HBT} decreases 2 : 1

→ Increased junction temperature



cylindrical heat flow near junction $r < L_e$ | spherical heat flow for $L_e < r < D_{HBT}/2$ | planar heat flow for $r > D_{HBT}/2$

$$\Delta T_{\text{substrate}} \cong \frac{P}{\pi K_{InP} L_E} \ln\left(\frac{L_e}{W_e}\right) + \frac{P}{\pi K_{InP}}\left(\frac{1}{L_E} - \frac{1}{D}\right) + \frac{P}{K_{InP}} \cdot \left(\frac{T_{sub} - D/2}{D^2}\right)$$

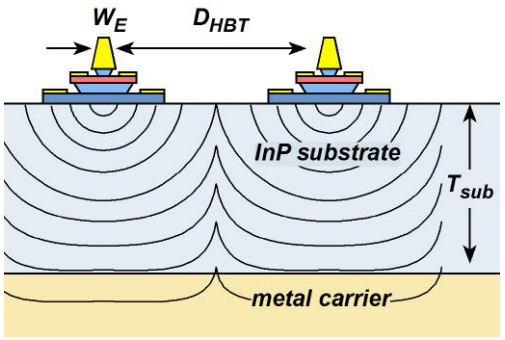
increases logarithmically with scaling	negligible variation with scaling	increases quadratically with scaling IF T_{sub} is constant

Temperature Rise Within Transistor & Substrate

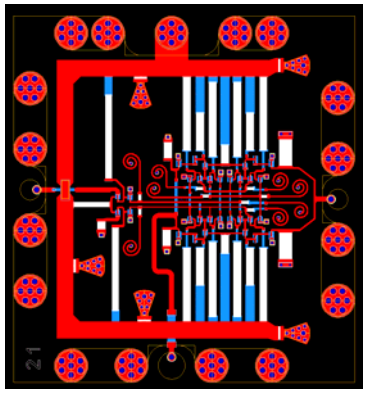
cylindrical heat flow near junction | spherical flow for $r > L_e$ | planar flow for $r > D_{HBT}/2$

$$\Delta T_{\text{substrate}} \cong \frac{P}{\pi K_{InP} L_E} \ln\left(\frac{L_e}{W_e}\right) + \frac{P}{\pi K_{InP}}\left(\frac{1}{L_E} - \frac{1}{D}\right) + \frac{P}{K_{InP}} \cdot \left(\frac{T_{sub} - D/2}{D^2}\right)$$

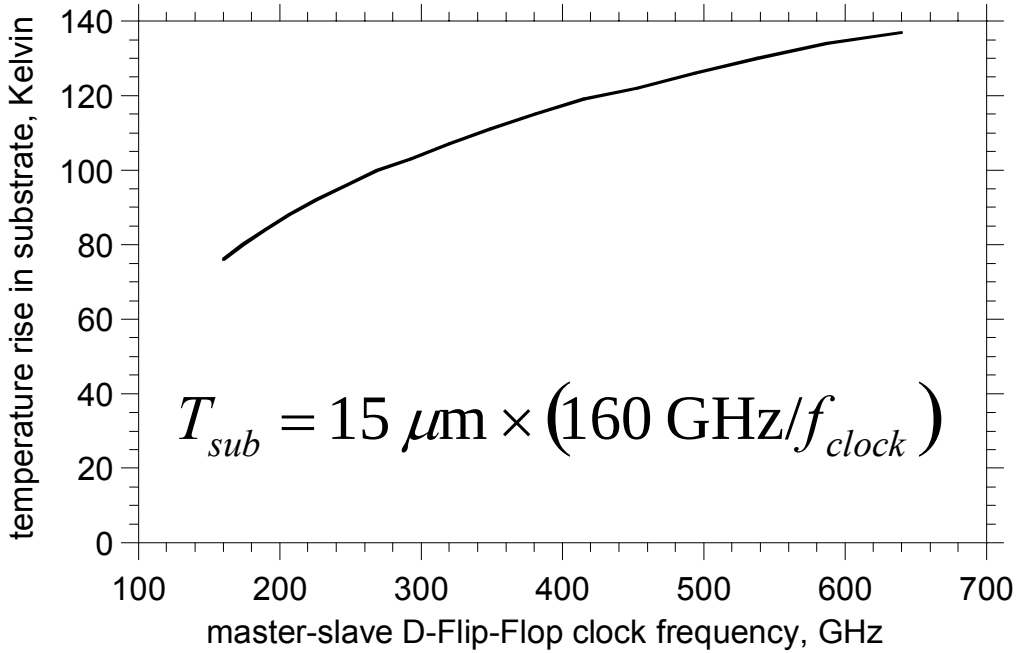
increases logarithmically | insignificant variation | increases quadratically if T_{sub} is constant



Agressively reducing substrate thickness T_{sub} allows acceptable substrate temperature rise even at 300 GHz digital clock rate.



Wiring lenghts, clock rates, power densities, etc. scaled from demonstrated 150 GHz digital ICs



Temperature Rise Within Package

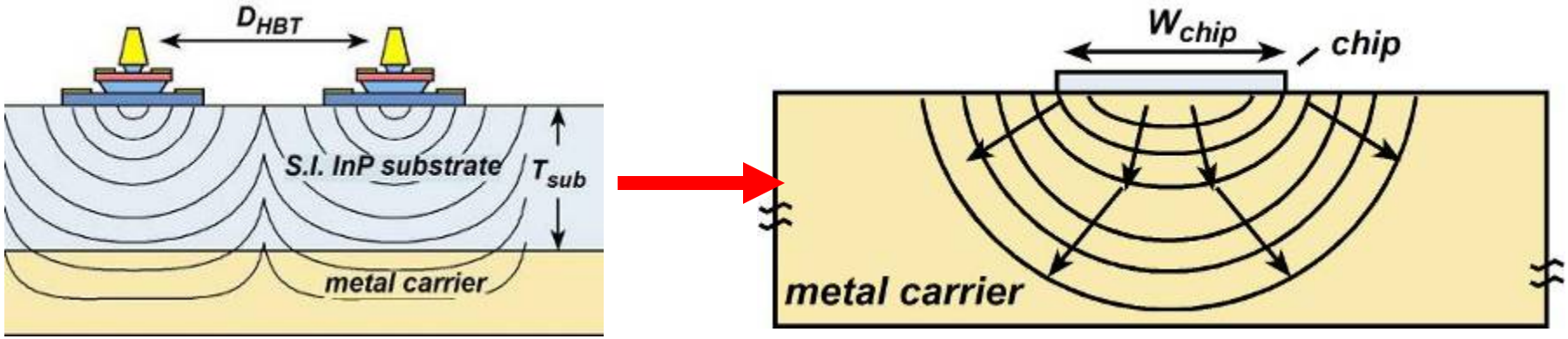
For each doubling in digital clock rate

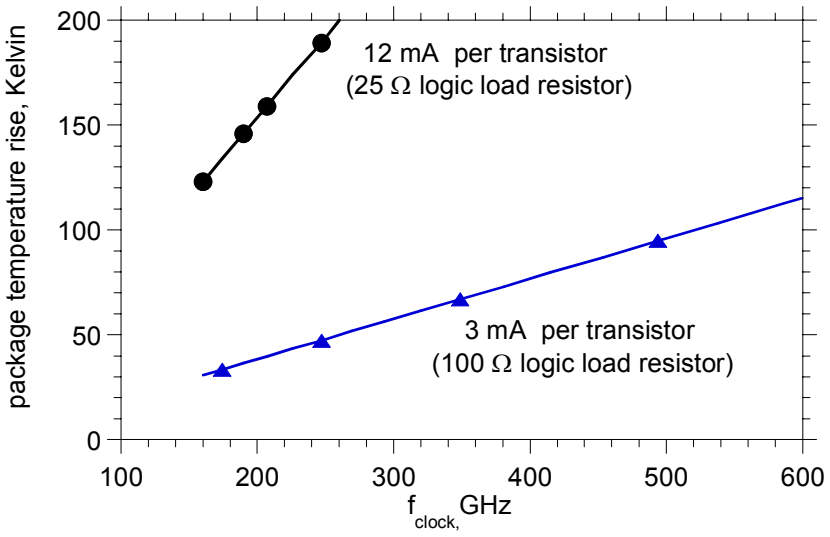
HBT spacings D_{HBT} decrease 2 : 1

$\rightarrow$ chip dimensions W_{chip} decrease 2 : 1

Total Package Temperature Rise

$$\Delta T_{package} \cong \left(\frac{1}{\pi} + \frac{1}{2}\right) \frac{P_{chip}}{K_{Cu} W_{chip}}$$





At 3 mA per transistor (100 Ω loading)
acceptable package temperature rise
with 1000 transistors / IC
even at 300 GHz digital clock rate.

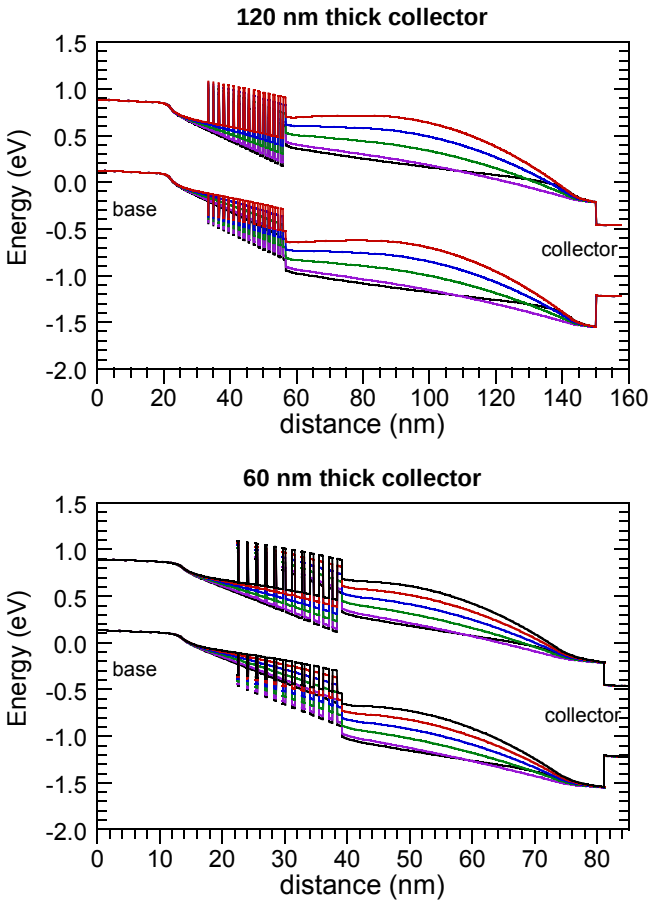
Assumptions :

- Transistor spacing : 20 μm $\cdot$ (150 GHz/f_{clock})
- V_{ce} = 2 V bias
- 1000 transistors/IC
- IC power = 1.5 × (transistor dissipation)

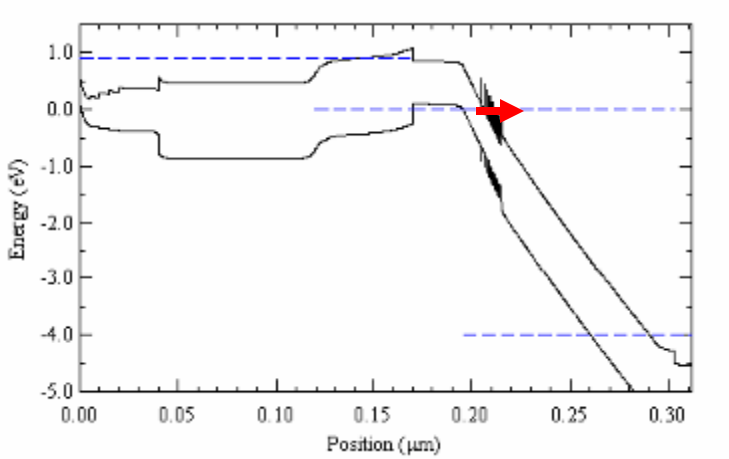
Scaling of Breakdown Voltage with InP/InGaAs InP DHBTs

Erik Lind

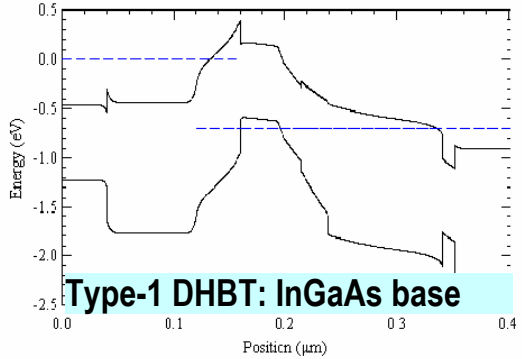
If collector is thinned without thinning grade and setback layers...

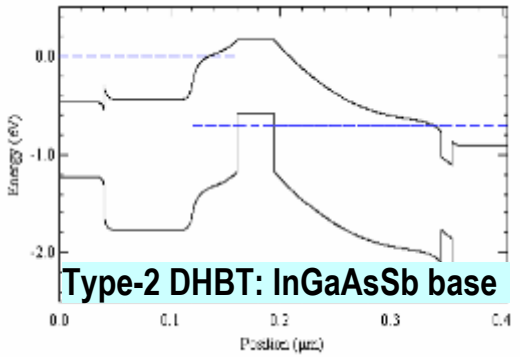


..then Zener tunneling through grade & setback layers can reduce BVCEO



Should we switch from type-I DHBT to type-2, eliminating the grade but sacrificing base transport ?

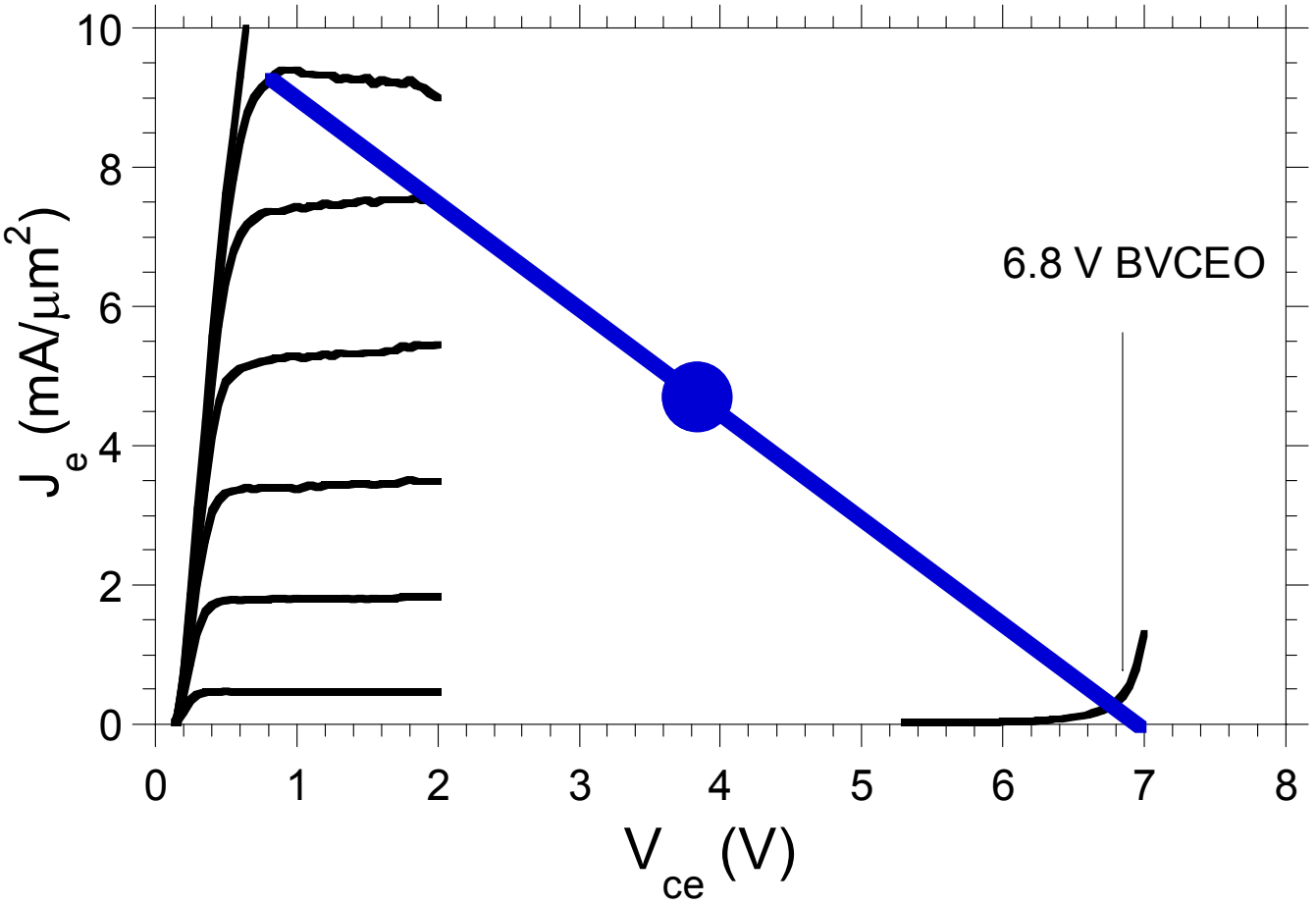




Or, should we simply thin the grade, using fewer superlattice periods ?

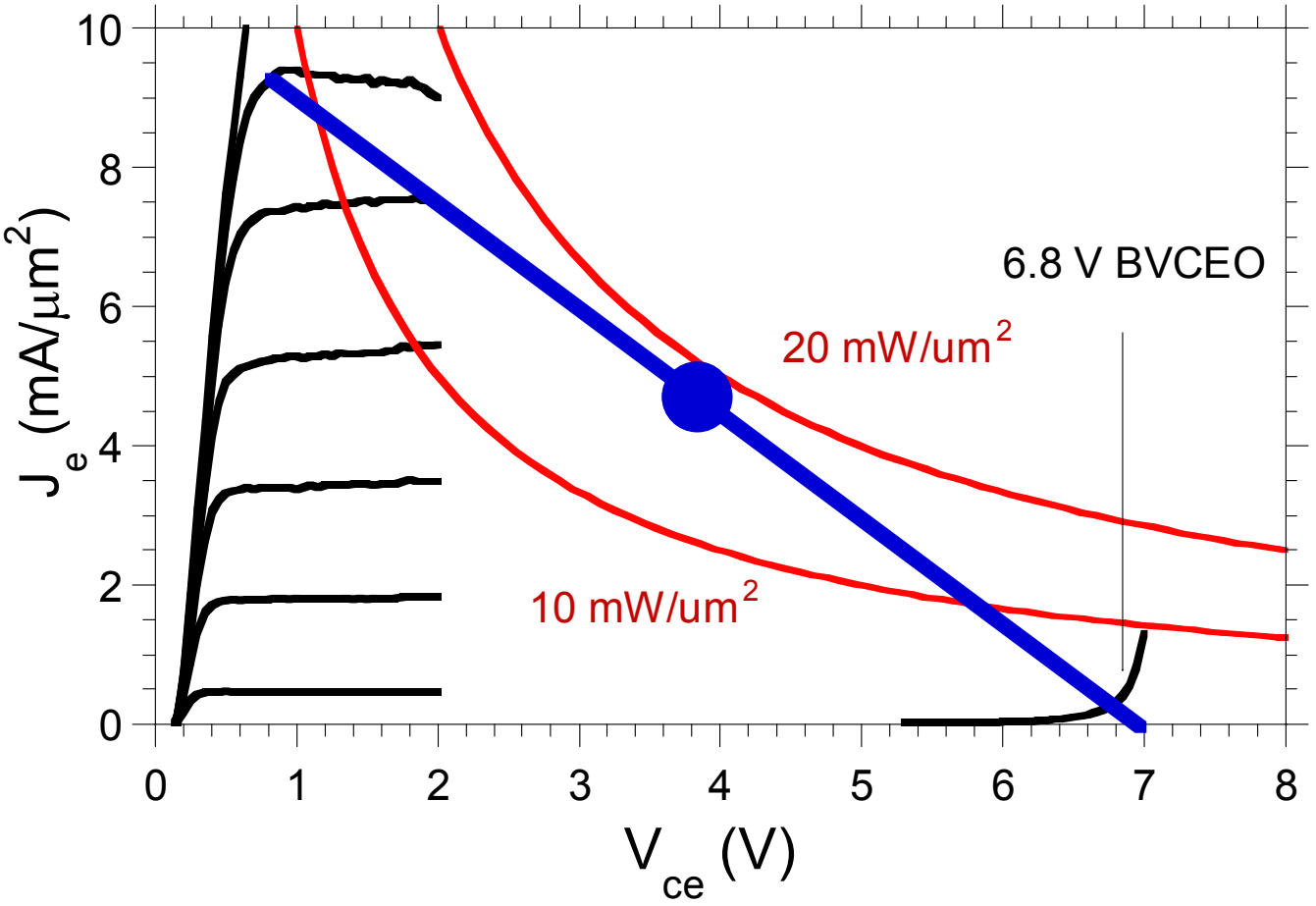
...or other approaches...

Breakdown Voltage: What do we really need ?



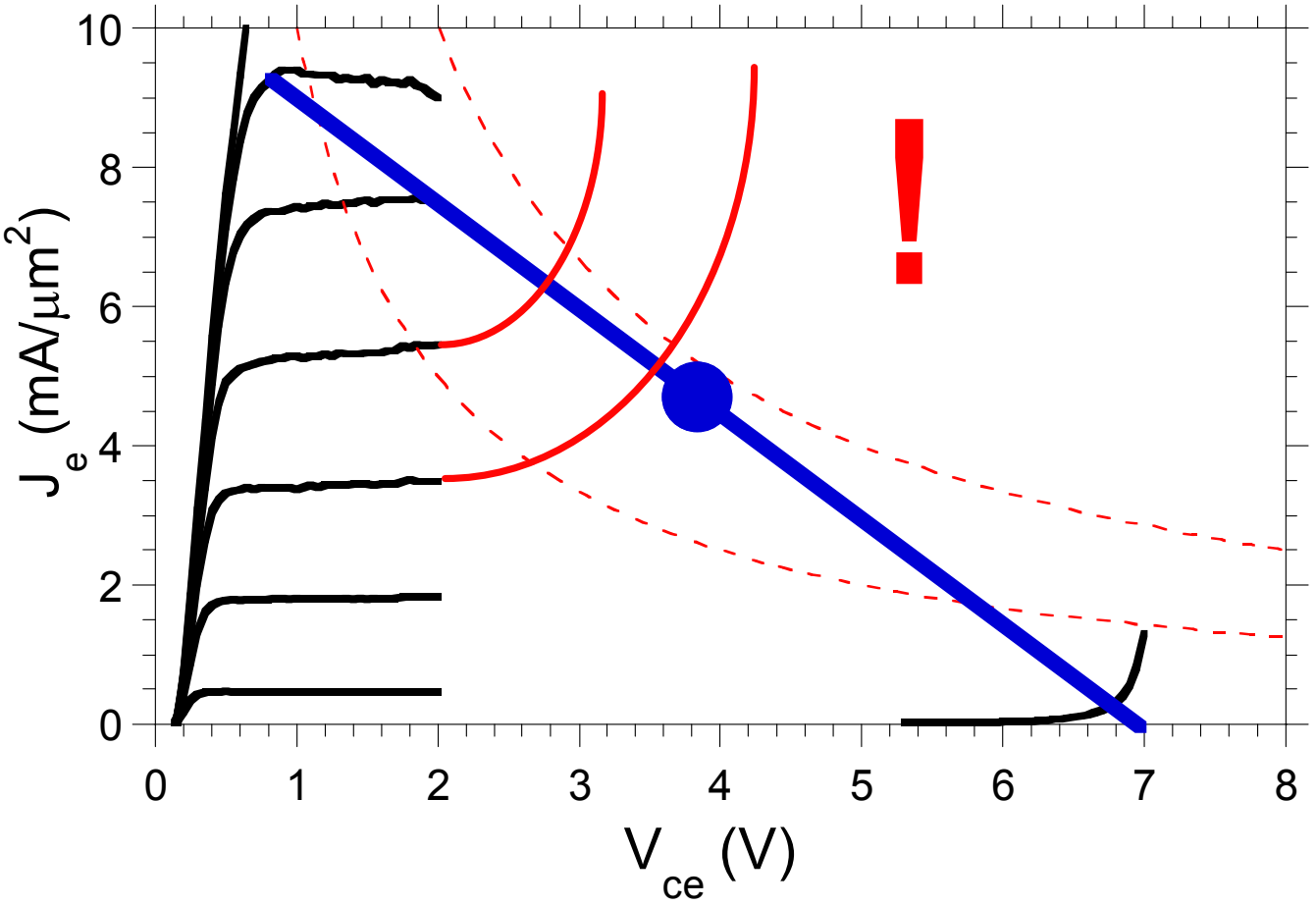
$$P_{\max} = (1/8)(V_{\max} - V_{\min})I_{\max}$$

Breakdown Voltage: What do we really need ?



$$P_{\max} = (1/8)(V_{\max} - V_{\min})I_{\max}$$

Breakdown Voltage: What do we really need ?



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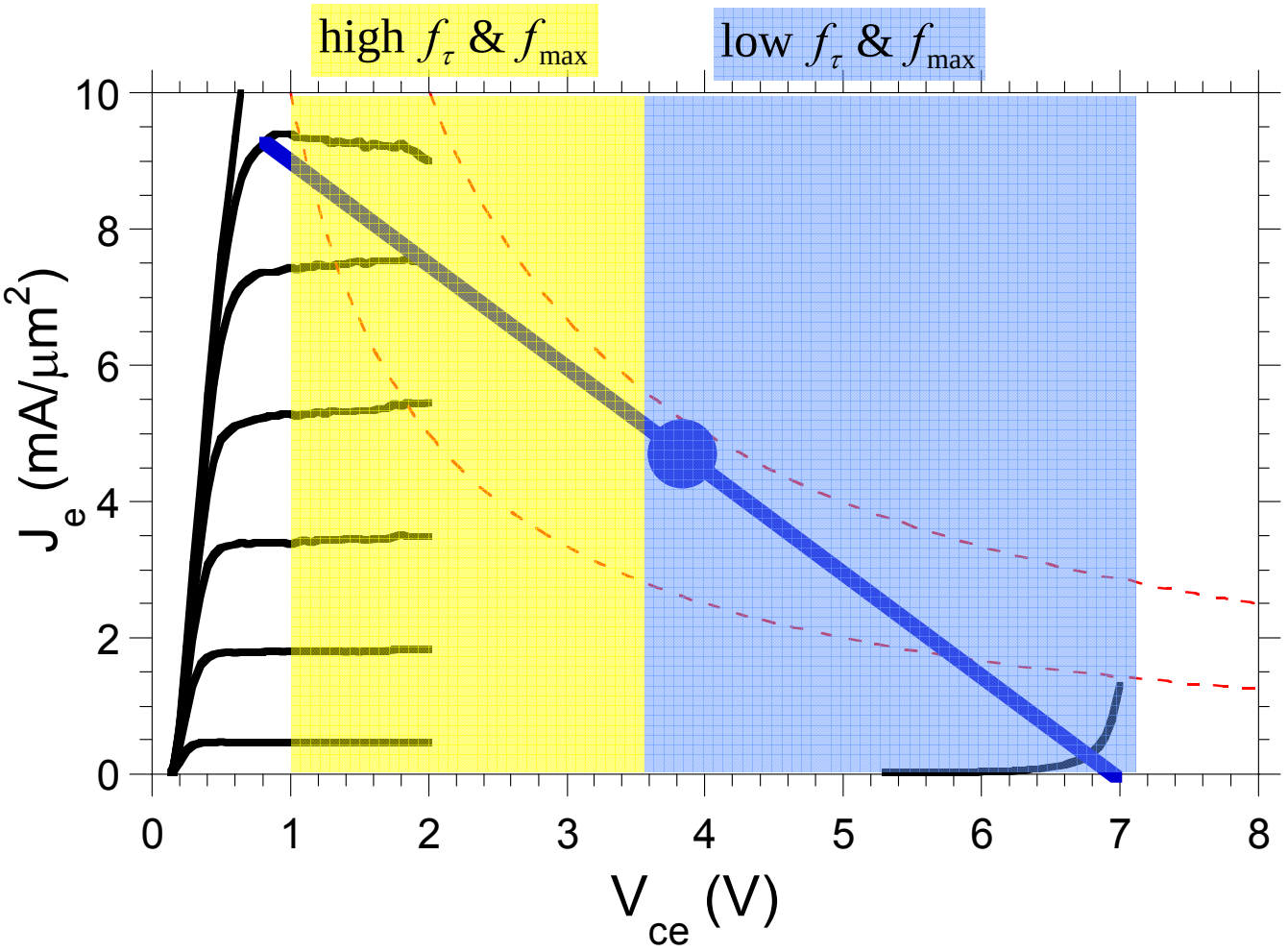
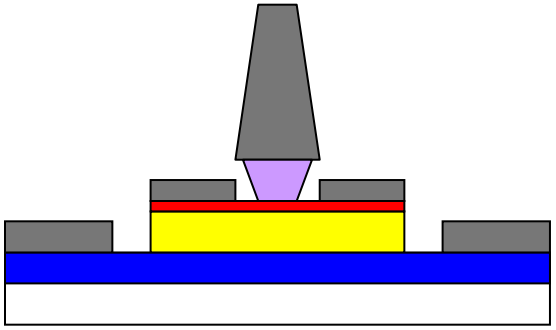
Breakdown Voltage: What do we really need ?



$$P_{max} = (1/8)(V_{max} - V_{min})I_{max}$$

bandwidth decreases at high V_{ce} due to velocity-field characteristics

Scaling challenges: What looks easy, what looks hard ?

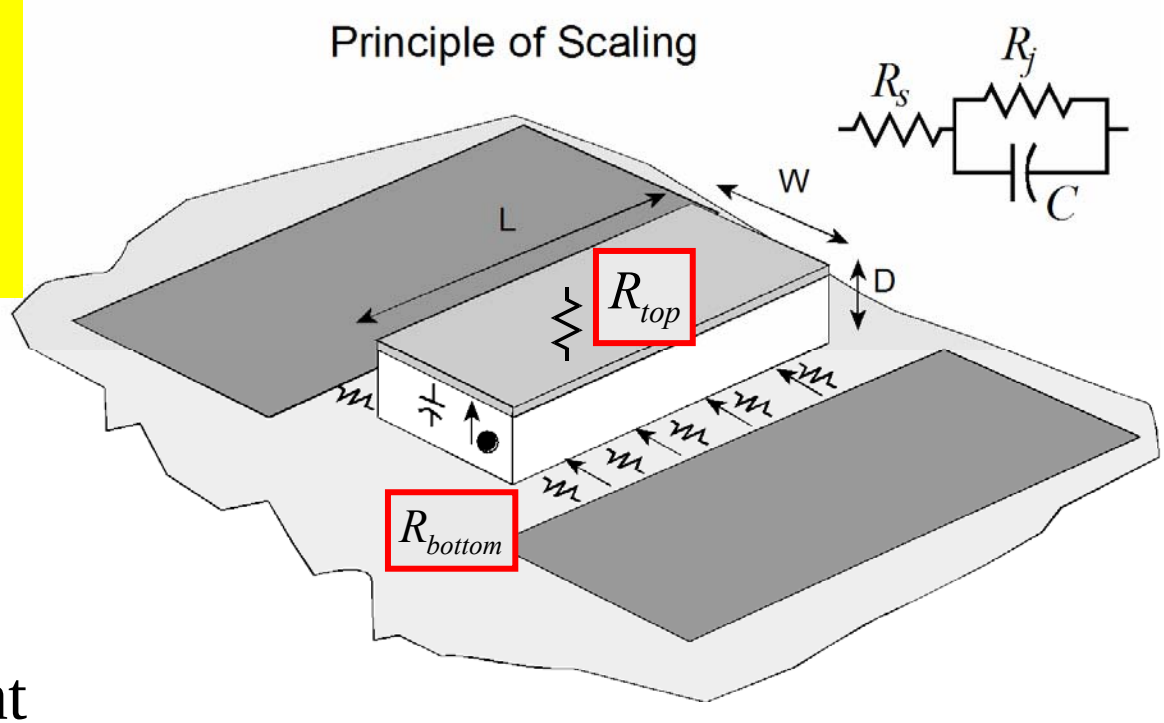


key device parameter	required change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter resistance per unit emitter area	decrease 4:1
current density	increase 4:1
base contact resistivity (if contacts lie above collector junction)	decrease 4:1
base contact resistivity (if contacts do not lie above collector junction)	unchanged

Hard:
Thermal resistance (ICs)
Emitter contact + access resistance
Yield in deep submicron processes
Contact electromigration (?), dark-line defects (?)

Probably not as hard :
Maintaining adequate breakdown for 3 V operation...

Frequency Limits and Scaling Laws of (most) Electron Devices



$\tau \propto$ thickness

$C \propto$ area / thickness

$R_{top} \propto \rho_{contact}$ / area

$R_{bottom} \propto 1/$ stripe lenght

resistance *capacitance* *transit time*

device bandwidth

applies to:

transistors: BJTs & HBTs, MOSFETS & HEMTs,
Schottky diodes, photodiodes, photo mixers, RTDs,

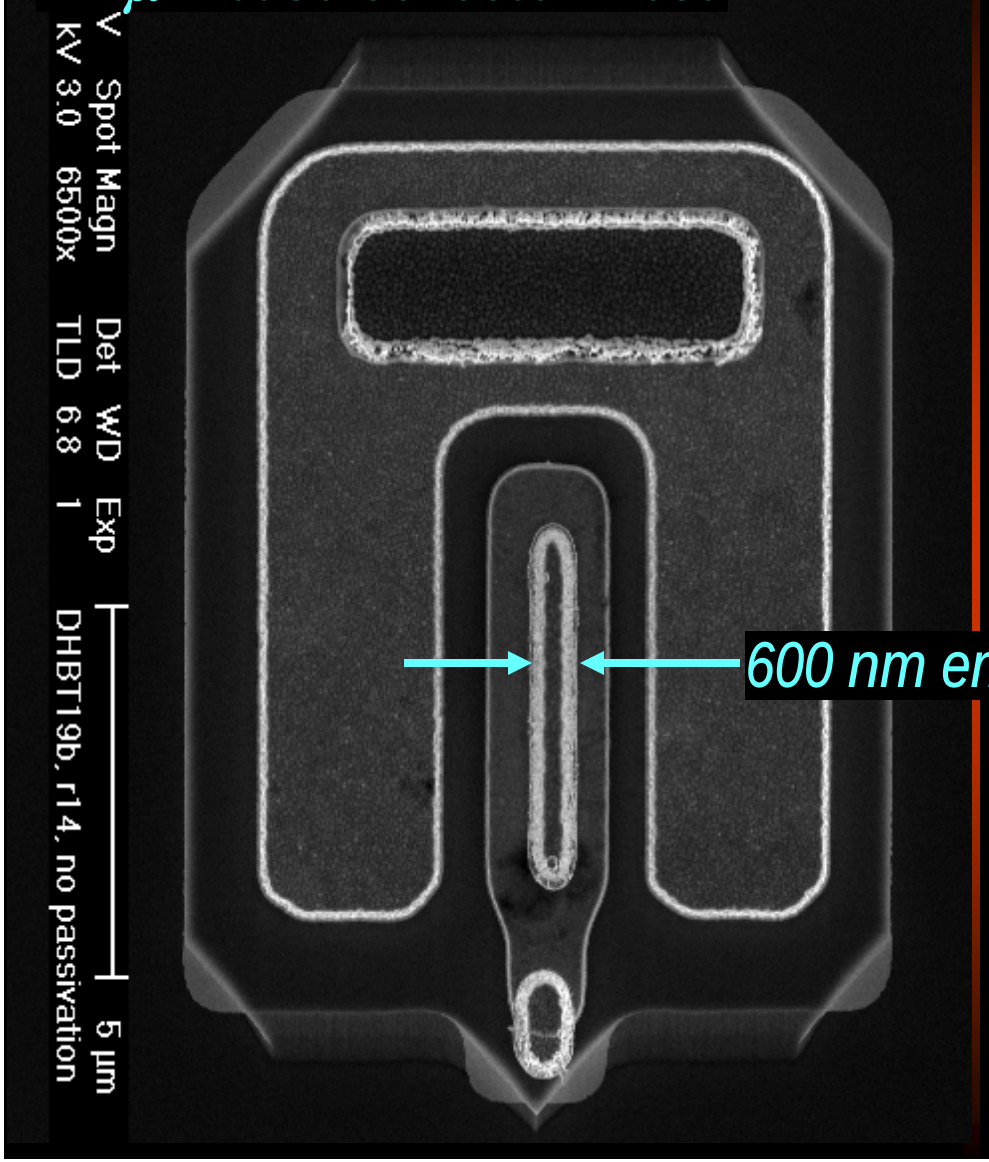
Applies whenever AC signals are removed though Ohmic contacts
Semiconductor lasers avoid R/C/τ limits by radiating through end facets

Mesa HBTs

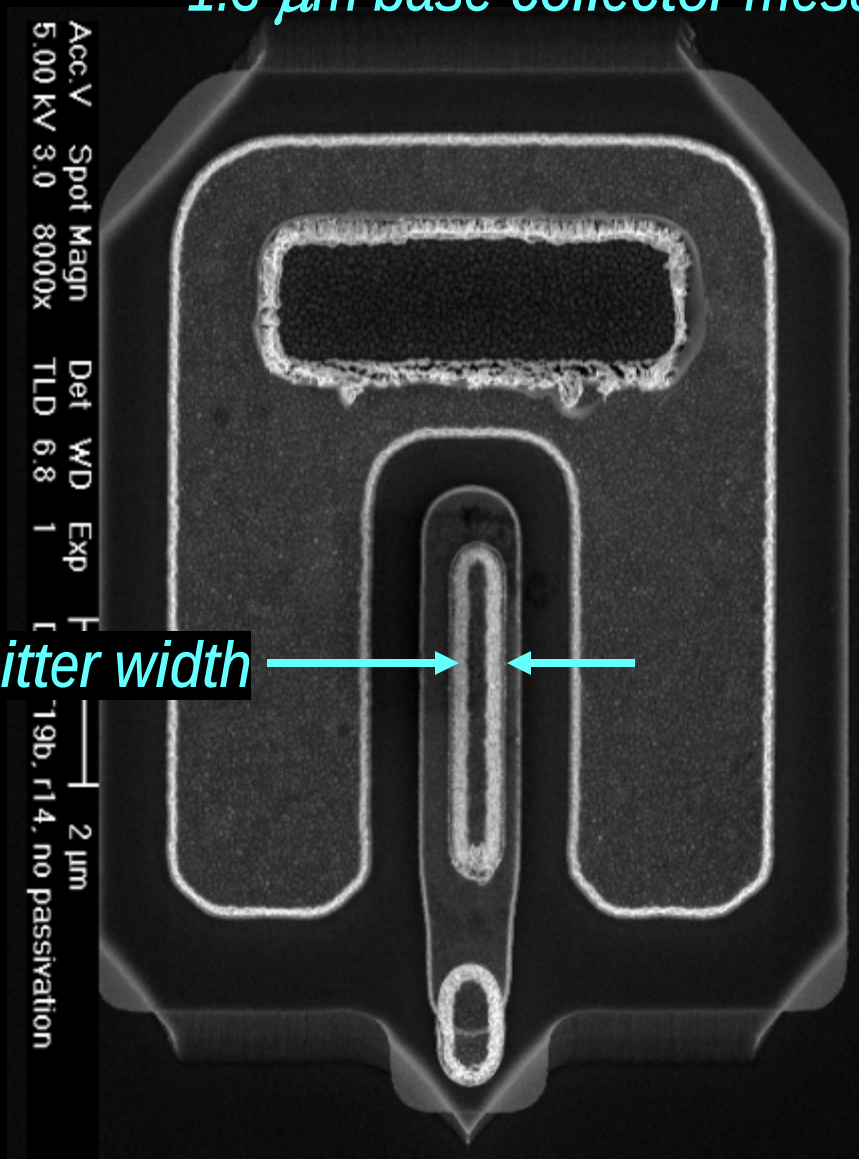
Zach Griffith

Mesa DHBTs at the 500-600 nm Scaling Generation

1.7 μm base-collector mesa



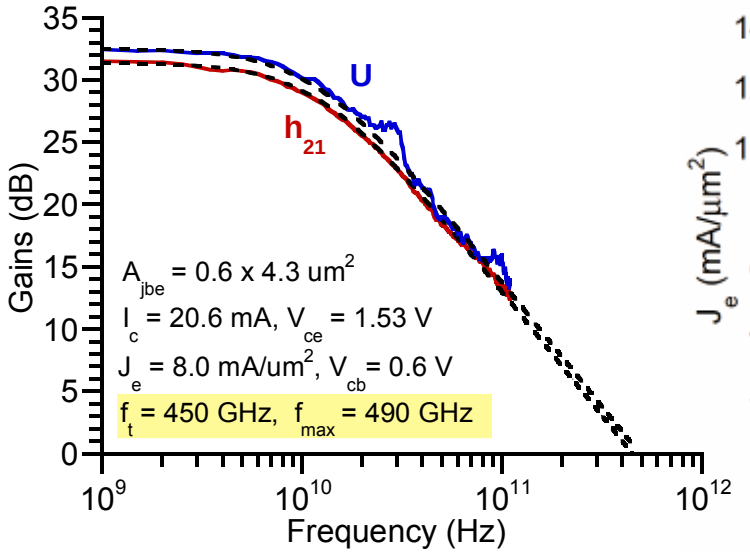
1.3 μm base-collector mesa

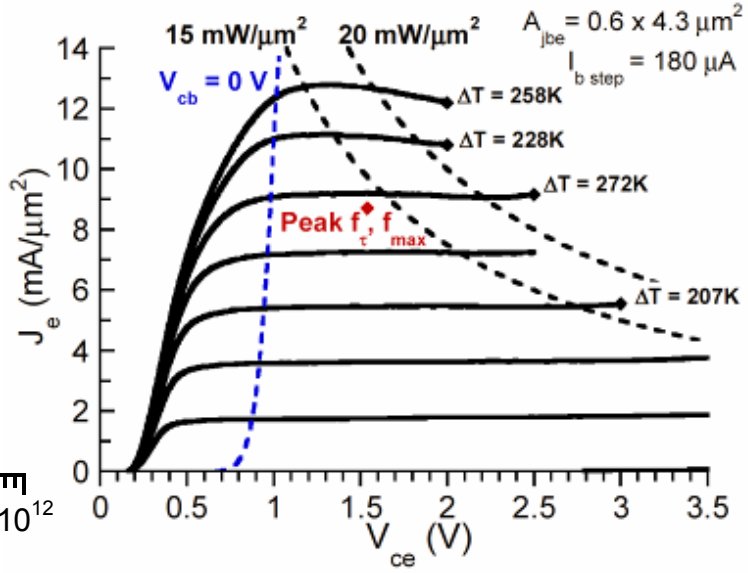


600 nm emitter width

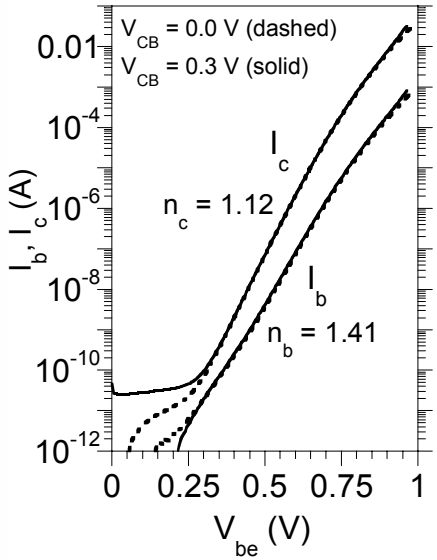
Zach Griffith

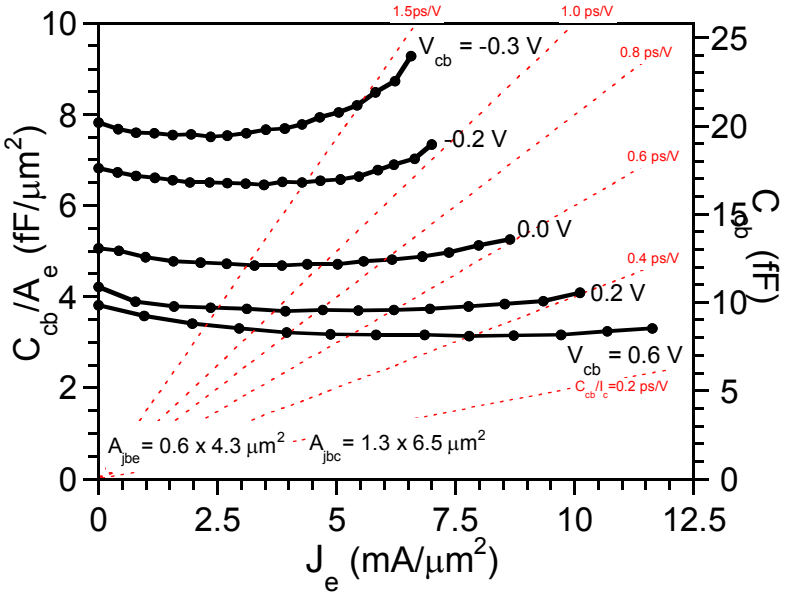
InP DHBT: 600 nm lithography, 120 nm thick collector, 30 nm thick base





Gummel characteristics





$\beta \approx 40$, $V_{BR,CEO}$ = 3.9 V.

Emitter contact $R_{cont} < 10\ \Omega\cdot\mu m^2$

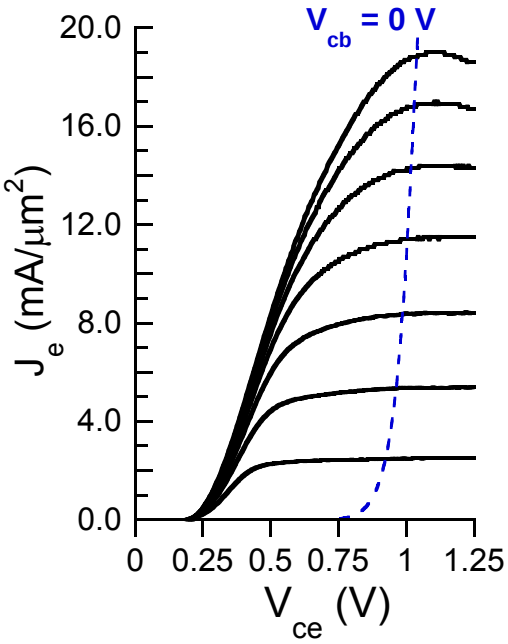
Base : R_{sheet} = 610 Ω/sq, $R_{cont} = 4.6\ \Omega\cdot\mu m^2$

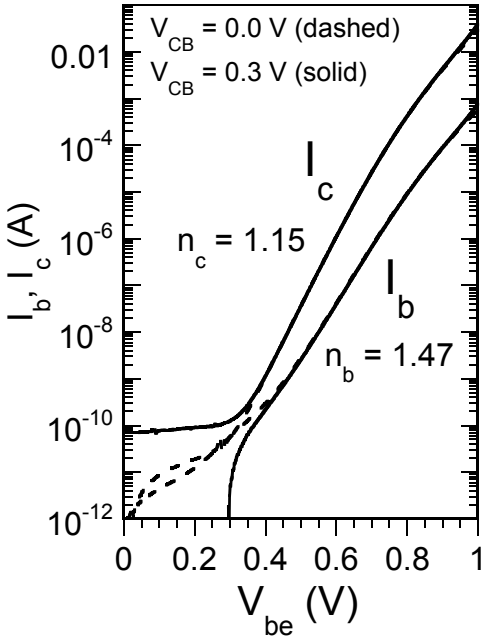
Collector : R_{sheet} = 12.1 Ω/sq, $R_{cont} = 8.4\ \Omega\cdot\mu m^2$

Zach Griffith

InP DHBT: 600 nm lithography, 75 nm thick collector, 20 nm base

DC characteristics





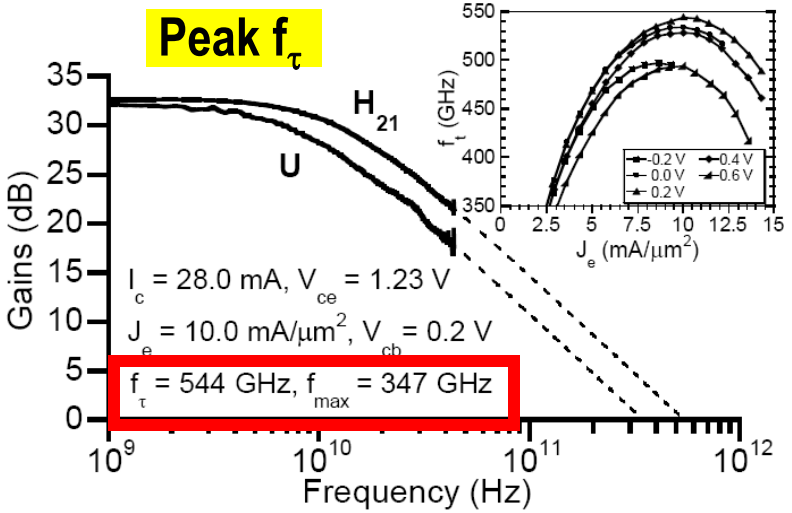
$A_{je} = 0.65 \times 4.3\ \mu m^2$, $I_{b,step} = 175\ \mu A$

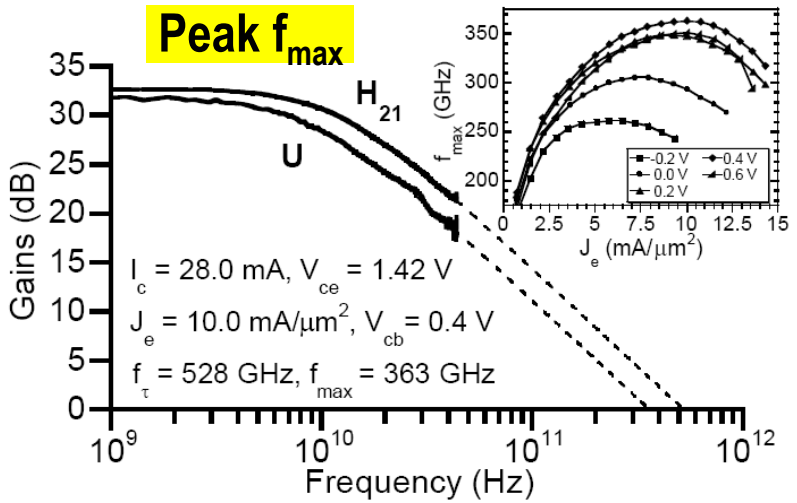
Average $\beta \approx 50$, $BV_{CEO} = 3.2$ V, $BV_{CBO} = 3.4$ V ($I_c = 50\ \mu A$)

Emitter contact (from RF extraction), $R_{cont} \approx 8.6\ \Omega \cdot \mu m^2$

Base (from TLM) : $R_{sheet} = 805\ \Omega/sq$, $R_{cont} = 16\ \Omega \cdot \mu m^2$

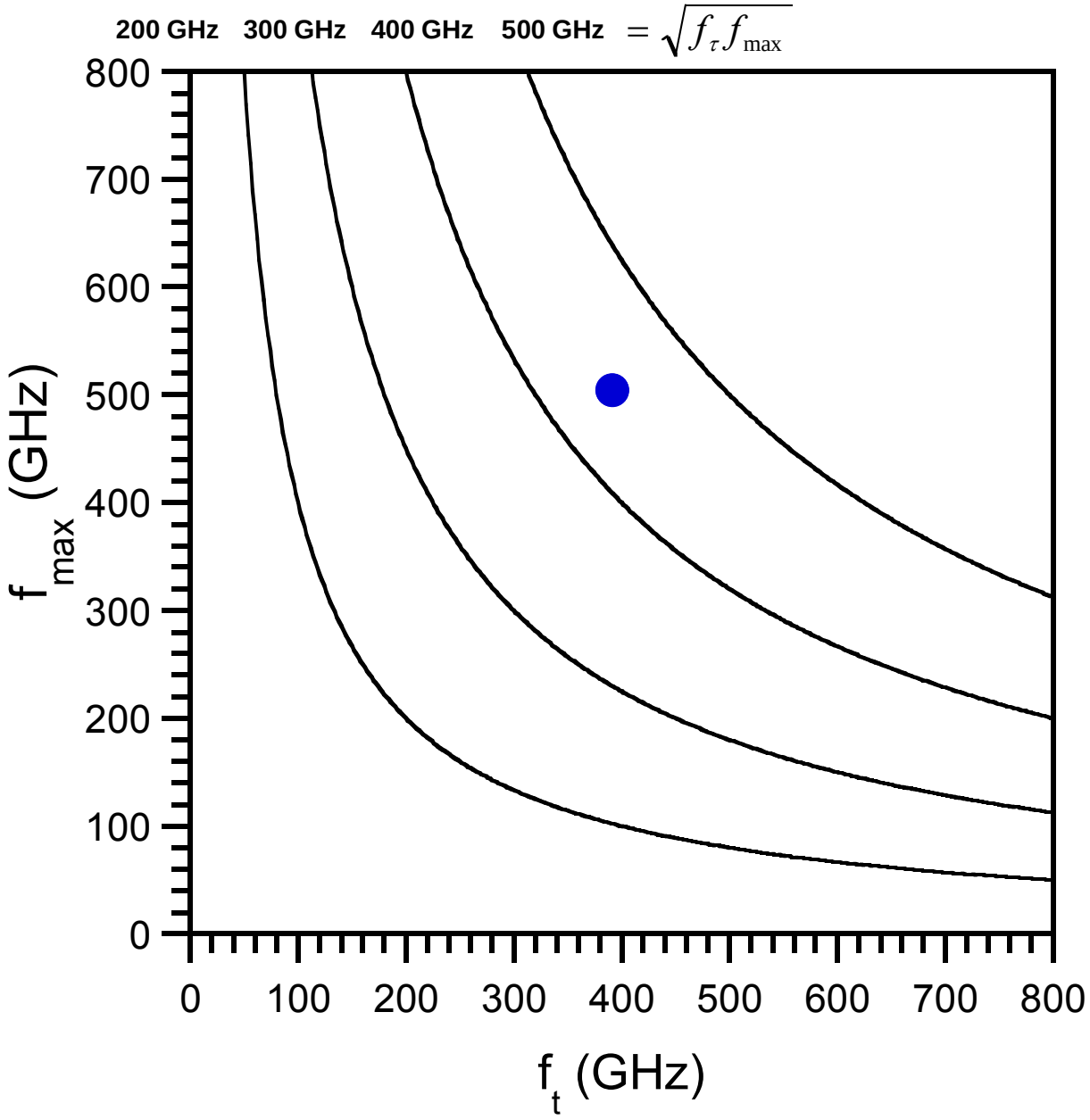
Collector (from TLM) : $R_{sheet} = 12.0\ \Omega/sq$, $R_{cont} = 4.7\ \Omega \cdot \mu m^2$





RF characteristics

Variation of Transistor Bandwidth with Scaling



popular metrics :

f_τ or f_{max} alone

$(f_\tau + f_{max})/2$

$\sqrt{f_\tau\, f_{max}}$

$(1/f_\tau + 1/f_{max})^{-1}$

much better metrics :

power amplifiers :

PAE, associated gain, mW/μm

low noise amplifiers :

F_{min}, associated gain,

digital :

f_{clock}, hence

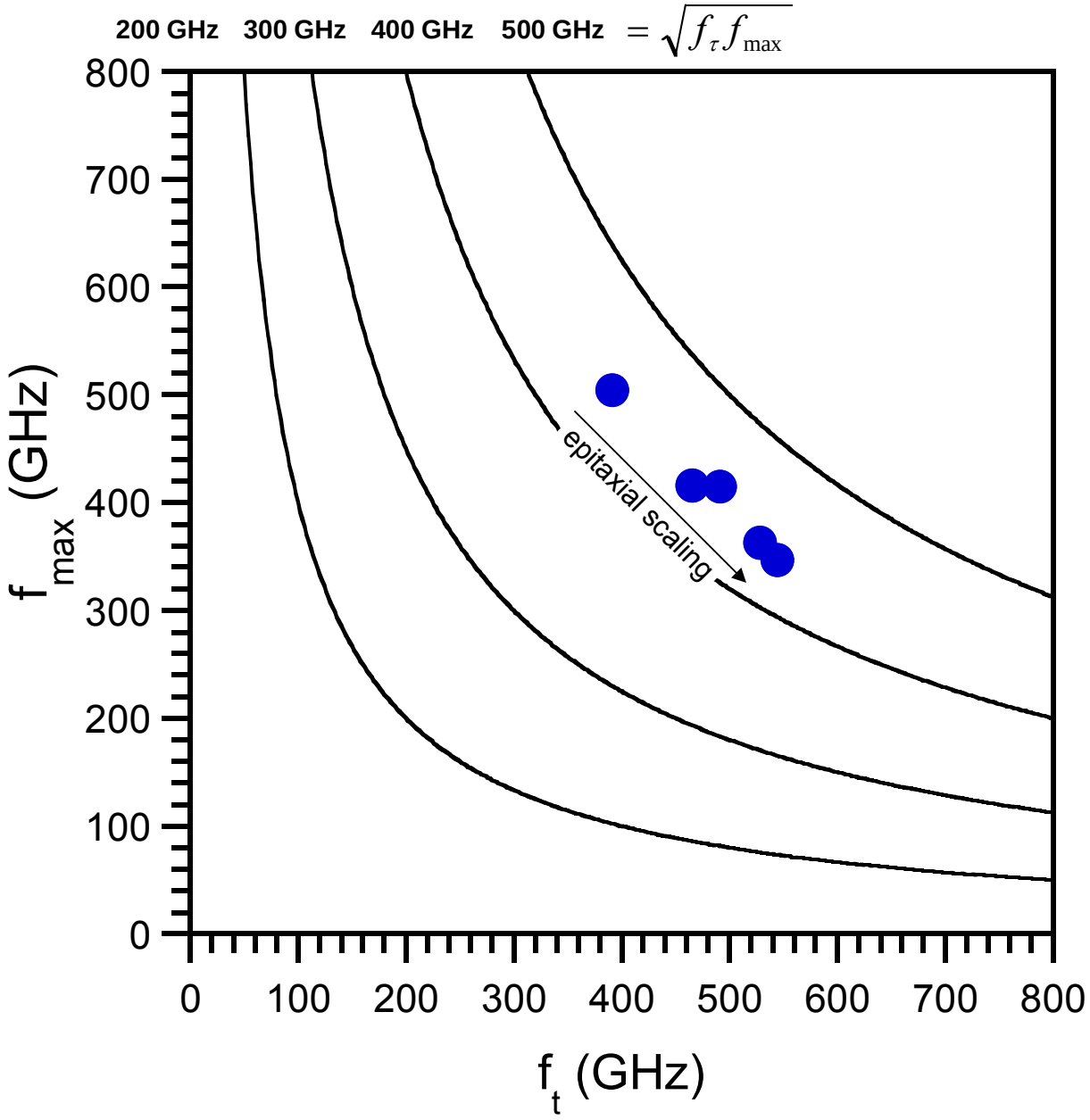
$(C_{cb}\Delta V / I_c)$,

$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

$(\tau_b + \tau_c)$

Variation of Transistor Bandwidth with Scaling



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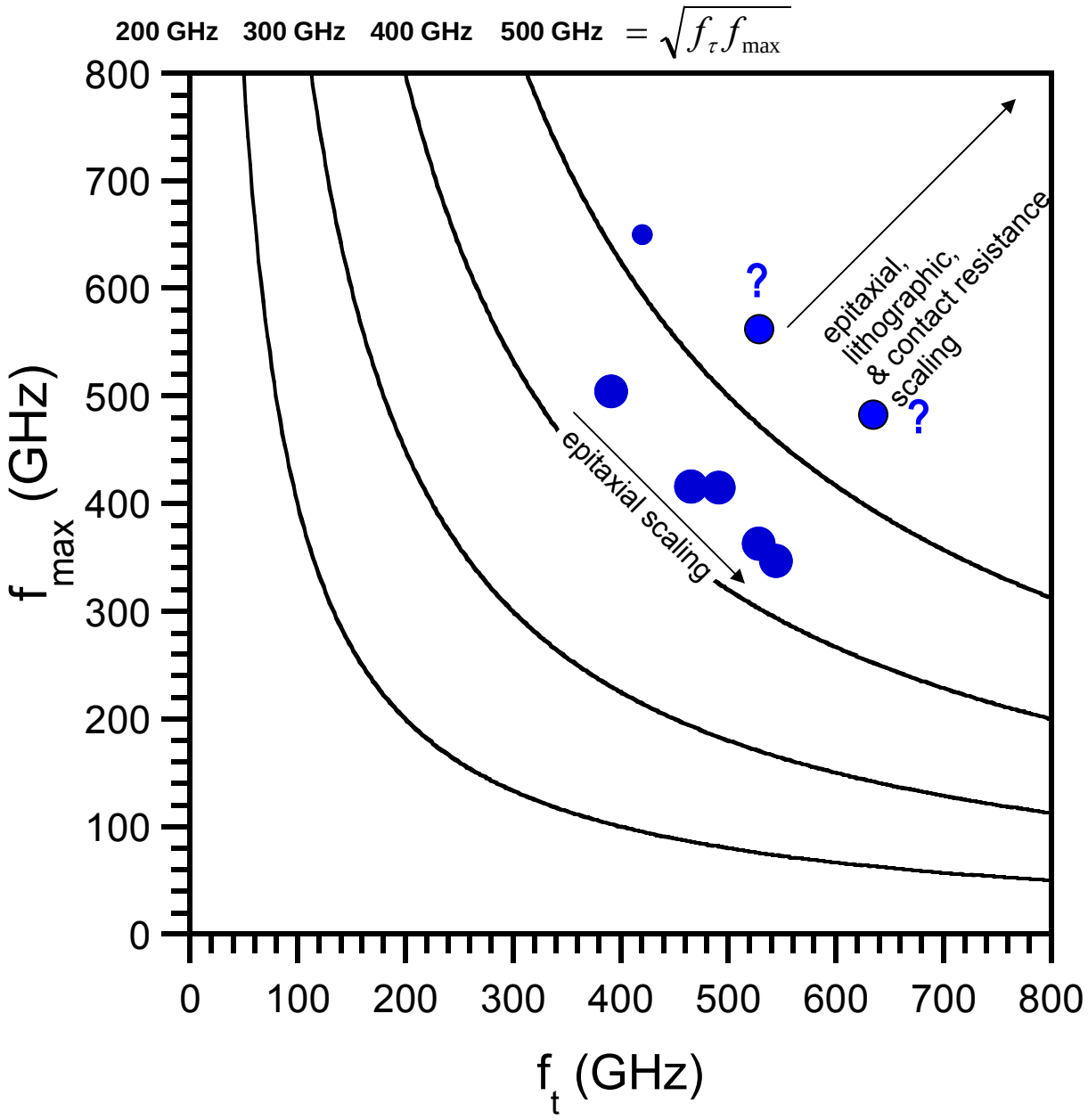
$(R_{bb} I_c / \Delta V)$,

$(\tau_b + \tau_c)$

Variation of Transistor Bandwidth with Scaling



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PAE, associated gain, mW/μm

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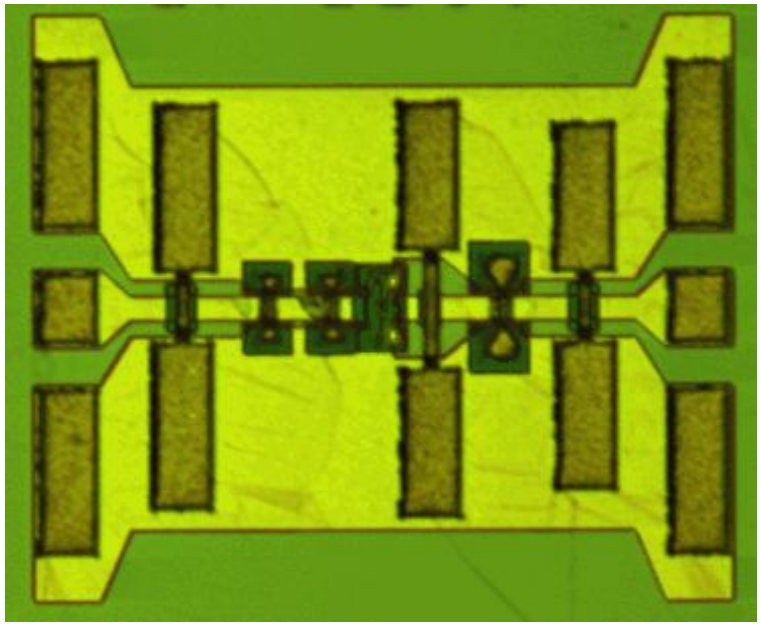
F_{min}, associated gain,

digital :

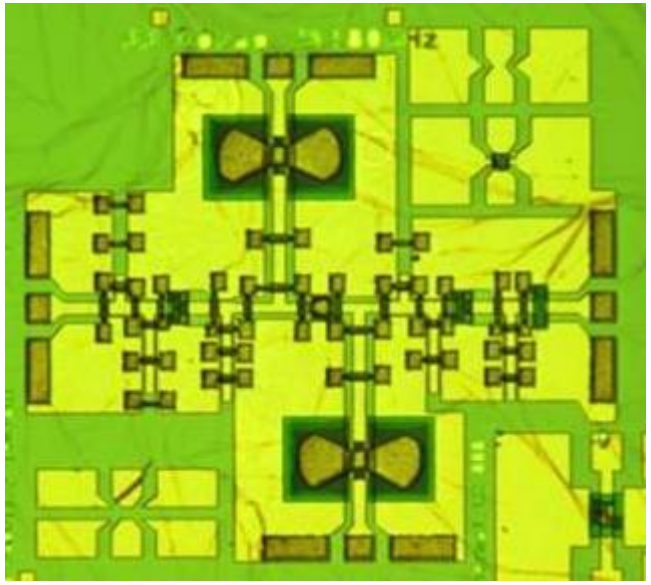
f_{clock}, hence $(C_{cb}\Delta V / I_c)$, $(R_{ex} I_c / \Delta V)$, $(R_{bb} I_c / \Delta V)$, $(\tau_b + \tau_c)$

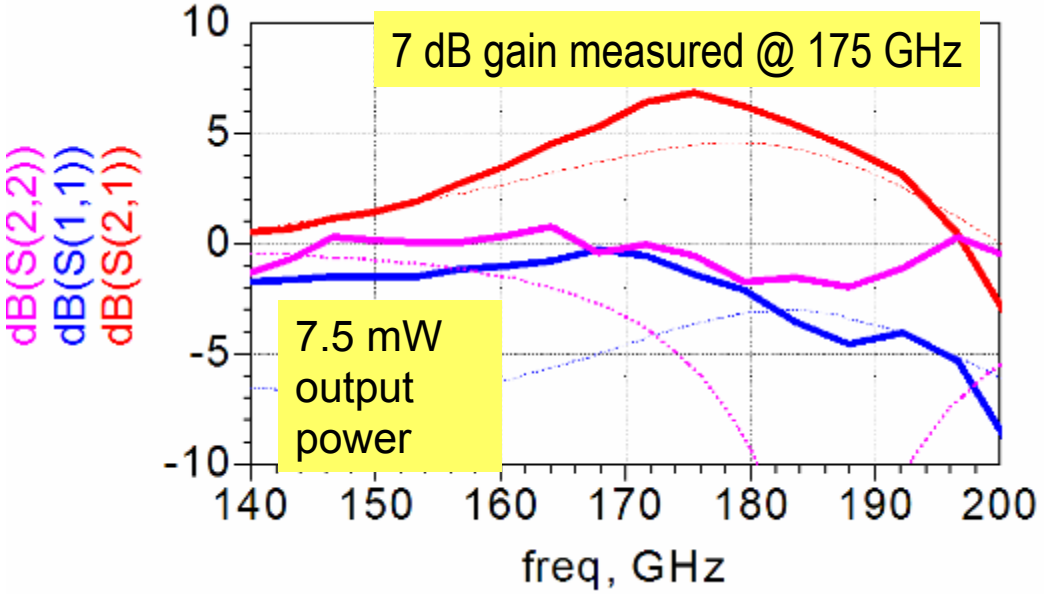
V. Paidi, Z. Griffith, M. Dahlström

175 GHz Amplifiers with 300 GHz f_{max} Mesa DHBTs

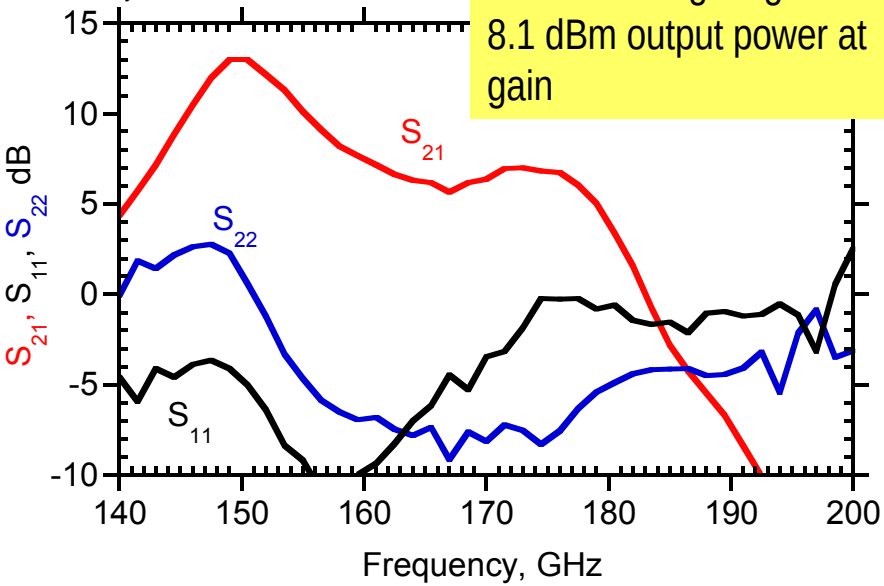


2 fingers x 0.8 um x 12 um, ~250 GHz f_{τ}, 300 GHz f_{max} , V_{br} ~ 7V, ~ 3 mA/um^2 current density



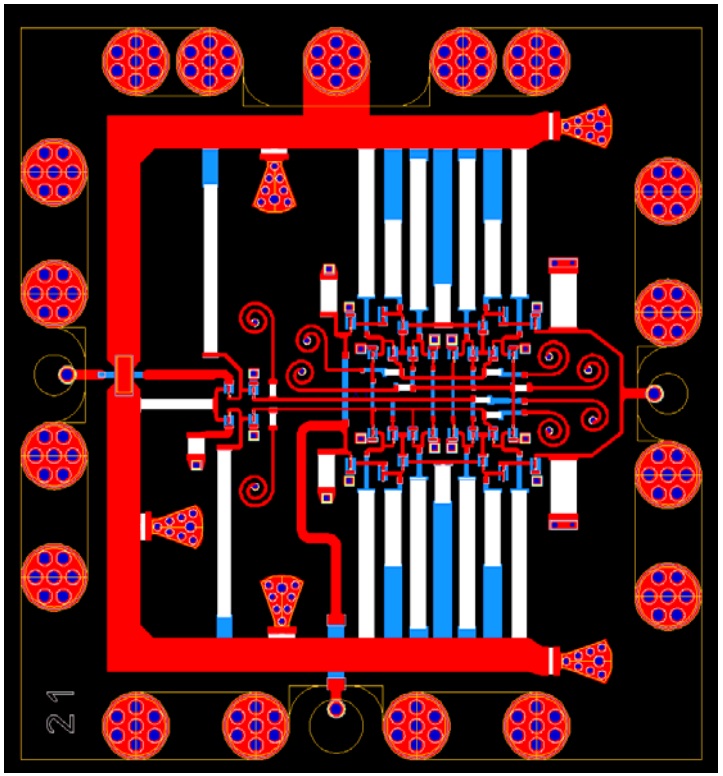


7-dB small-signal gain at 176 GHz
8.1 dBm output power at 6.3 dB gain

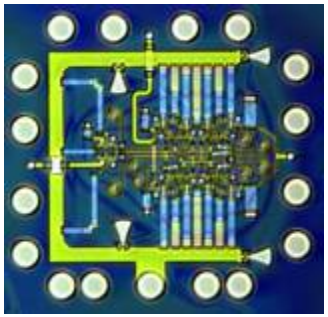


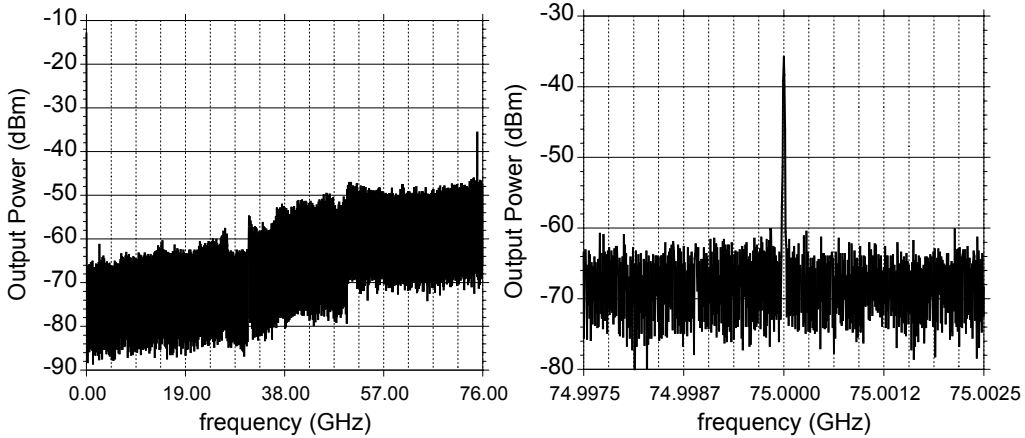
UCSB / RSC / GCS 150 GHz Static Frequency Dividers

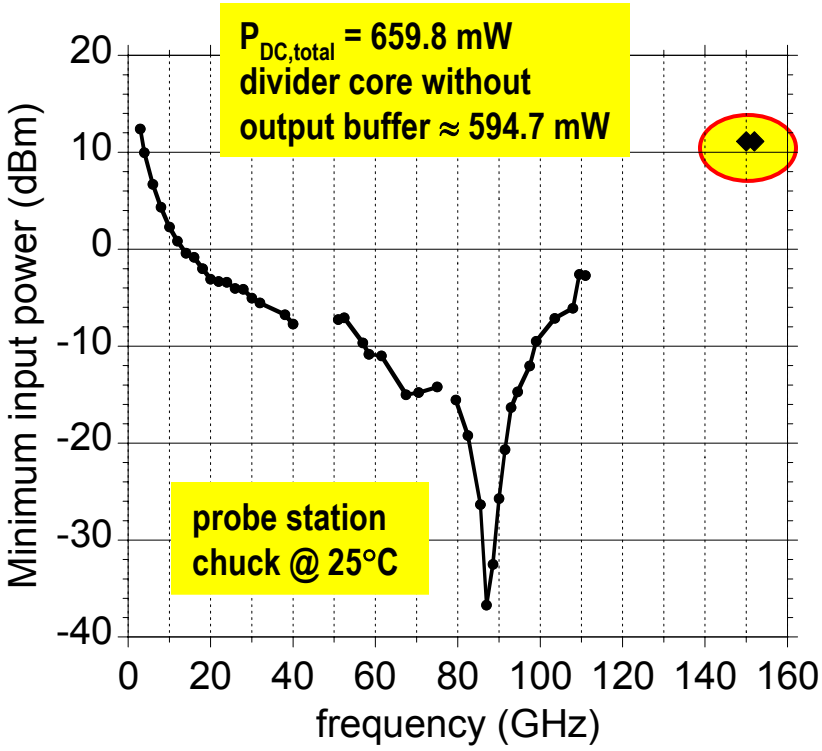
IC design: Z. Griffith, UCSB
HBT design: RSC / UCSB / GCS
IC Process / Fabrication: GCS
Test: UCSB / RSC / Mayo



	units	data current steering	data emitter followers	clock current steering	clock emitter followers
size	μm^2	0.5 x 3.5	0.5 x 4.5	0.5 x 4.5	0.5 x 5.5
current density	$mA/\mu m^2$	6.9	4.4	4.4	4.4
C_{cb}/I_c	psec / V	0.59	0.99	0.74	0.86
V_{cb}	V	0.6	0	0.6	1.7
f_τ	GHz	301	260	301	280
f_{max}	GHz	358	268	358	280



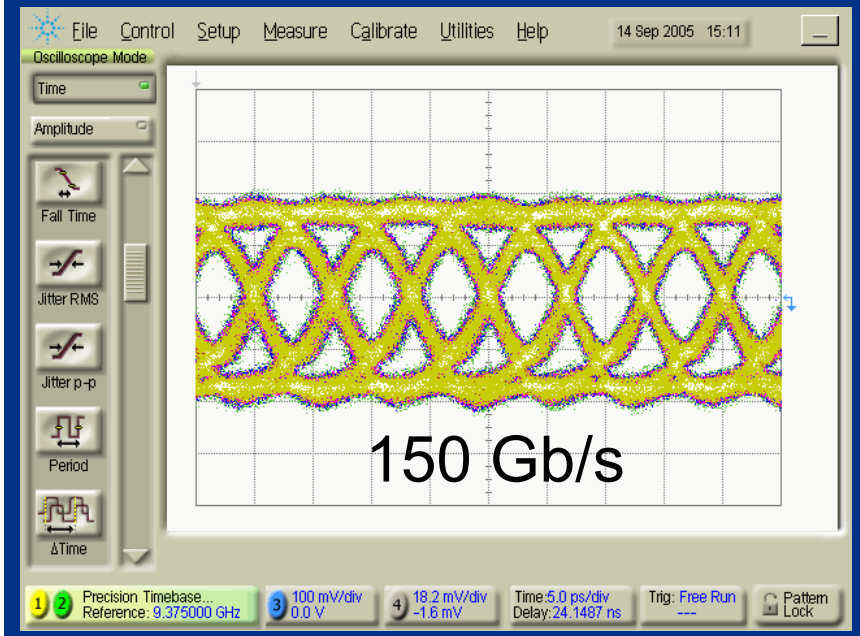


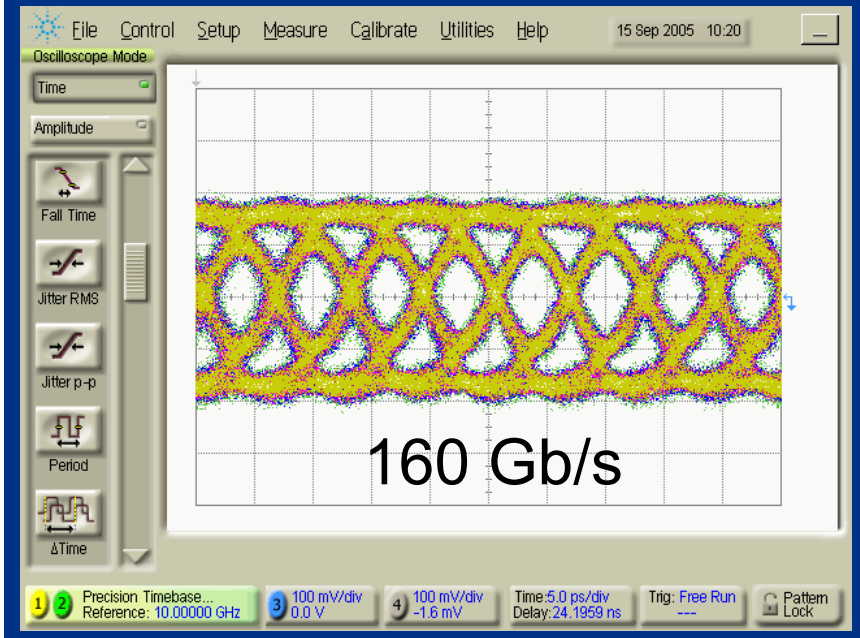


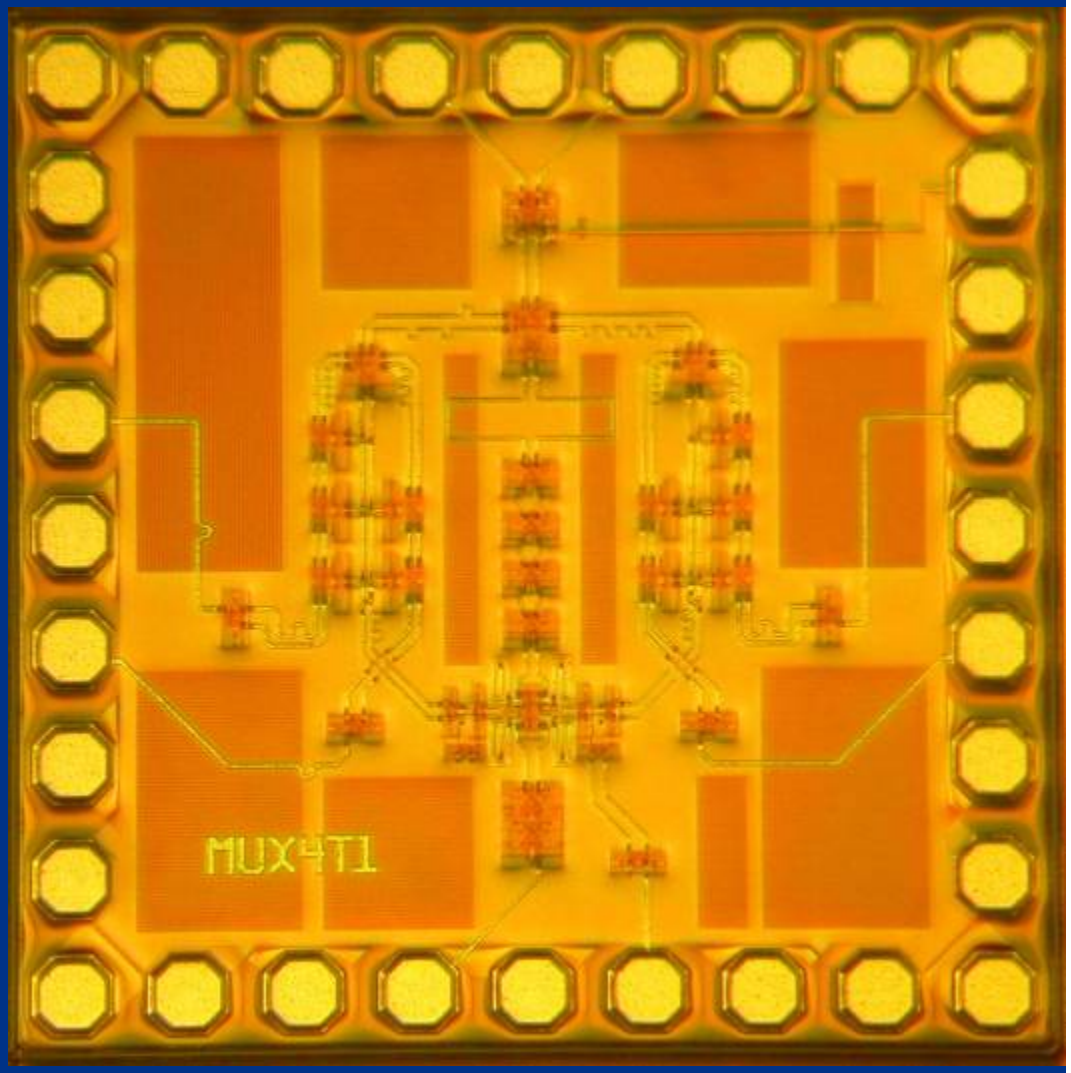
CHALMERS

4:1 Mux in Vitesse VIP3 InP HBT Process

T. Swahn *et al*



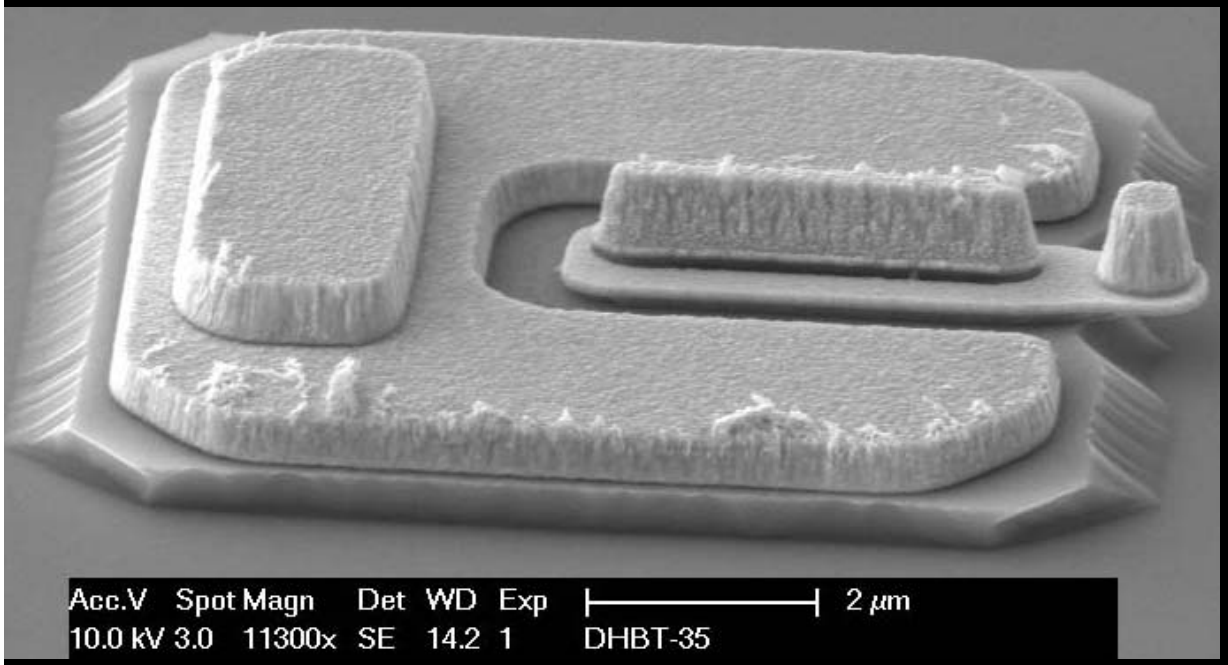


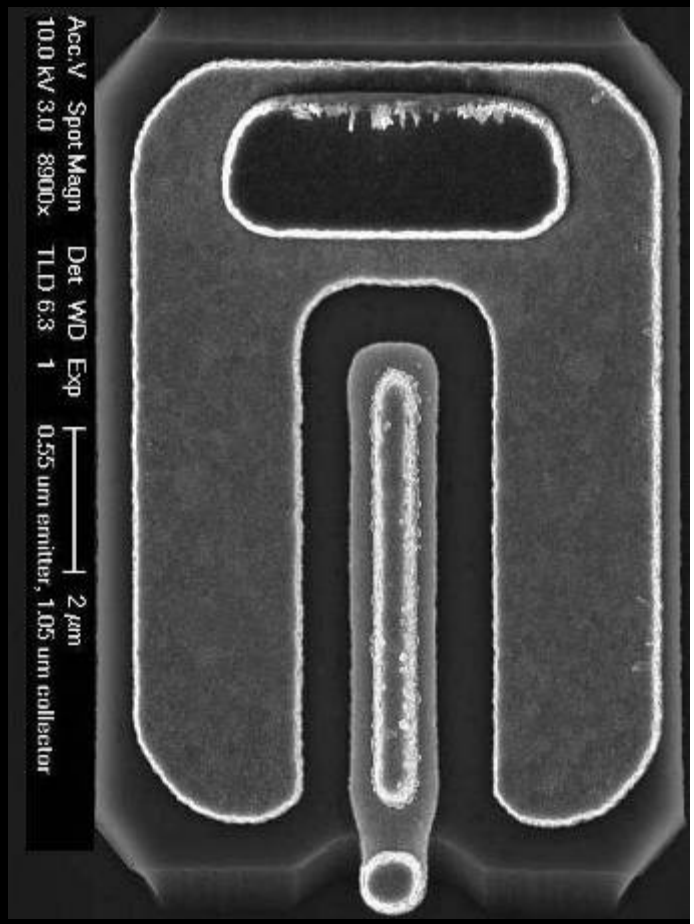


MC2

250 nm scaling generation DHBTs

Zach Griffith

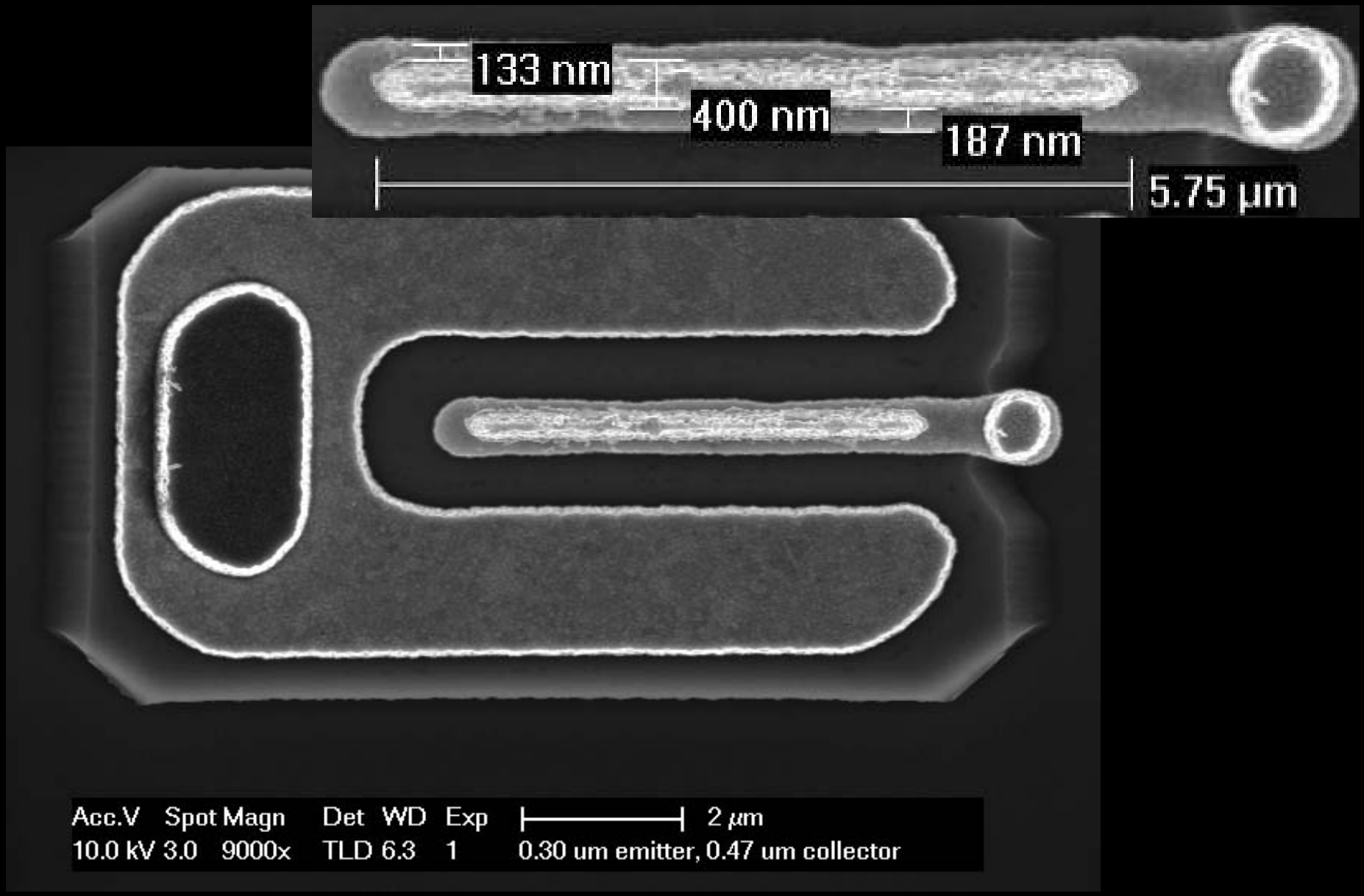




- 100 % I-line lithography
- Emitter contact resistance reduced 40%: from 8.5 to 5 $\Omega \cdot \mu m^2$
- Base contact resistance is < 5 $\Omega \cdot \mu m^2$ --hard to measure
- Recall, 1/8 μm scaling generation needs $\leq$ 5 $\Omega \cdot \mu m^2$ emitter ρ_c

Zach Griffith

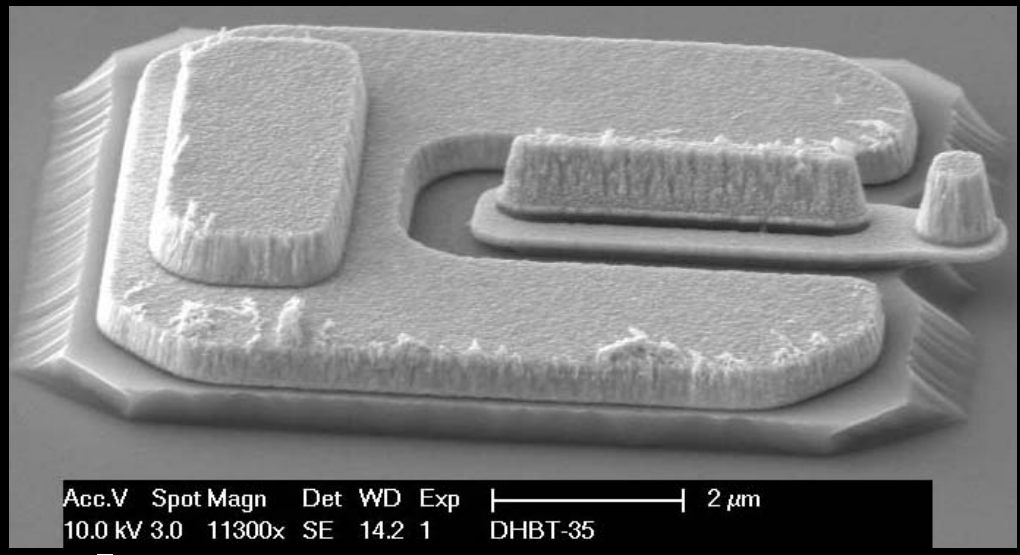
0.30 µm emitter junction, $W_c/W_e \sim 1.6$



First mm-wave results with 250 nm InP DHBTs

Erik Lind

150 nm material
250 nm emitter width

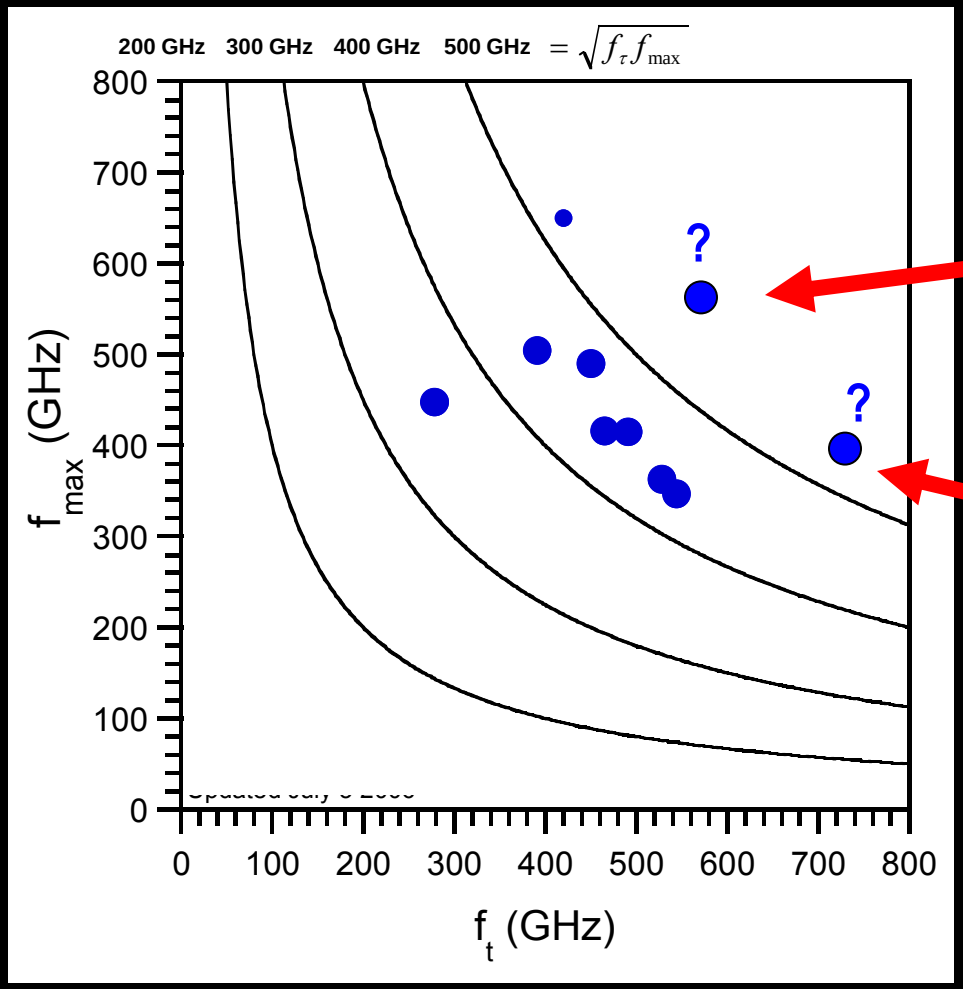


f_τ = 420 GHz
f_{max} = 650 GHz
~6 V breakdown
30 mW/um² power handling

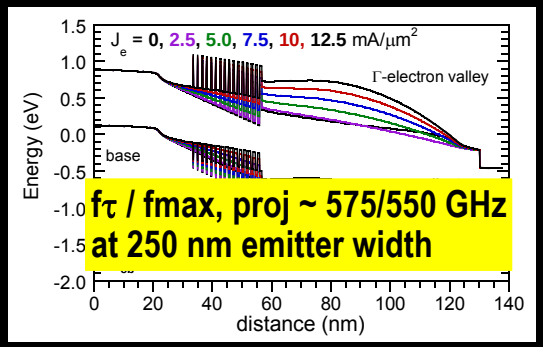
results to be presented postdeadline this conference, E. Lind, Z. Griffith et al

Epitaxial scaling at 250 nm design rules

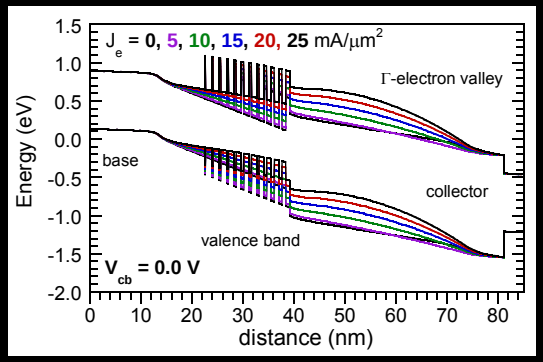
Zach Griffith



100 nm thick collector

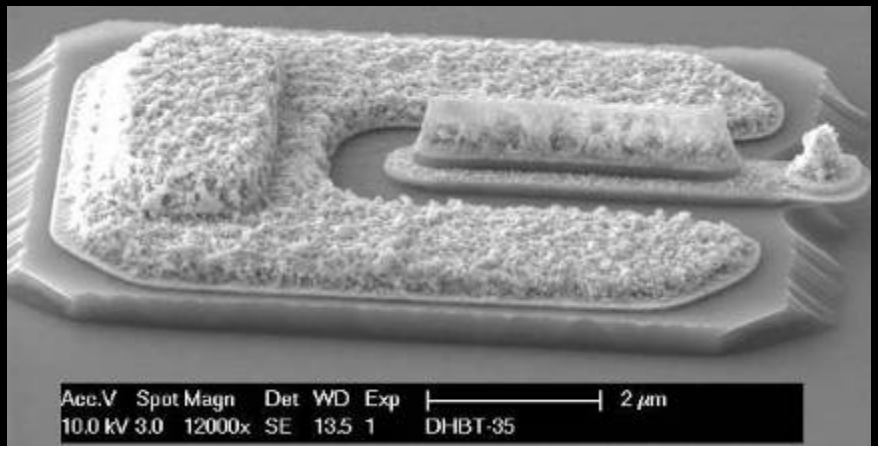


60 nm thick collector



process failure

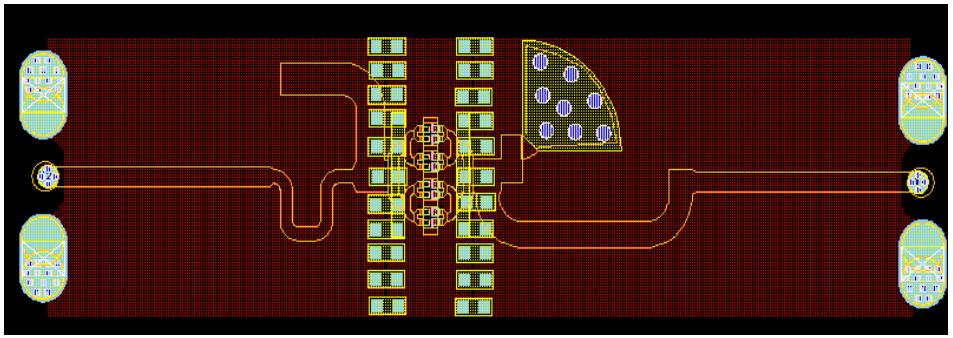
new fab run in progress

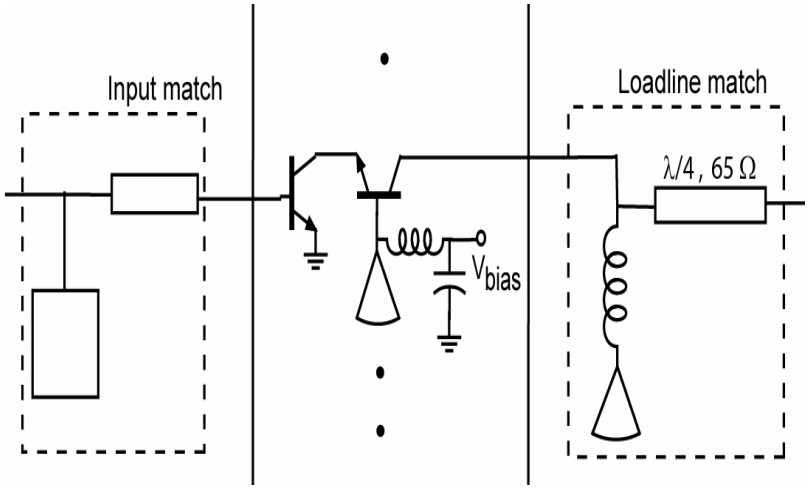


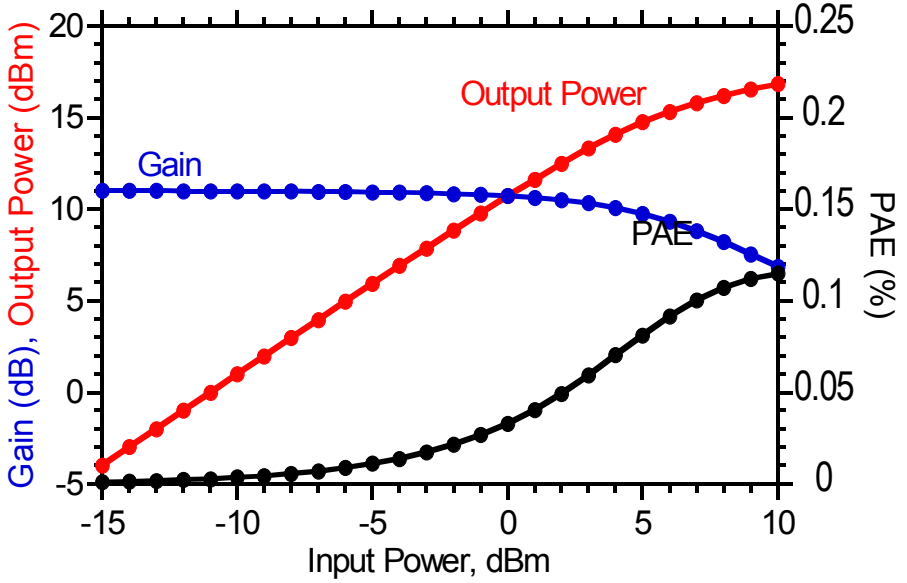
330 GHz Cascode Power Amplifiers In Design

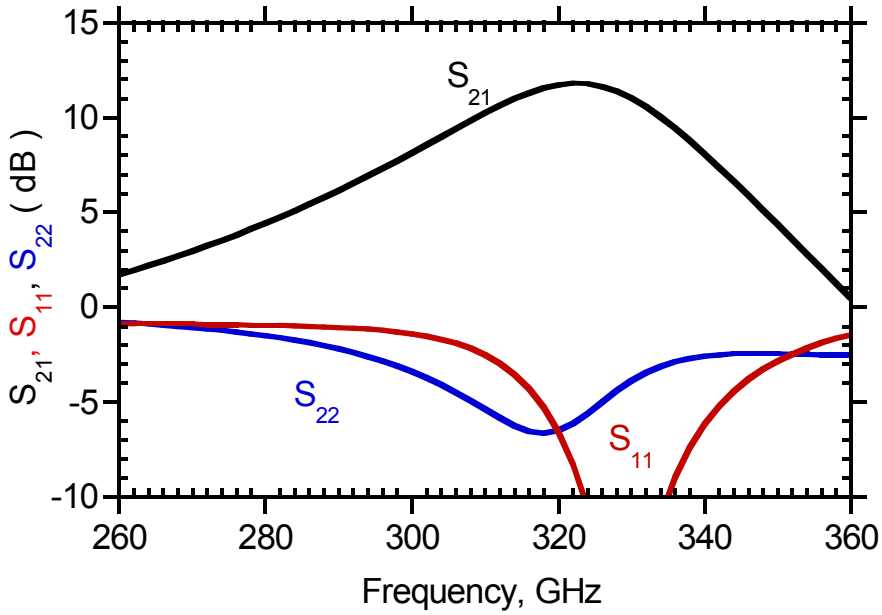
Navin Parthasarathy

P_{sat} = 50 mW (17 dBm)
10-dB associated power gain
use 650 GHz f_{max} transistors









Manufacturable Process Flows

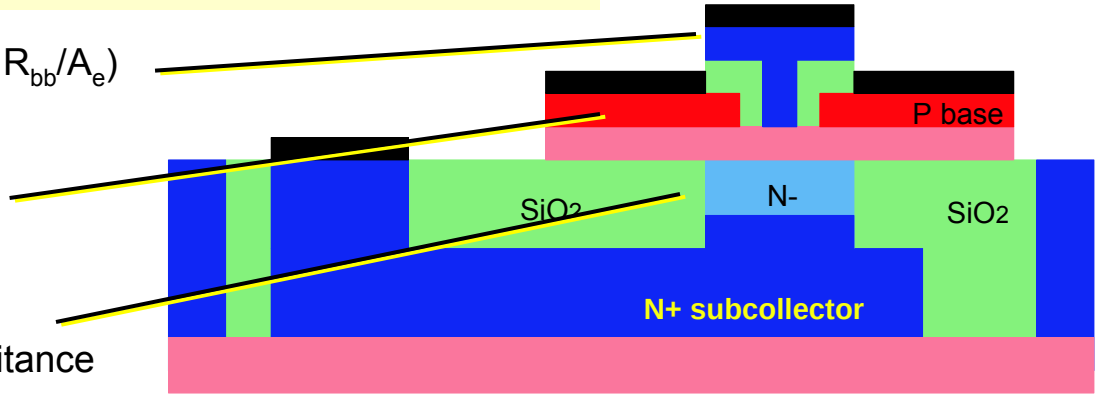
Parasitic Reduction for Improved InP HBT Bandwidth

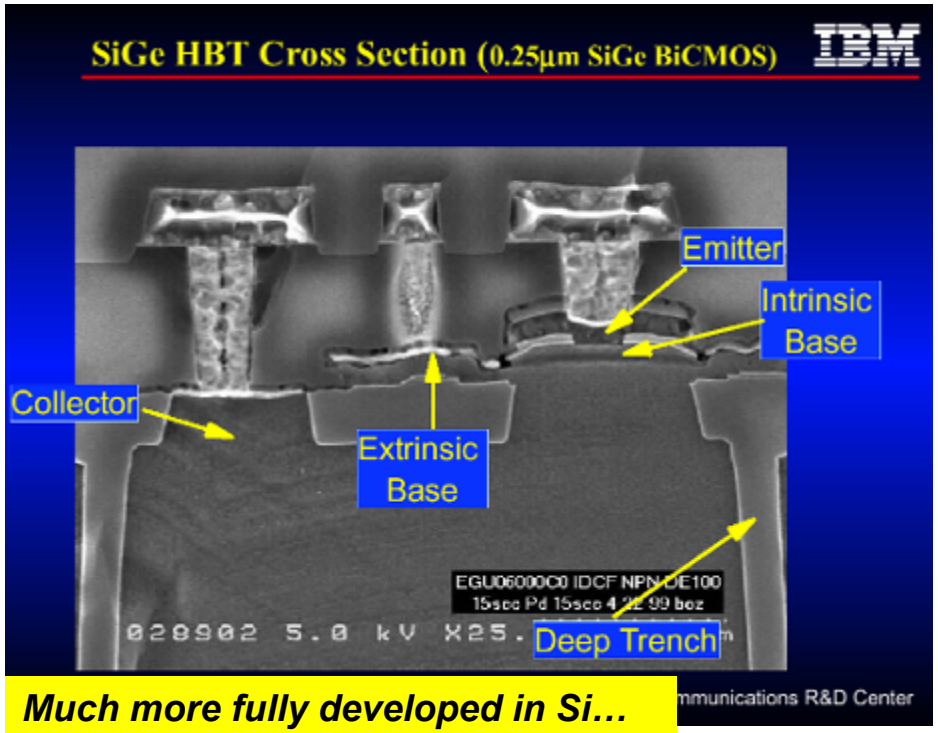
At a given scaling generation, intelligent choice of device geometry reduces extrinsic parasitics

wide emitter contact: low resistance
narrow emitter junction: scaling (low R_{bb}/A_e)

thick extrinsic base : low resistance
thin intrinsic base: low transit time

wide base contacts: low resistance
narrow collector junction: low capacitance





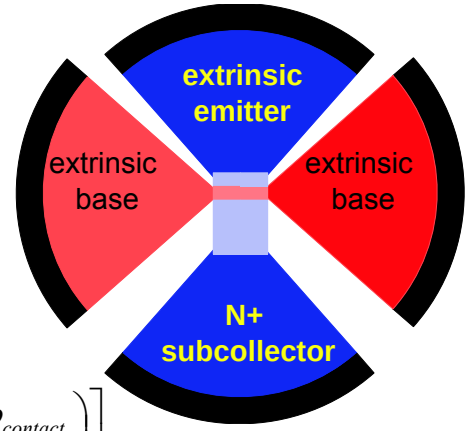
Much more fully developed in Si…

These are planar approximations to radial contacts:

$$R_{bulk} = \frac{2\rho_{bulk}}{\pi L}\ln\left(\frac{\sqrt{2}\cdot r}{W}\right)$$

$$R_{contact} = \frac{2\rho_c}{\pi L r}$$

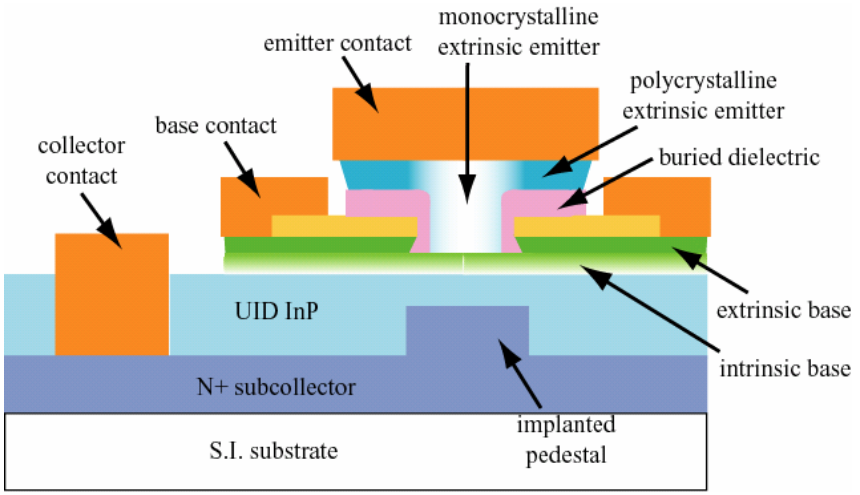
$$R_{\text{total,min}} = \frac{2\rho_{bulk}}{\pi L}\left[1.34 + \ln\left(\frac{\rho_{contact}}{W\rho_{bulk}}\right)\right]$$

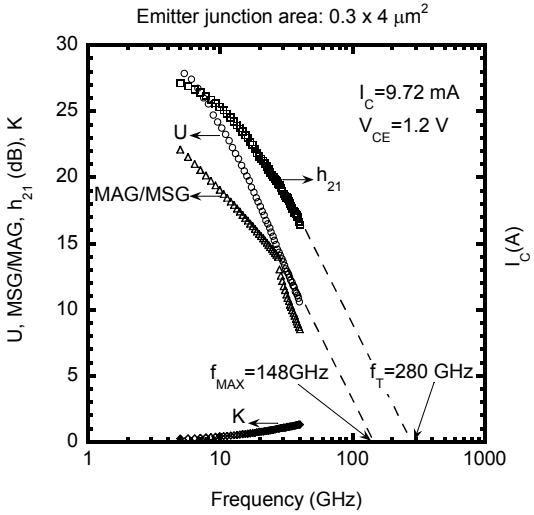


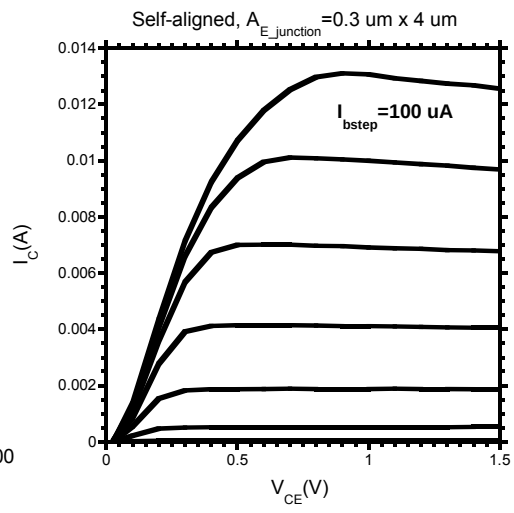
→ ***greatly reduced access resistance***

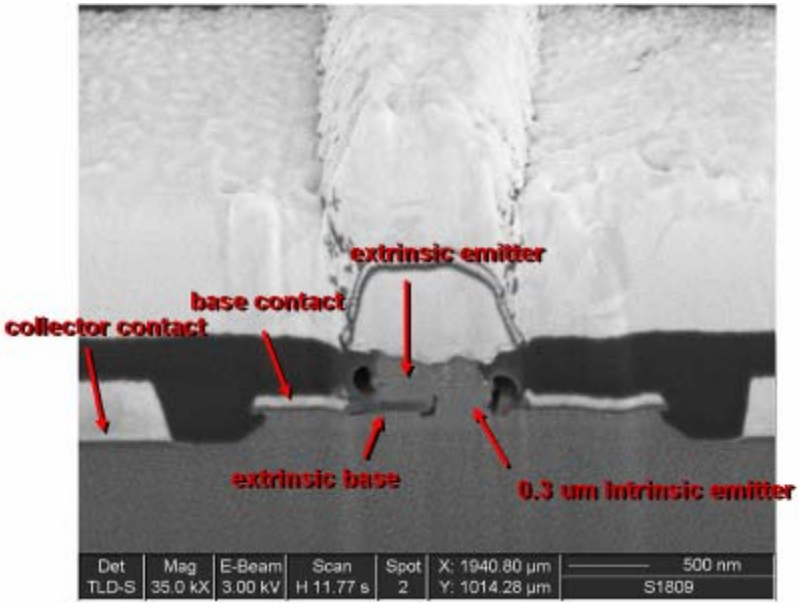
D. Scott, Y. Wei

Polycrystalline Extrinsic Emitter







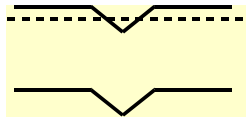


Approach

Wide emitter contact for low emitter access resistance
Thick extrinsic base for low base resistance
Self-aligned refractory base contacts

Enabling Technology

Low-resistance polycrystalline InAs
In-band Fermi-level pinning eliminates barriers



Challenges

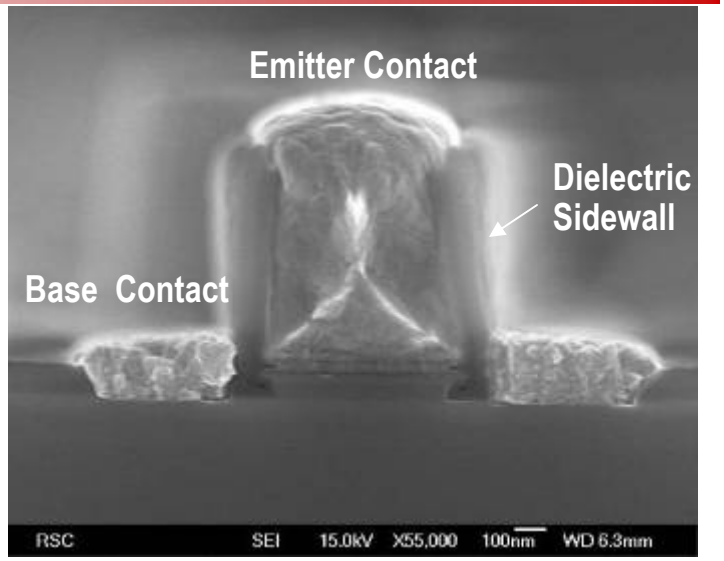
Very complex process
Hydrogen passivation
Resistance of Refractory contacts

Self-aligned Sidewall Spacer (S3) Manufacturable HBT Process

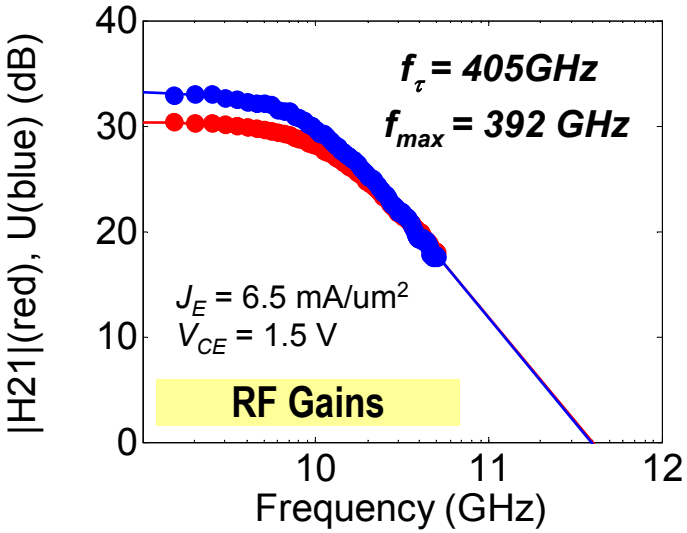
ROCKWELL SCIENTIFIC

Miguel Urteaga, Richard Pierson, Petra Rowell
Keisuke Shinohara, Berinder Brar

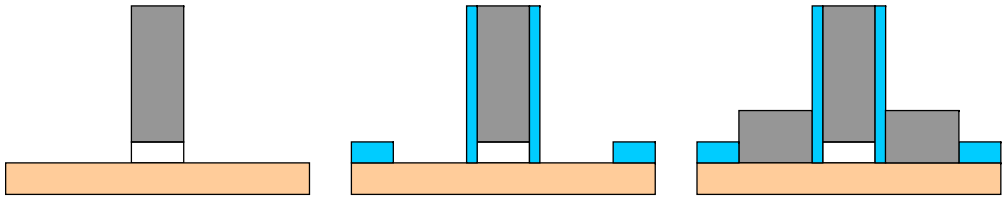
- Self-aligned contacts are critical to submicron device scaling. Eliminates lithography alignment tolerance.
- RSC's S3 HBT process utilizes electroplated contacts with dielectric sidewalls. Eliminates low yield liftoff processes from base-emitter junction formation.
- Electroplated base contact is *selectively* deposited on the base semiconductor.
- Process enables deep submicron scaling while maintaining high levels of *performance* and *yield*



SEM Cross-Section of B-E Junction



RF Gains

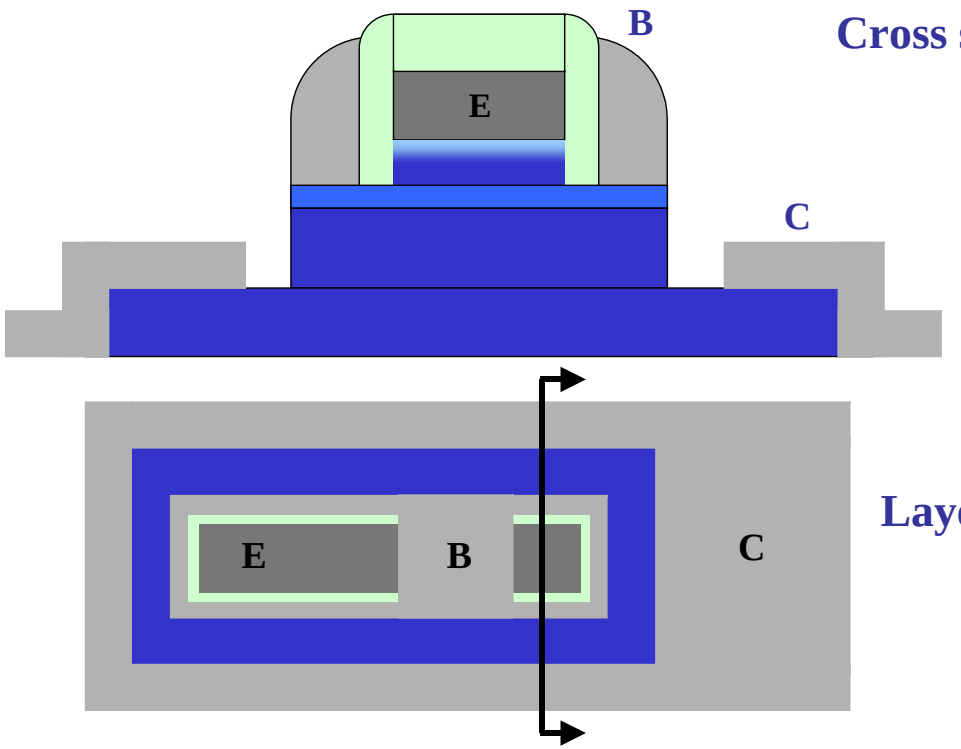


S3 Process Flow

VIP-2 HBT structure: Dielectric Sidewall

Minh Le *et al*

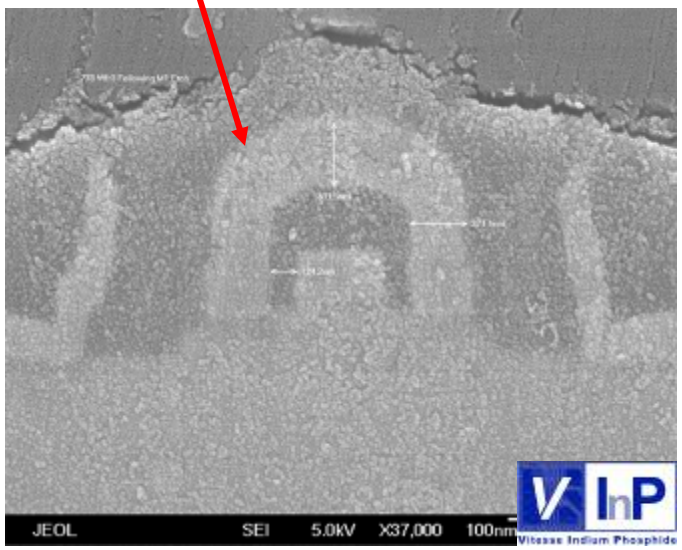
Dielectric Spacer allows tightly controlled separation between Emitter and Base to minimize Rbx and Cbcx



Cross section

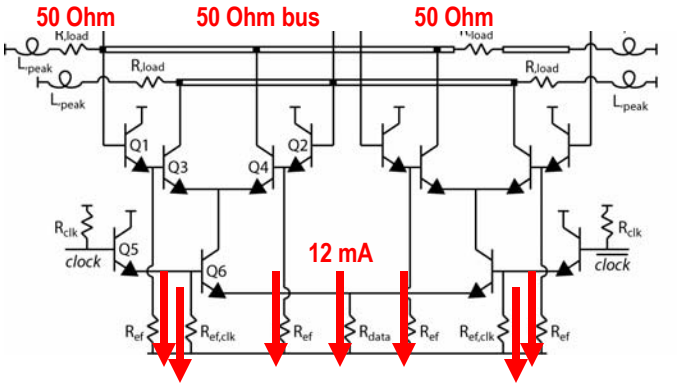
Layout

Note that the base via is "folded" on top of the transistor to reduce Cbc

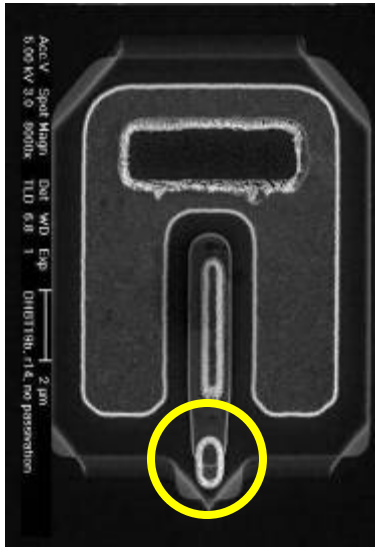


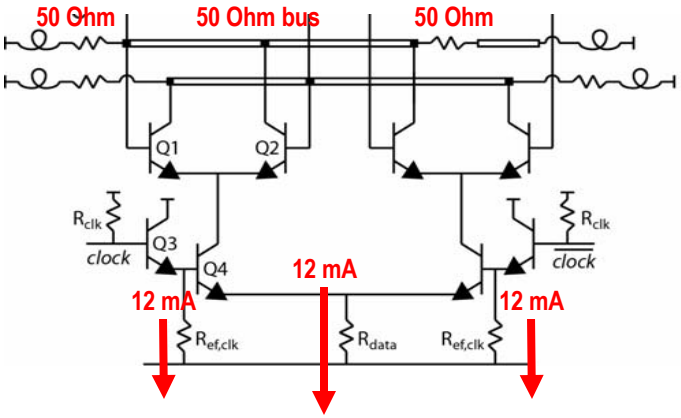
G. He, J. Howard, M. Le, P. Partyka, B. Li, G. Kim, R. Hess, R. Bryie, R. Lee, S. Rustomji, J. Pepper, M. Kail, M. Helix, R. Elder, D. Jansen, N. Harff, J. Prairie, E. Daniel, and B. Gilbert, "Self-Aligned InP DHBT with ft and fmax over 300 GHz in a new manufacturable technology," IEEE Electron Device Lett., vol. 25, no. 8, pp. 520–522, Aug. 2004.

Low-Power High-Speed Logic → Small Pad Capacitance

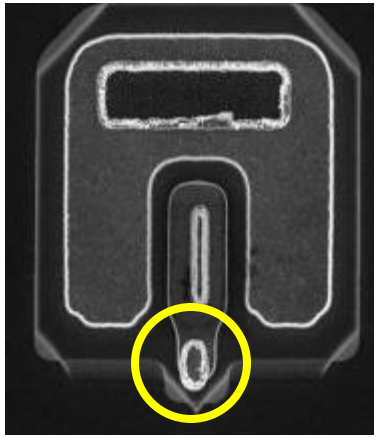


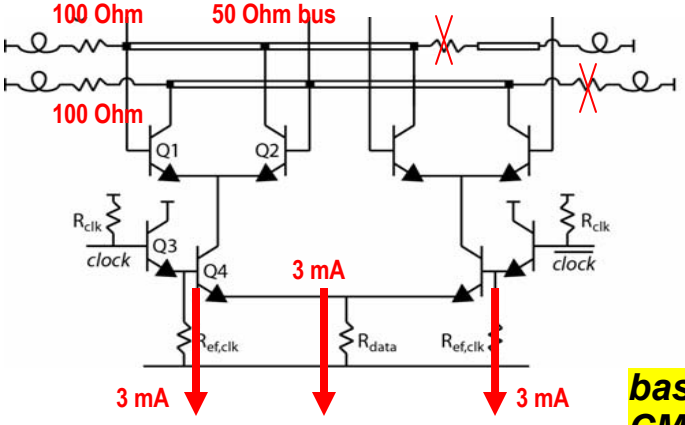
ECL with impedance-matched 50 Ohm bus:
25 Ohm load→ switch 12 mA
12 mA x 7 x 4 V = 336 mW/latch





CML with impedance-matched 50 Ohm bus:
25 Ohm load→ switch 12 mA
12 mA x 3 x 3 V = 108 mW/latch





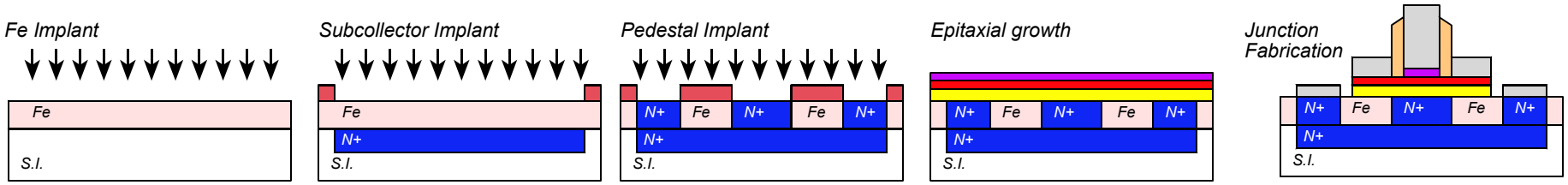
Low-Power CML
100 Ohm loaded → switch 3 mA
3 mA x 3 x 3 V = 27 mW/latch

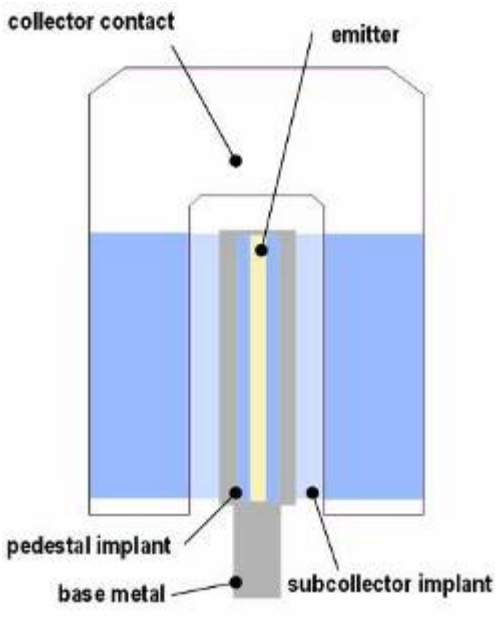
$$\text{High speed @ low power} = \text{low } C_{wiring}\text{, low } C_{cb,pad}$$

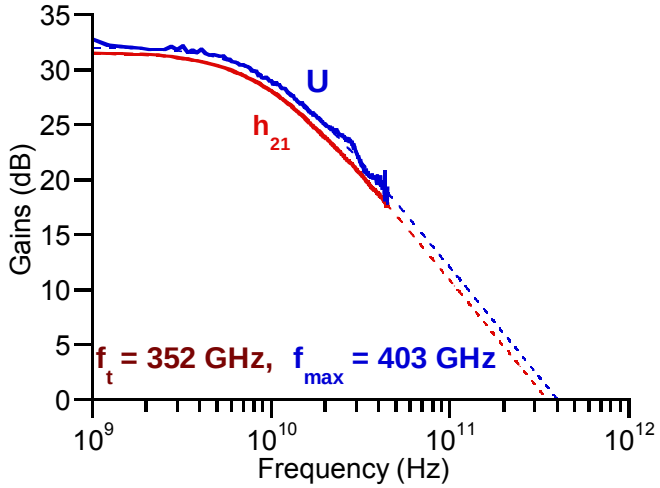
base pad capacitance key parasitic in low power bipolar logic
CML operates at lower Vce → reduced Kirk-effect-limited current

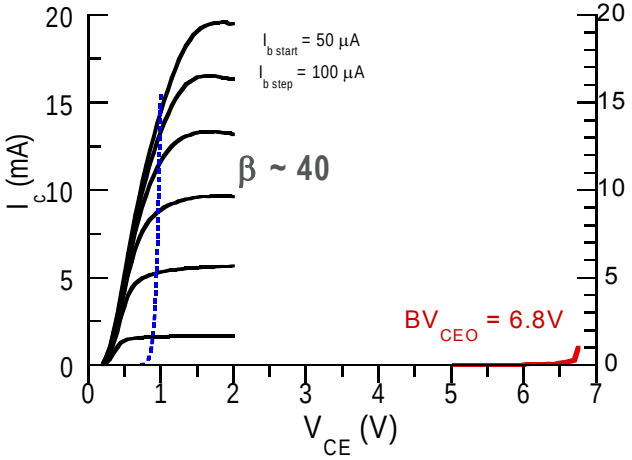
Navin Parthasarathy

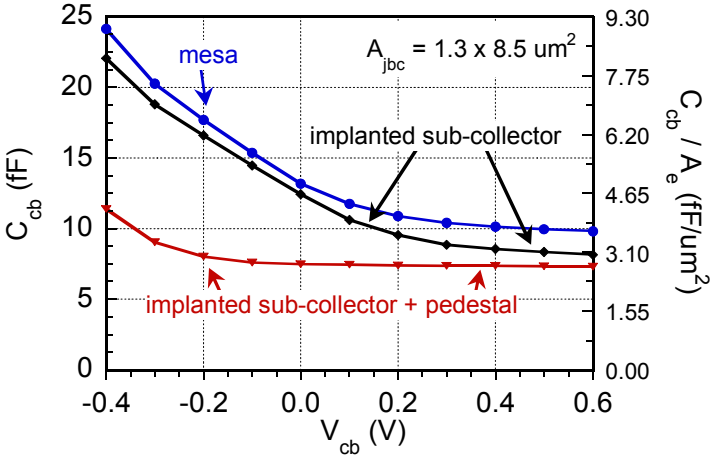
Subcollector & Pedestal Implant

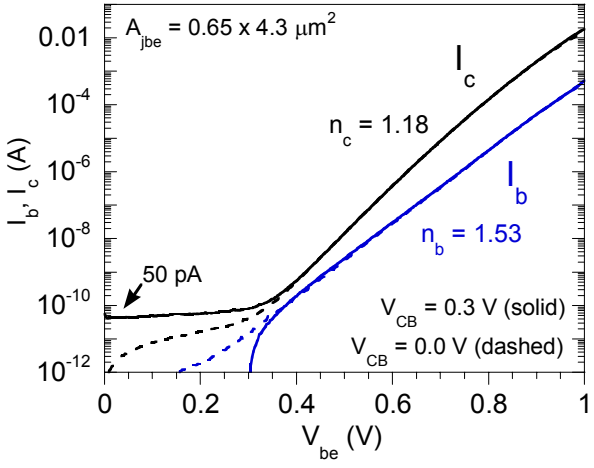








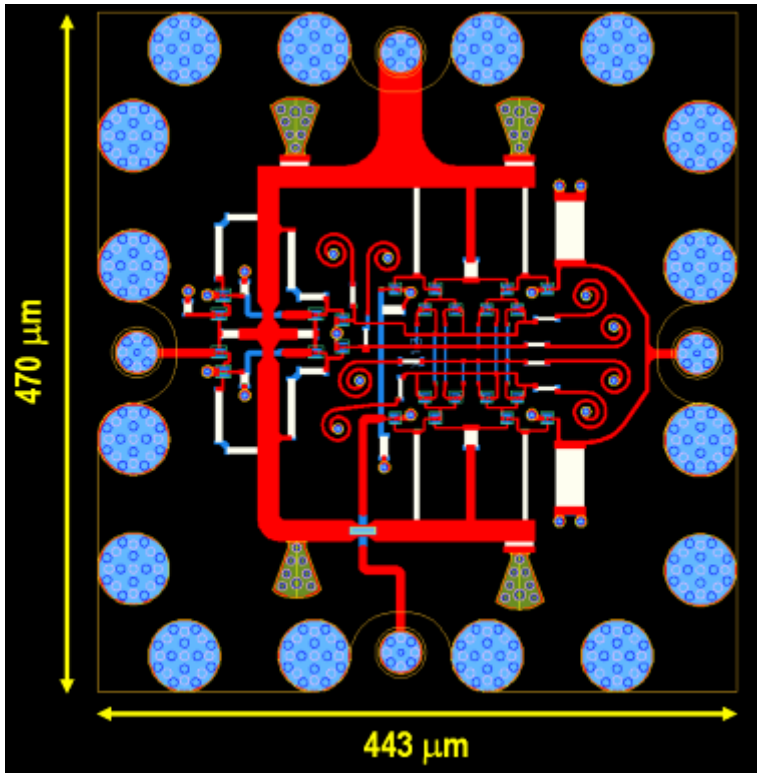


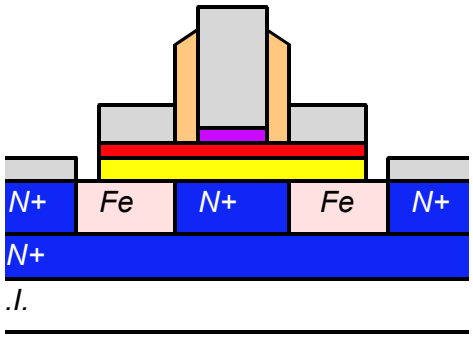


Subcollector implant eliminates C_{cb} in base pad area .

Pedestal further reduces C_{cb}.

Ultra low power CML Static Frequency Divider: RSC S³ Process with Pedestal





Without C_{cb} reduction

f_{max} = 51 GHz

With Pedestal

f_{max} = 61.2 GHz (measured)
f_{max} ~ 100 GHz (simulated)

$P_{divider\ core}$, ≈ 31 mW
(*includes* emitter follower buffers)

Low-Power IC Design:
Z. Griffith, N. Parthasarathy, M. Rodwell, M. Urteaga, K. Shinohara, P. Rowell, R. Pierson, and B. Brar
"An Ultra Low-Power (≤ 13.6 mW/latch) Static Frequency Divider in an InP/InGaAs DHBT Technology" ,
2006 IEEE IMS Symposium

Device technology, other higher-speed circuits,

M. Urteaga, K. Shinohara, R. Pierson, P. Rowell, B. Brar, Z. Griffith, N. Parthasarathy, M. Rodwell
" InP DHBT IC Technology with Implanted Collector-Pedestal and Electroplated Device Contacts" ,
submitted to IEEE CSIC Symposium

Frequency Limits of Bipolar Integrated Circuits

500 nm generation: Done

~475 GHz f_t & f_{max}

150 GHz static dividers (digital ICs)

250 nm results coming very soon.

expect ~225 GHz digital clock rate, 300-400 GHz amplifiers

125 nm devices are the next target .

→ 300 GHz digital clock rate, 600 GHz amplifiers

THz transistors will come

The approach is scaling.

The limits are contact & thermal resistance

serious challenge: volume applications to support development