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Frequency Limits of Bipolar Integrated Circuits

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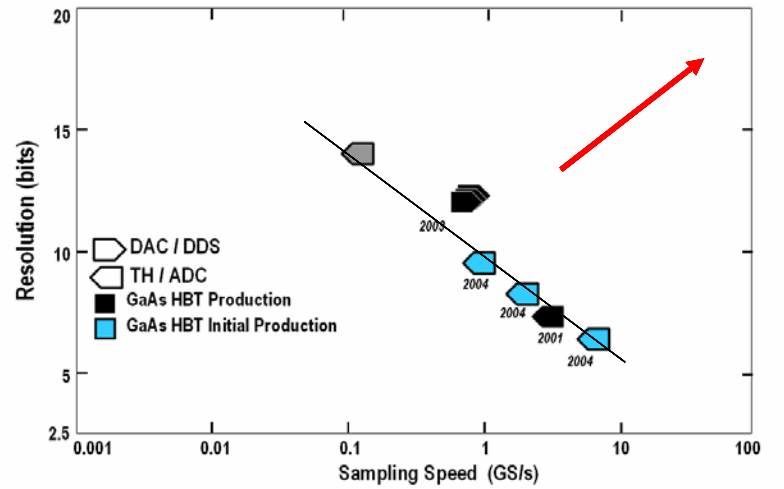
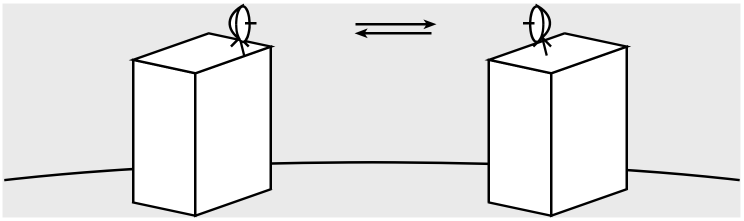
THz Transistors:
What does this mean ?
What are they for ?
How do we make them ?

What could we do with a THz Transistor ?

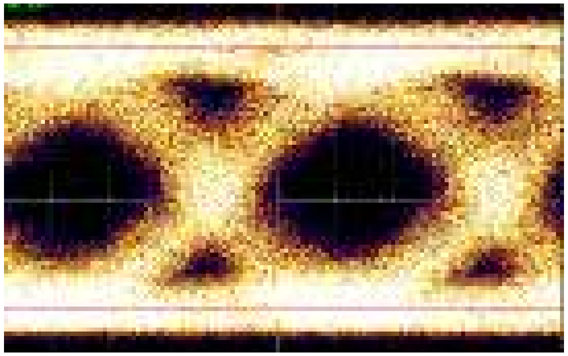
High-Resolution Microwave ADCs and DACs



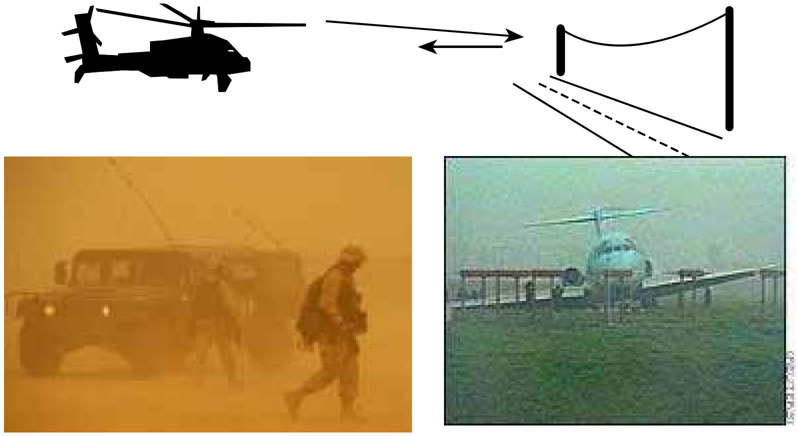
mm-wave radio:
40+ Gb/s on 250 GHz carrier



320 Gb/s fiber optics



340 GHz imaging systems



Why develop transistors for mm-wave & sub-mm-wave applications ?
→ compact ICs supporting complex high-frequency systems.

THz Transistors: What does this mean ?

A 1 THz current-gain cutoff frequency (f_τ) alone has little value

a transistor with 1000 GHz f_τ and 100 GHz f_{max}
cannot amplify a 101 GHz signal

RF-ICs & MIMICs need high power-gain cutoff frequency (f_{max})

also need high breakdown
& high safe operating area (power density)

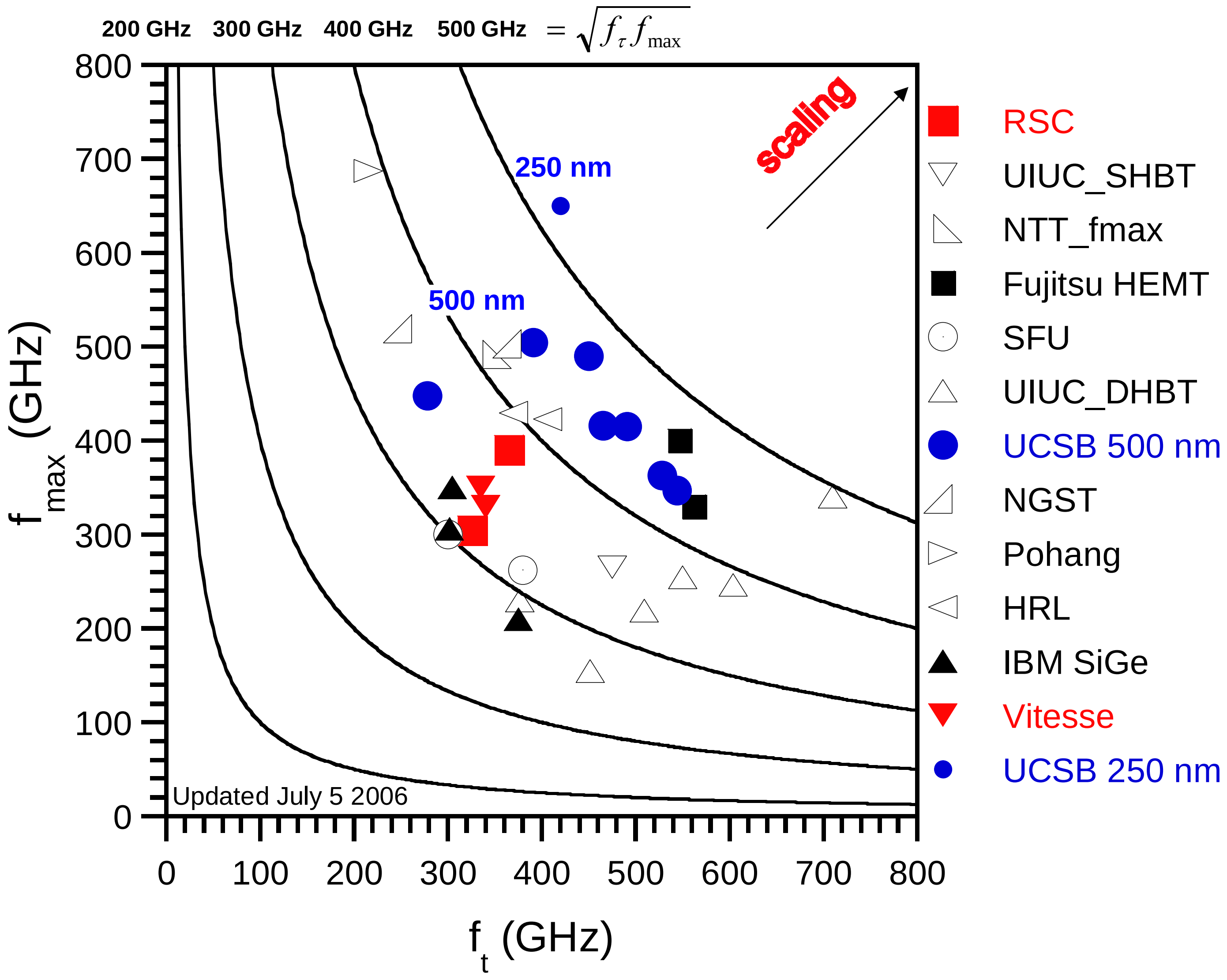
100+ GHz digital also needs

low ($C_{depletion}\Delta V / I$) and low ($I*R_{parasitic}/\Delta V$)

So, how do we make a transistor with
>1 THz f_τ , >1 THz f_{max}
<50 fs $C\Delta V / I$ charging delays
and < 100 mV ($I*R_{parasitic}$) parasitic voltage drops ?

THZ Transistors: How do we make them ?

Present Status of Fast III-V Transistors



popular metrics :

f_τ or $f_{\max}$ alone

$(f_\tau + f_{\max})/2$

$\sqrt{f_\tau f_{\max}}$

$(1/f_\tau + 1/f_{\max})^{-1}$

much better metrics :

power amplifiers:

PAE, associated gain,

mW/μm

low noise amplifiers:

$F_{\min}$, associated gain,

digital:

f_{clock}, hence

$(C_{cb}\Delta V / I_c)$,

$(R_{ex} I_c / \Delta V)$,

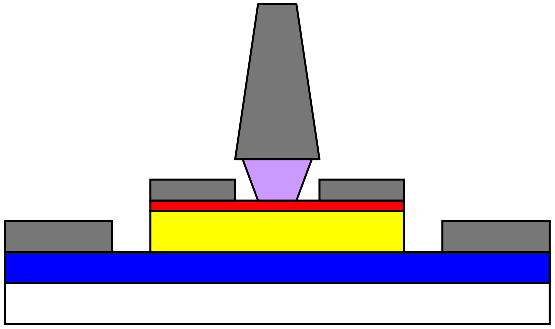
$(R_{bb} I_c / \Delta V)$,

$(\tau_b + \tau_c)$

Red = manufacturable technology for 10,000- transistor ICs

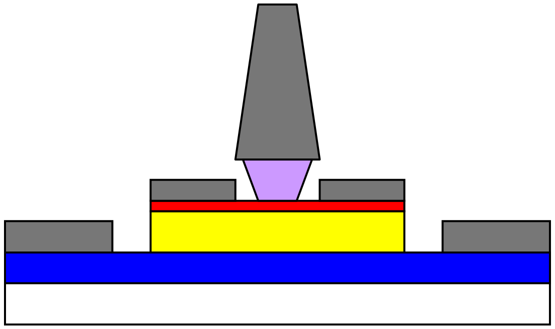
Bipolar Transistor Scaling Laws

Design changes required to double transistor bandwidth



key device parameter	required change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter resistance per unit emitter area	decrease 4:1
current density	increase 4:1
base contact resistivity (if contacts lie above collector junction)	decrease 4:1
base contact resistivity (if contacts do not lie above collector junction)	unchanged

InP HBT Scaling Roadmaps



Parameter	scaling law	Gen. 2 (500 nm)	Gen. 3 (250 nm)	Gen. 4 (125 nm)	Gen 5 (62.5nm)
MS-DFF speed	γ^1	150 GHz	235 GHz	330 GHz	440 GHz
Amplifier center frequency	γ^1	245 GHz	400 GHz	650 GHz	750 GHz
Emitter Width	$1/\gamma^2$	500 nm	250 nm	125 nm	62.5 nm
Resistivity	$1/\gamma^2$	$16\ \Omega\text{-}\mu m^2$	$9\ \Omega\text{-}\mu m^2$	$4\ \Omega\text{-}\mu m^2$	$2\ \Omega\text{-}\mu m^2$
Base Thickness	$1/\gamma^{1/2}$	300Å	250 Å	212 Å	180 Å
Contact width	$\sim 1/\gamma^2$	300 nm	175 nm	120 nm	70 nm
Doping	γ^0	$7\ 10^{19}\ /cm^2$	$7\ 10^{19}\ /cm^2$	$7\ 10^{19}\ /cm^2$	$7\ 10^{19}\ /cm^2$
Sheet resistance	$\gamma^{1/2}$	500 Ω	600 Ω	707 Ω	830 Ω
Contact ρ	$1/\gamma^{1/2}$	$20\ \Omega\text{-}\mu m^2$	$10\ \Omega\text{-}\mu m^2$	$5\ \Omega\text{-}\mu m^2$	$5\ \Omega\text{-}\mu m^2$
Collector Width	$1/\gamma^2$	1.2 μm	0.60 μm	0.37 μm	0.20 μm
Thickness	$1/\gamma$	1500 Å	1060 Å	750 Å	530 Å
Current Density	γ^2	4.5 $mA/\mu m^2$	9 $mA/\mu m^2$	18 $mA/\mu m^2$	36 $mA/\mu m^2$
$A_{collector}/A_{emitter}$	γ^0	2.4	2.4	2.9	2.8
f_τ	γ^1	370 GHz	530 GHz	730 GHz	1.0 THz
f_{max}	γ^1	490 GHz	801 GHz	1.30 THz	1.5 THz
I_E / L_E	γ^0	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm
τ_f	$1/\gamma$	340 fs	240 fs	180 fs	130 fs
C_{cb} / I_c	$1/\gamma$	400 fs/V	280 fs/V	250 fs/V	190 fs/V
$C_{cb}\Delta V_{logic} / I_c$	$1/\gamma$	120 fs	85 fs	74 fs	57 fs
$R_{bb}/(\Delta V_{logic} / I_c)$	γ^0	0.76	0.54	0.34	0.39
$C_{je}(\Delta V_{logic} / I_C)$	$1/\gamma^{3/2}$	380 fs	180 fs	94 fs	50 fs
$R_{ex}/(\Delta V_{logic} / I_c)$	γ^0	0.24	0.24	0.24	0.24

key figures of merit for logic speed

Key scaling challenges →

emitter & base contact resistivity

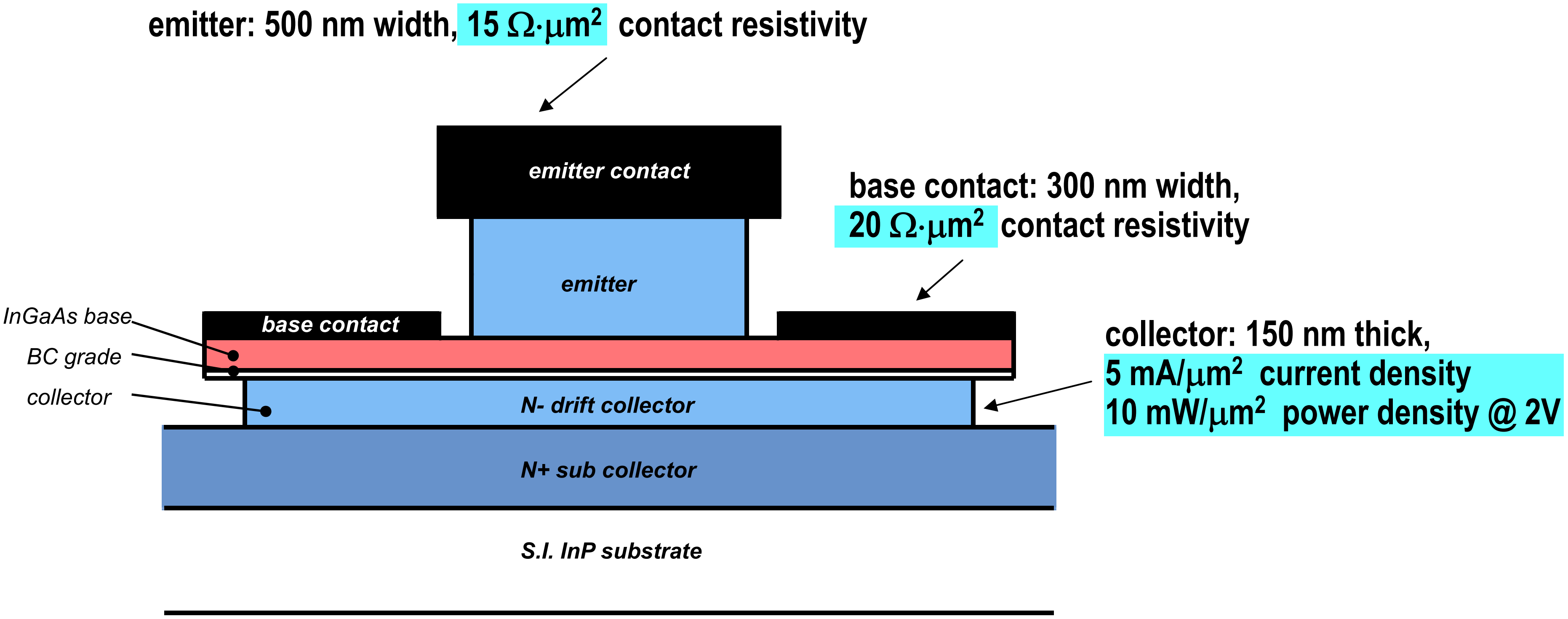
current density→ device heating

collector-base junction width scaling

& Yield !

2005: InP DHBTs @ 500 nm Scaling Generation

Target Performance:
400 GHz f_τ
500 GHz f_{max}
150 GHz digital clock rate (static dividers)
250 GHz power amplifiers



emitter: 500 nm width, 15 $\Omega\cdot\mu m^2$ contact resistivity

base contact: 300 nm width, 20 $\Omega\cdot\mu m^2$ contact resistivity

collector: 150 nm thick,
5 mA/μm^2 current density
10 mW/μm^2 power density @ 2V

2006: 250 nm Scaling Generation, 1.414:1 faster

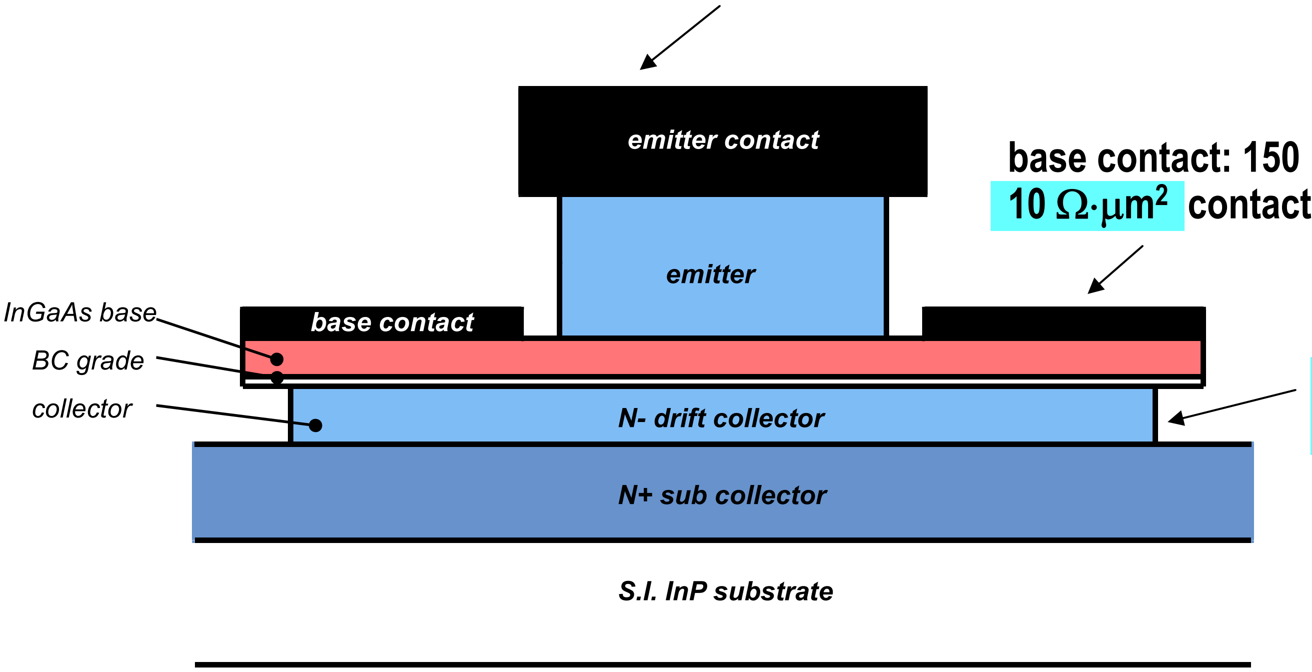
Target Performance:

500 GHz f_τ

700 GHz f_{max}

230 GHz digital clock rate (static dividers)

400 GHz power amplifiers



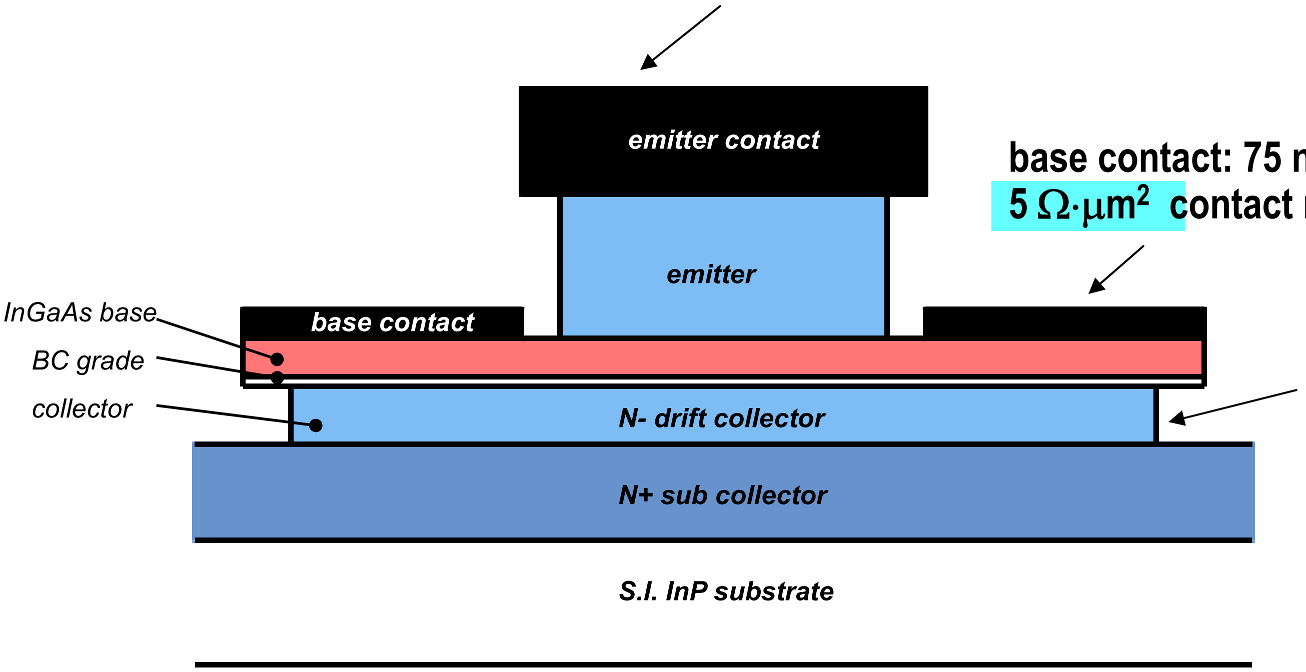
emitter: 250 nm width, 7.5 $\Omega\cdot\mu m^2$ contact resistivity

base contact: 150 nm width,
10 $\Omega\cdot\mu m^2$ contact resistivity

collector: 100 nm thick,
10 $mA/\mu m^2$ current density
20 $mW/\mu m^2$ power density @ 2V

125 nm Scaling Generation→ almost-THz HBT

Target Performance:
700 GHz f_τ
~1000 GHz f_{max}
330 GHz digital clock rate (static dividers)
600 GHz power amplifiers



emitter: 125 nm width, $5\ \Omega\cdot\mu m^2$ contact resistivity

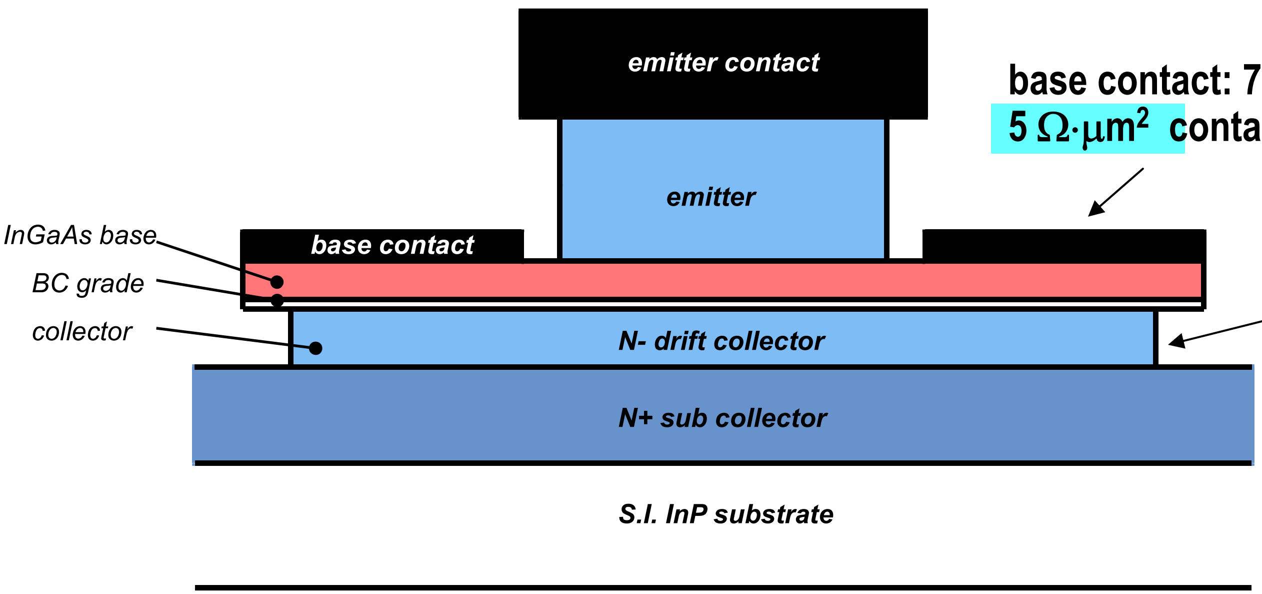
base contact: 75 nm width,
$5\ \Omega\cdot\mu m^2$ contact resistivity

collector: 75 nm thick,
$20\ mA/\mu m^2$ current density
$40\ mW/\mu m^2$ power density @ 2V

~3-4 V breakdown (BVCEO)

65 nm Scaling Generation→beyond 1-THz HBT

Target Performance:
1.0 THz f_τ
1.7 GHz f_{max}
450 GHz digital clock rate (static dividers)
1 THz power amplifiers



emitter: 62.5 nm width, 2.5 $\Omega\cdot\mu m^2$ contact resistivity

base contact: 70 nm width,
5 $\Omega\cdot\mu m^2$ contact resistivity

collector: 53 nm thick,
35 $mA/\mu m^2$ current density
70 $mW/\mu m^2$ power density @ 2V
→ 2-3 V breakdown (BVCEO)

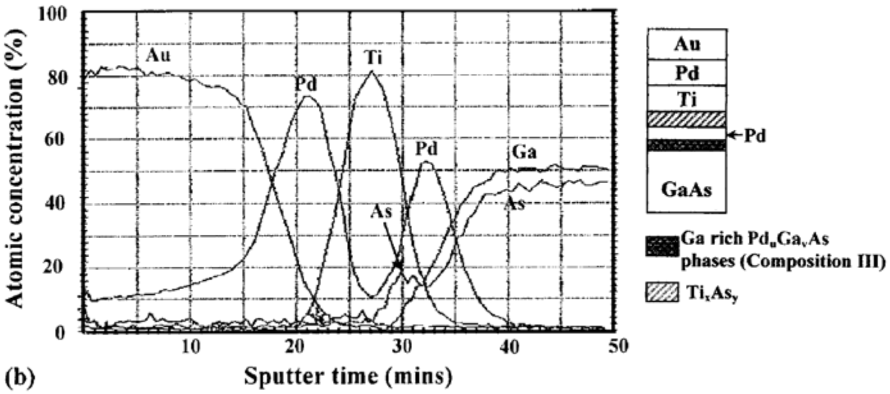
THZ Transistors: addressing the key scaling challenges

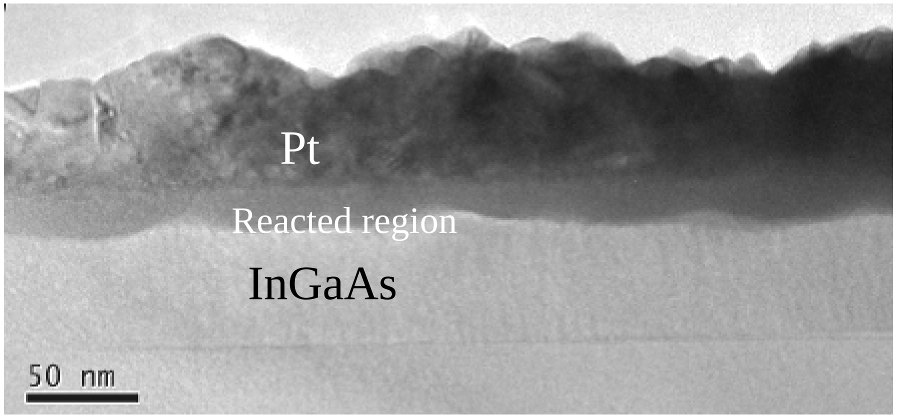
Our HBT Base Contacts Today Use Pd or Pt to Penetrate Oxides

TEM : Lysczek, Robinson, & Mohney, Penn State
Sample: Urteaga, RSC

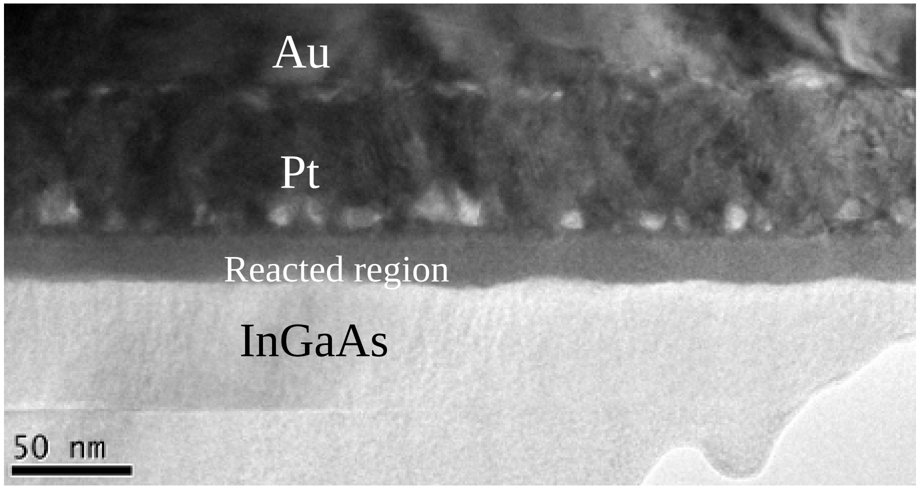
PENNSTATE

ROCKWELL SCIENTIFIC





Pt Contact after 4hr 260C Anneal



Pt/Au Contact after 4hr 260C Anneal

Wafer first cleaned in reducing

Pd & Pt react with III-V semiconductor

Penetrate surface oxide

Today provide 5 Ω-μm^2 resistivity (base)

→ investigate better cleaning, alternative reaction metals

Chor, E.F.; Zhang, D.; Gong, H.; Chong, W.K.; Ong, S.Y. **Electrical characterization, metallurgical investigation, and thermal stability studies of (Pd, Ti, Au)-based ohmic contacts.** Journal of Applied Physics, vol.87, (no.5), AIP, 1 March 2000. p.2437-44.

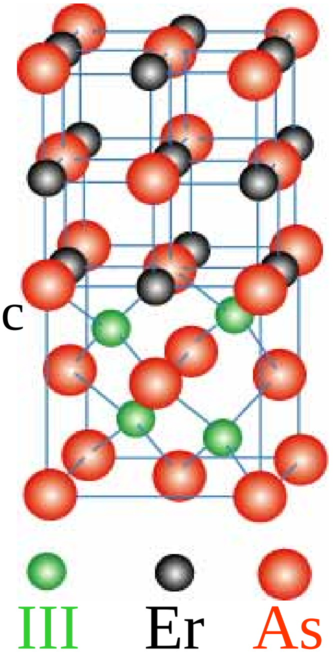
Reducing Emitter Resistance: ErAs Emitter Contacts

Material	Lattice constant	mismatch to ErAs	mismatch to ErSb
ErAs	5.7427Å		
ErSb	6.108Å		
GaAs	5.6532Å	-1.6%	-8.0%
InP	5.8687Å	2.1%	-4.0%
GaSb	6.0959Å	5.8%	-0.2%

Zimmerman, Gossard & Brown, UCSB

ErAs: Rocksalt structure

III-V: Zinc blend structure



Q. G. Sheng, J. Appl. Phys. (1993)
A Guivarc'h, J. Appl. Phys. (1994)

Epitaxial semimetal
- **similar crystal structure to III-V semiconductors**
- **can be grown by MBE**

*A. Guivarc'h, Electron. Lett.(1989)
**C.J.Palmstrøm Appl. Phys. Lett. (1990)

In-situ contacts → no oxides, no contaminants
Lattice matched → few defect states → no surface Fermi pinning
Thermodynamically stable → little intermixing
Well-controlled (atomic precision) interface

Temperature Rise Within Transistor & Substrate

For each doubling in digital clock rate

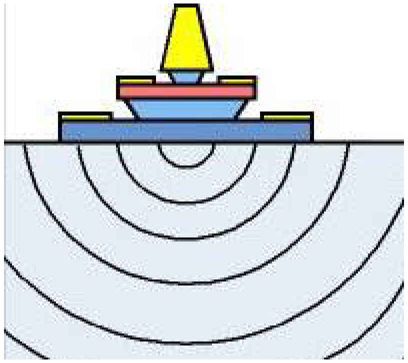
emitter width W_e decreases $4:1$

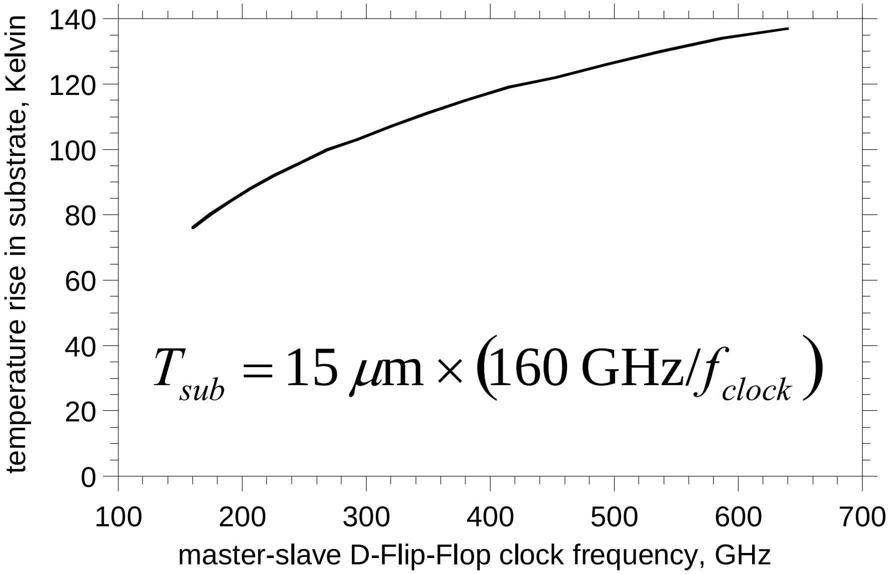
HBT spacing D decreases $2:1$

Thinning the substrate aggressively allows acceptable substrate temperature rise even at 300 GHz digital clock rate

HBT scaling → logarithic temperature increase

$$\Delta T_{InP,1} \cong \frac{P}{\pi K_{InP} L_E} \ln\left(\frac{L_e}{W_e}\right) + \ldots$$





$$T_{sub} = 15\ \mu\text{m} \times (160\ \text{GHz}/f_{clock})$$

Temperature Rise Within Package

Assumptions :

Transistor spacing : $20\ \mu\text{m} \cdot (150\ \text{GHz}/f_{clock})$

$V_{ce} = 2$ V bias

1000 transistors/IC

IC power $= 1.5 \times$ (transistor dissipation)

For each doubling in digital clock rate

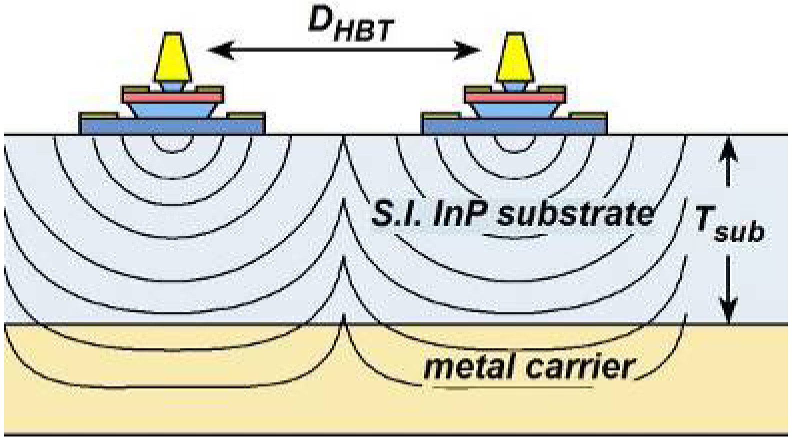
emitter width W_e decreases 4 : 1

HBT spacing D decreases 2 : 1

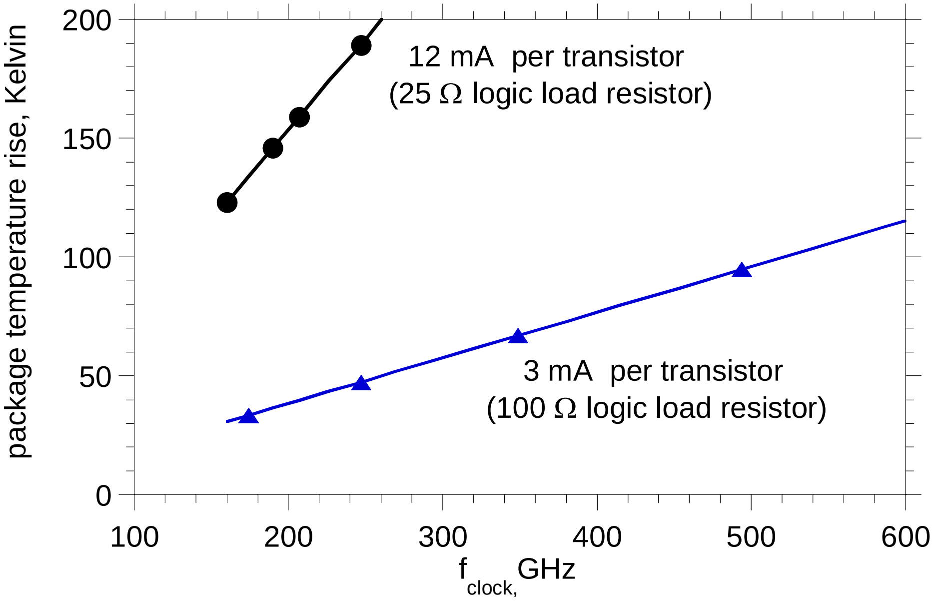
$\rightarrow$ chip dimensions W_{chip} decrease 2 : 1

Total Package Temperature Rise

$$\Delta T_{package} \cong \left(\frac{2+\pi}{2\pi}\right)\frac{P_{chip}}{K_{Cu}W_{chip}}$$

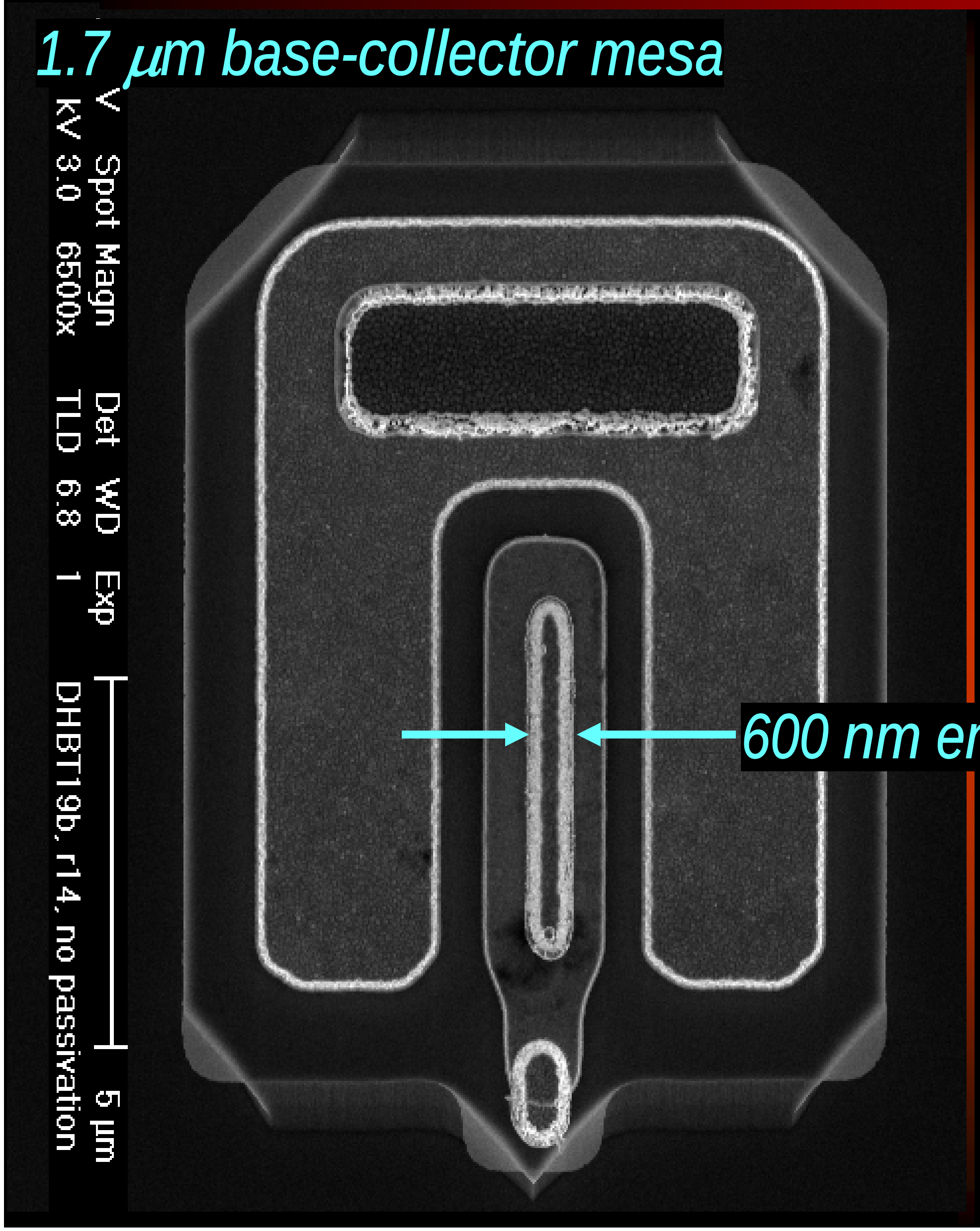


At 3 mA per transistor (100 Ω loading) acceptable package temperature rise with 1000 transistors / IC even at 300 GHz digital clock rate.

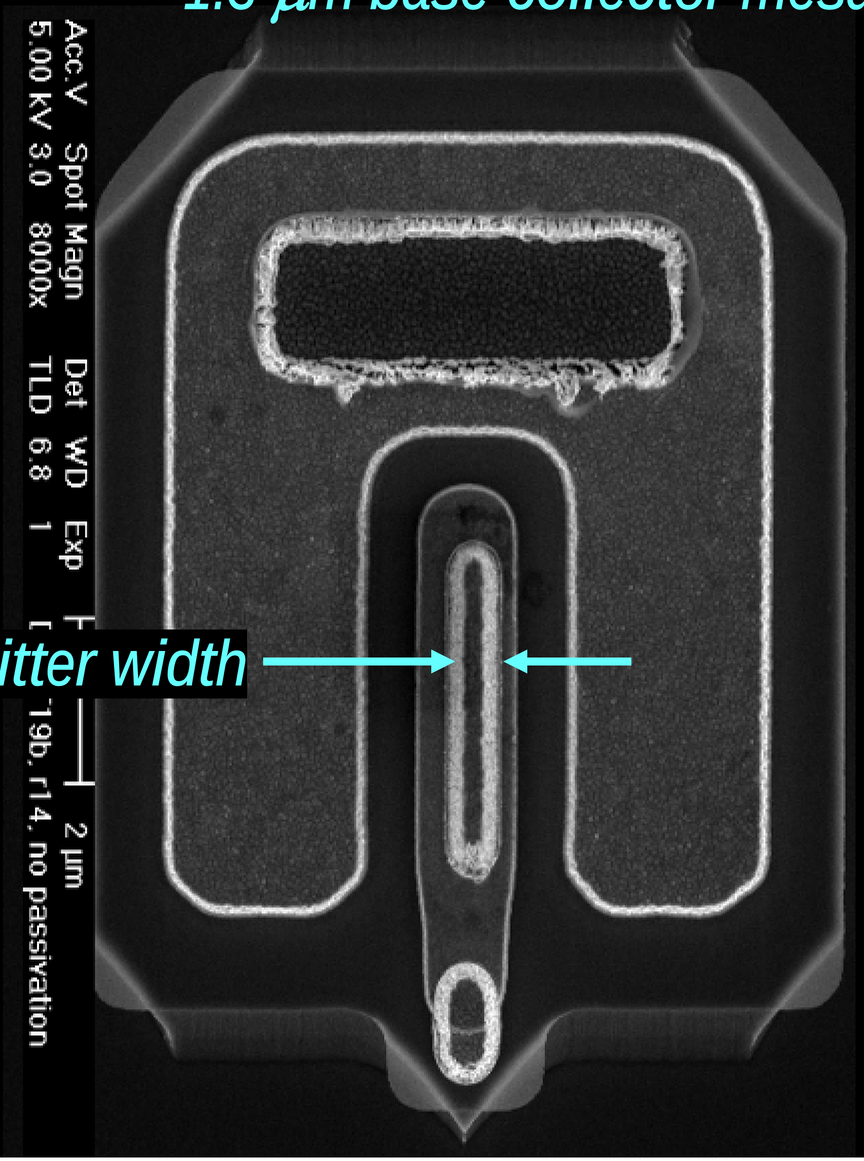


UCSB DHBTs: 500-600 nm Scaling Generation

1.7 μm base-collector mesa

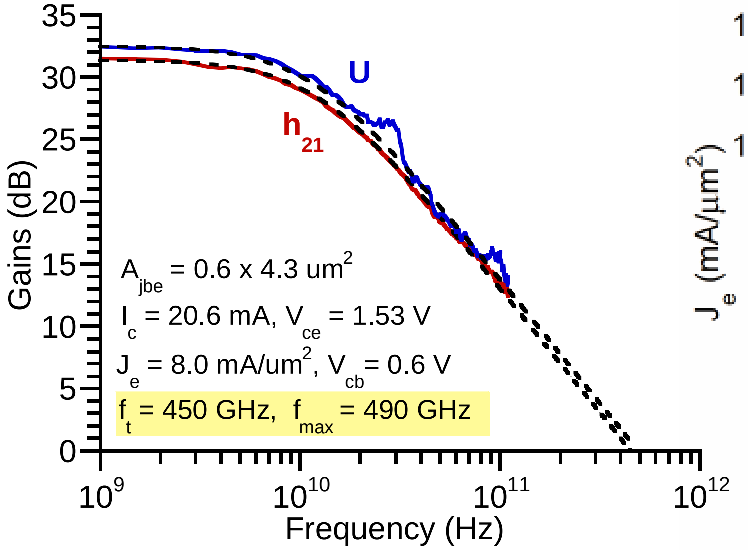


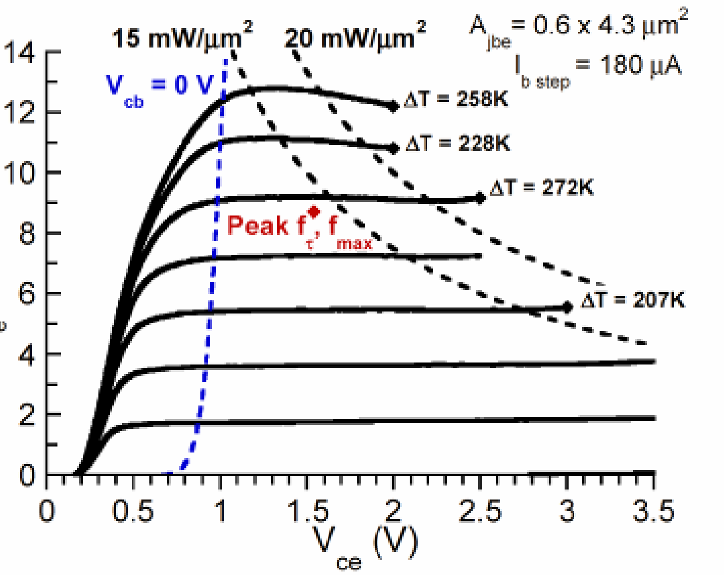
1.3 μm base-collector mesa

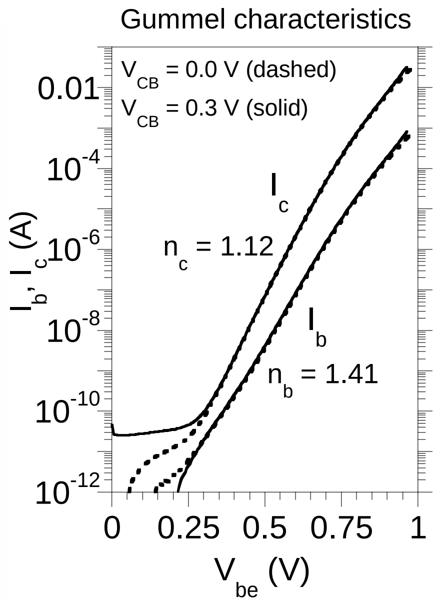


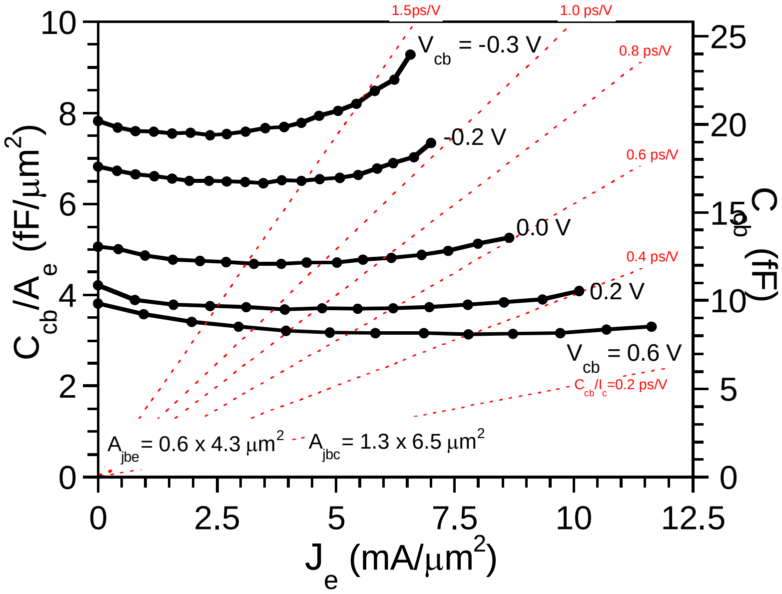
600 nm emitter width

InP DHBT: 600 nm lithography, 120 nm thick collector, 30 nm thick base






Gummel characteristics



$\beta \approx 40$, $V_{BR,CEO}$ = 3.9 V.

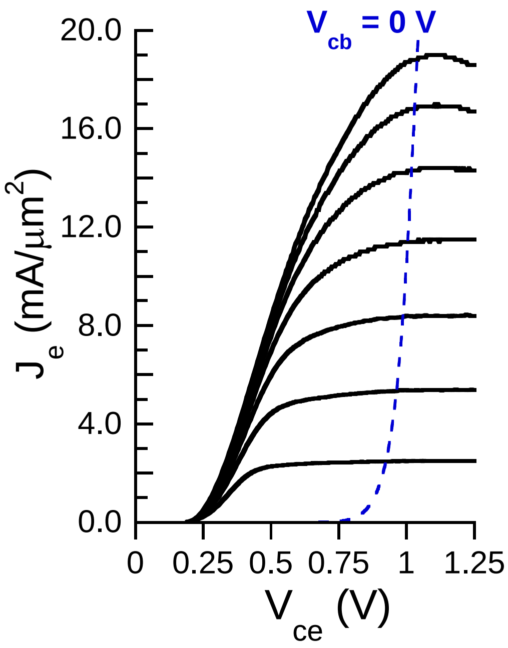
Emitter contact $R_{cont} < 10\ \Omega\cdot\mu m^2$

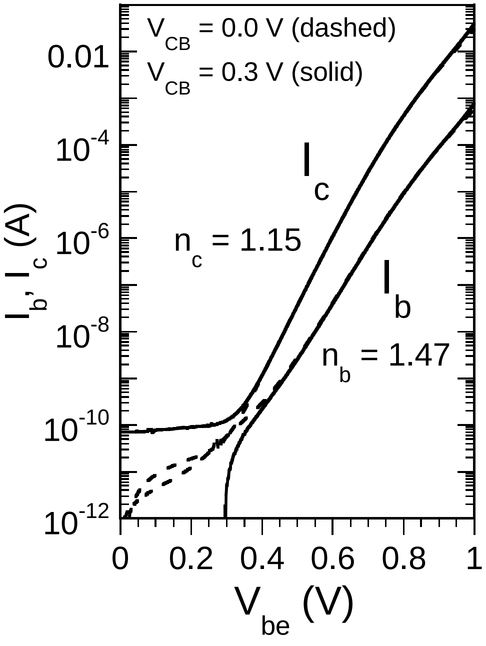
Base : R_{sheet} = 610 Ω/sq, $R_{cont} = 4.6\ \Omega\cdot\mu m^2$

Collector : R_{sheet} = 12.1 Ω/sq, $R_{cont} = 8.4\ \Omega\cdot\mu m^2$

InP DHBT: 600 nm lithography, 75 nm collector, 20 nm base

DC characteristics





$A_{je} = 0.65 \times 4.3\ \mu m^2$, $I_{b,step}$ = 175 μA

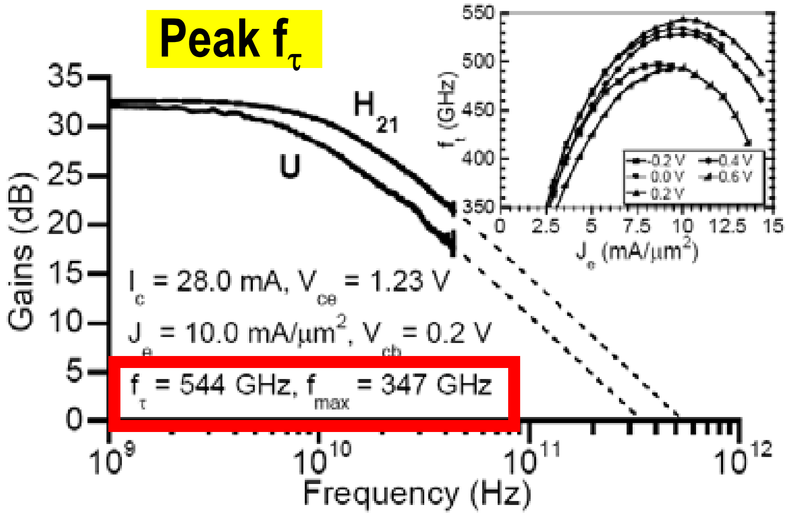
Average $\beta \approx 50$, BV_{CEO} = 3.2 V, BV_{CBO} = 3.4 V (I_C = 50 μA)

Emitter contact (from RF extraction), $R_{cont} \approx 8.6\ \Omega\cdot\mu m^2$

Base (from TLM) : R_{sheet} = 805 Ω/sq, R_{cont} = 16 $\Omega\cdot\mu m^2$

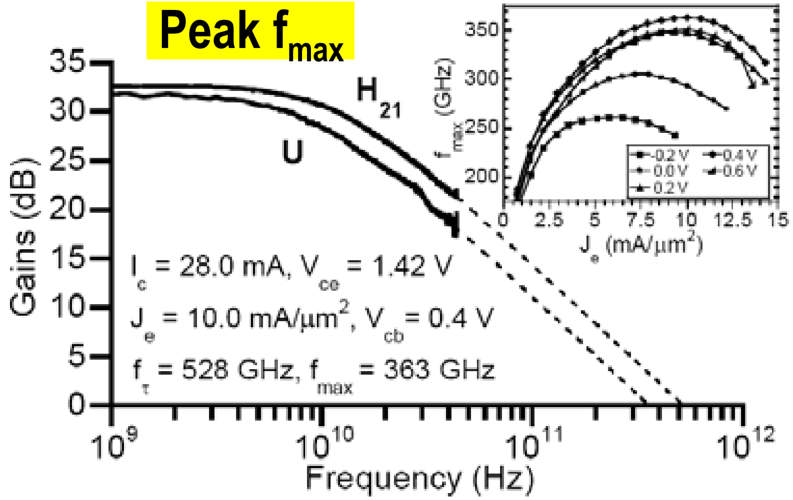
Collector (from TLM) : R_{sheet} = 12.0 Ω/sq, R_{cont} = 4.7 $\Omega\cdot\mu m^2$

Peak f_τ



I_c = 28.0 mA, V_{ce} = 1.23 V
J_e = 10.0 mA/μm^2, V_{cb} = 0.2 V
f_τ = 544 GHz, f_{max} = 347 GHz

Peak f_{max}

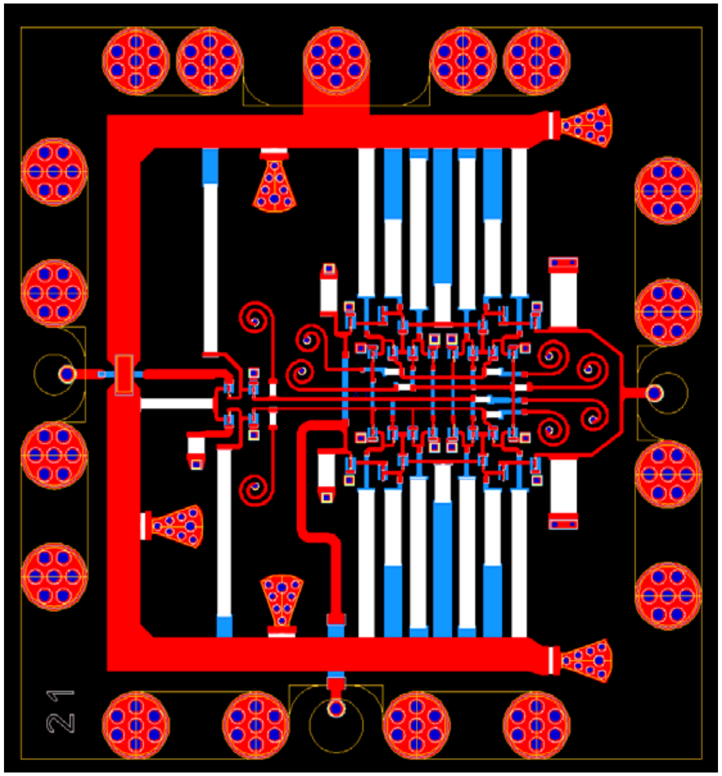


I_c = 28.0 mA, V_{ce} = 1.42 V
J_e = 10.0 mA/μm^2, V_{cb} = 0.4 V
f_τ = 528 GHz, f_{max} = 363 GHz

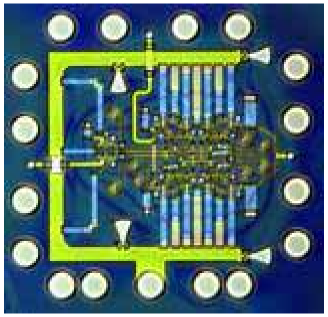
RF characteristics

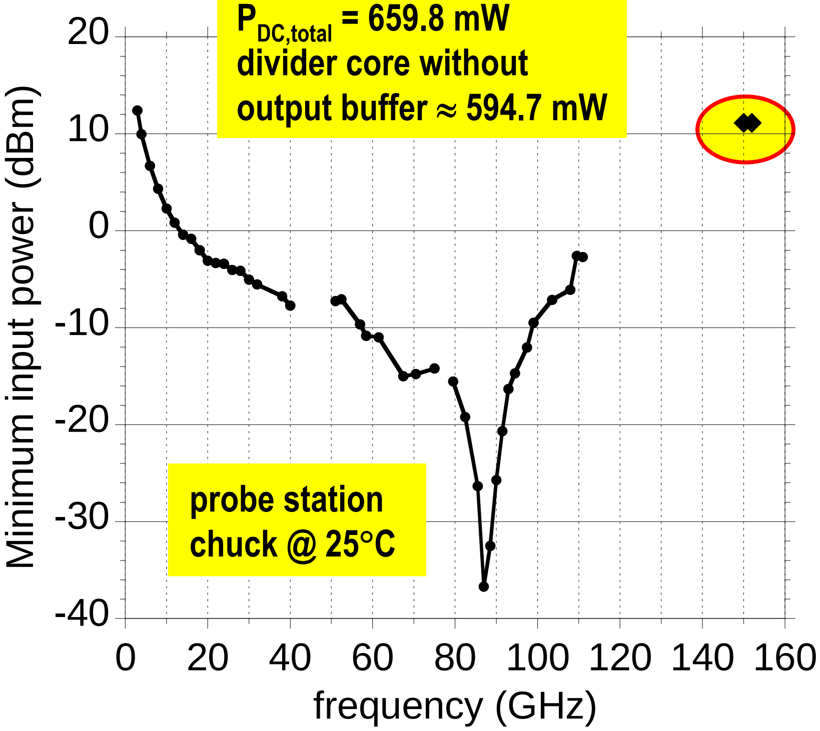
UCSB / RSC / GCS 150 GHz Static Frequency Dividers

IC design: Z. Griffith, UCSB
HBT design: RSC / UCSB / GCS
IC Process / Fabrication: GCS
Test: UCSB / RSC / Mayo



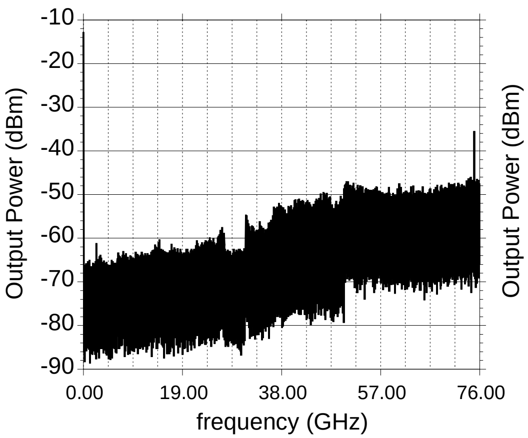
	units	data current steering	data emitter followers	clock current steering	clock emitter followers
size	μm^2	0.5 x 3.5	0.5 x 4.5	0.5 x 4.5	0.5 x 5.5
current density	$mA/\mu m^2$	6.9	4.4	4.4	4.4
C_{cb}/I_c	psec / V	0.59	0.99	0.74	0.86
V_{cb}	V	0.6	0	0.6	1.7
f_τ	GHz	301	260	301	280
f_{max}	GHz	358	268	358	280

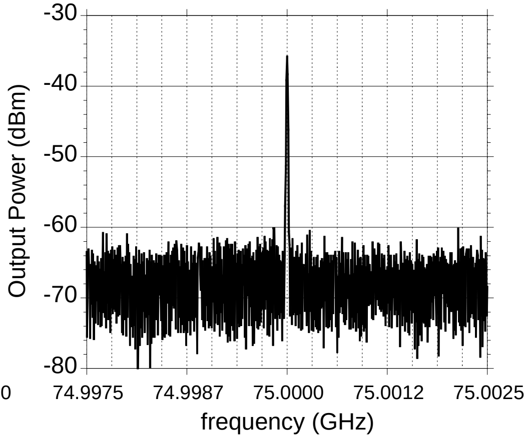




$P_{DC,total}$ = 659.8 mW
divider core without
output buffer ≈ 594.7 mW

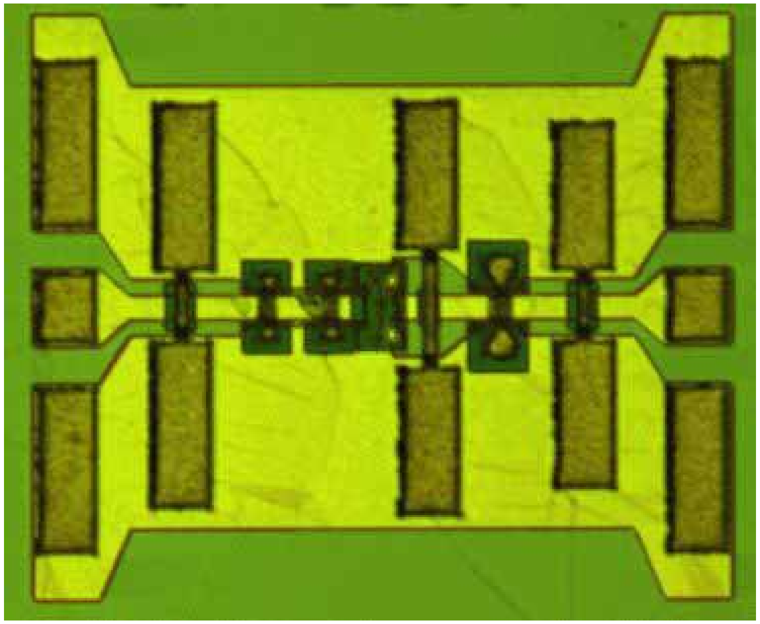
probe station chuck @ 25°C

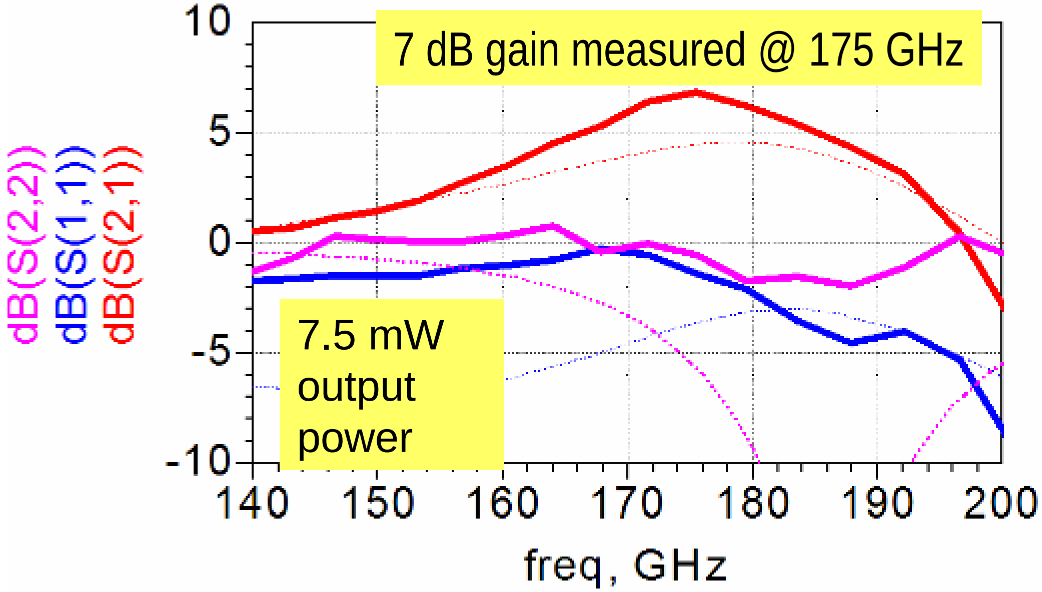




175 GHz Amplifiers with 300 GHz f_{max} Mesa DHBTs

V. Paidi, Z. Griffith, M. Dahlström

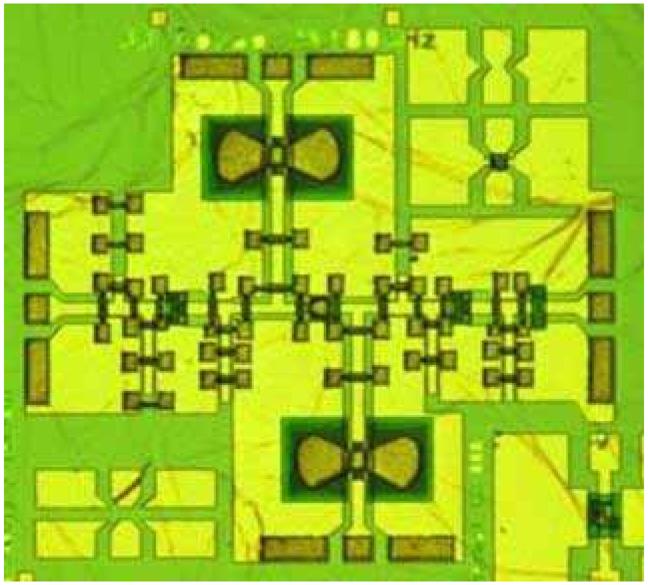




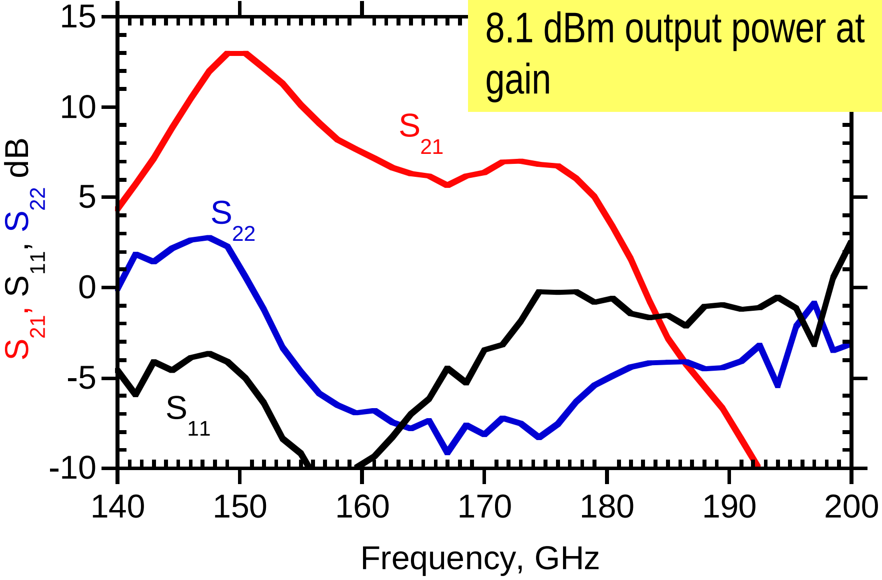
7 dB gain measured @ 175 GHz

7.5 mW output power

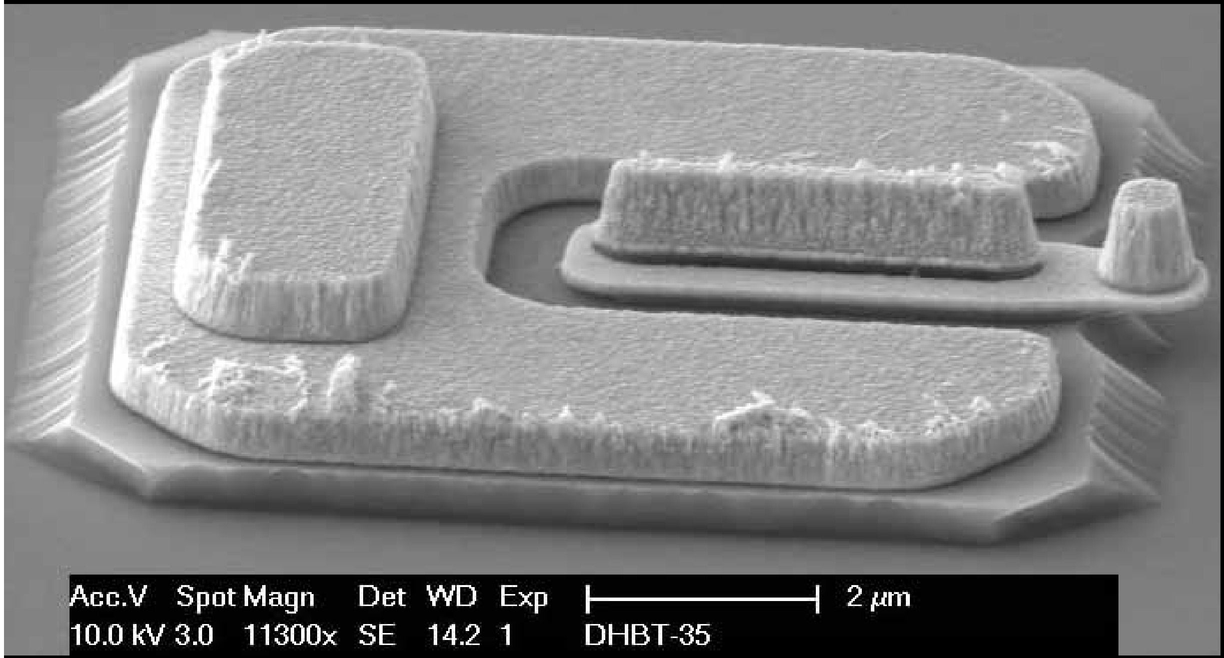
2 fingers x 0.8 um x 12 um, ~250 GHz f_τ, 300 GHz f_{max} , V_{br} ~ 7V, ~ 3 mA/um^2 current density

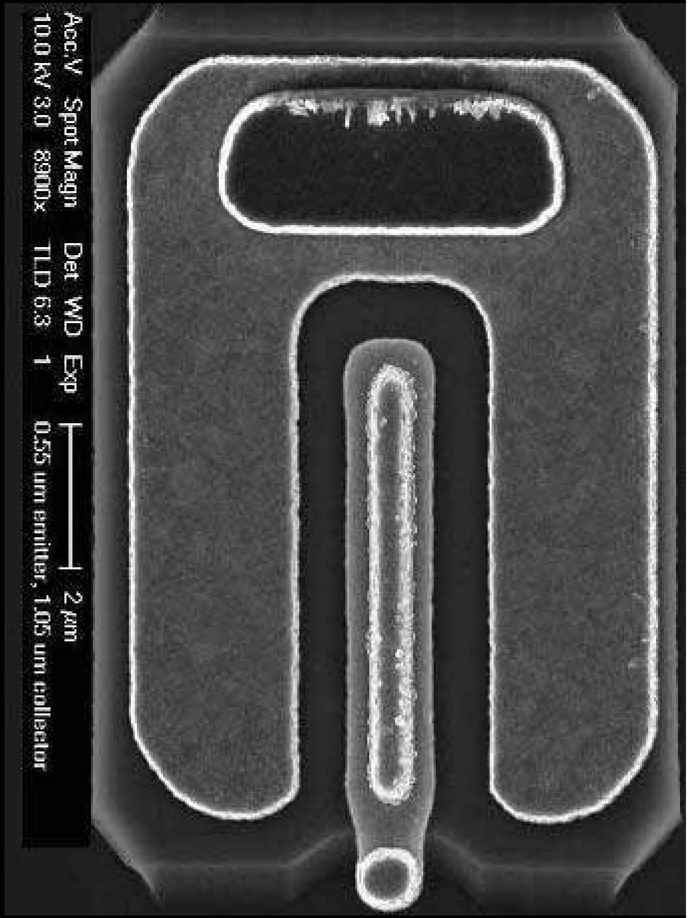


7-dB small-signal gain at 176 GHz
8.1 dBm output power at 6.3 dB gain



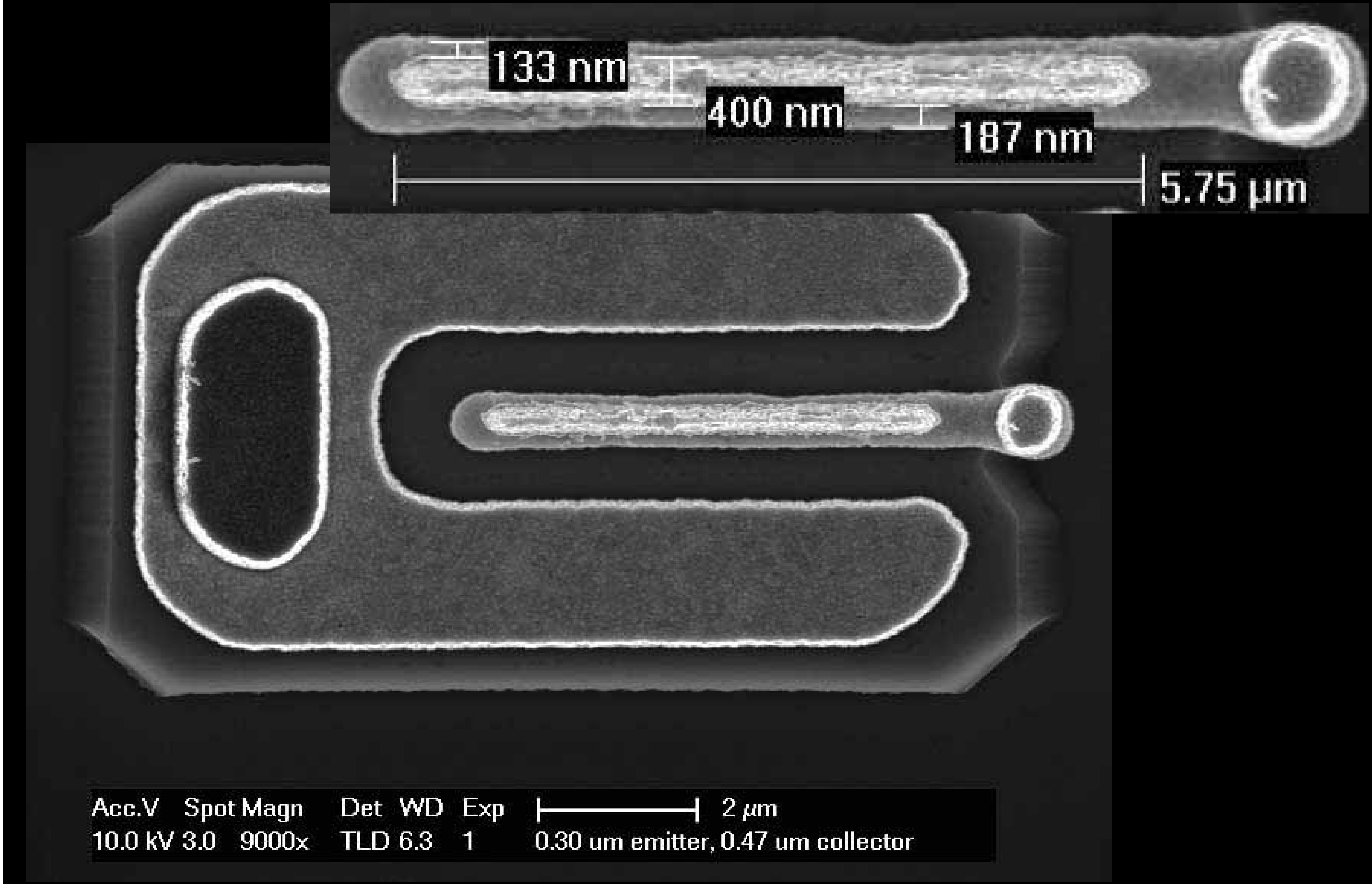
250 nm scaling generation DHBTs





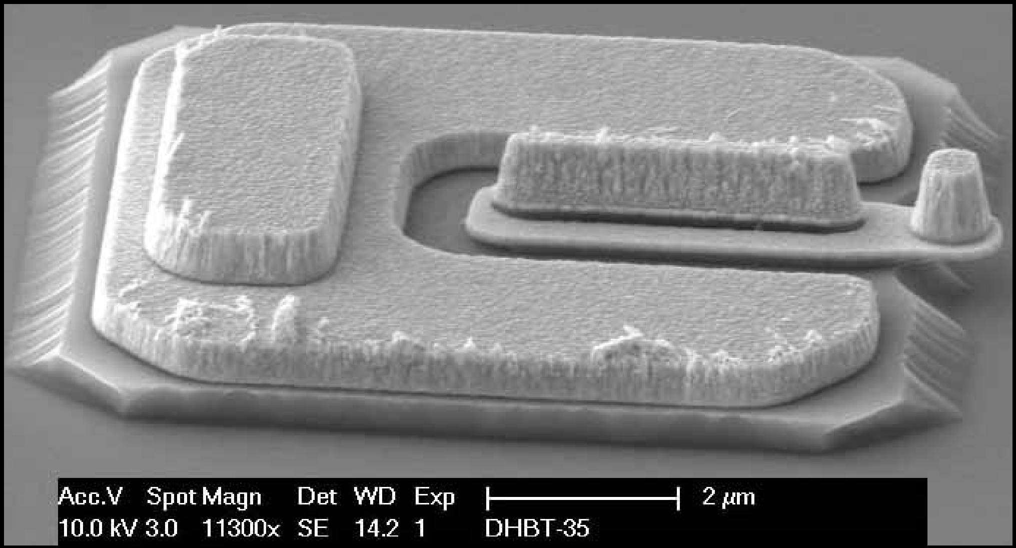
- 100 % I-line lithography
- Emitter contact resistance reduced 40%: from 8.5 to 5 $\Omega\cdot\mu m^2$
- Base contact resistance is < 5 $\Omega\cdot\mu m^2$ --hard to measure
- Recall, 1/8 μm scaling generation needs $\leq 5\ \Omega\cdot\mu m^2$ emitter ρ_c

0.30 µm emitter junction, $W_c/W_e \sim 1.6$



First mm-wave results with 250 nm InP DHBTs

150 nm material
250 nm emitter width



f_τ = 420 GHz
f_{max} = 650 GHz
~6 V breakdown
30 mW/um^2 power handling

results submitted postdeadline to 2006 DRC, E. Lind et al

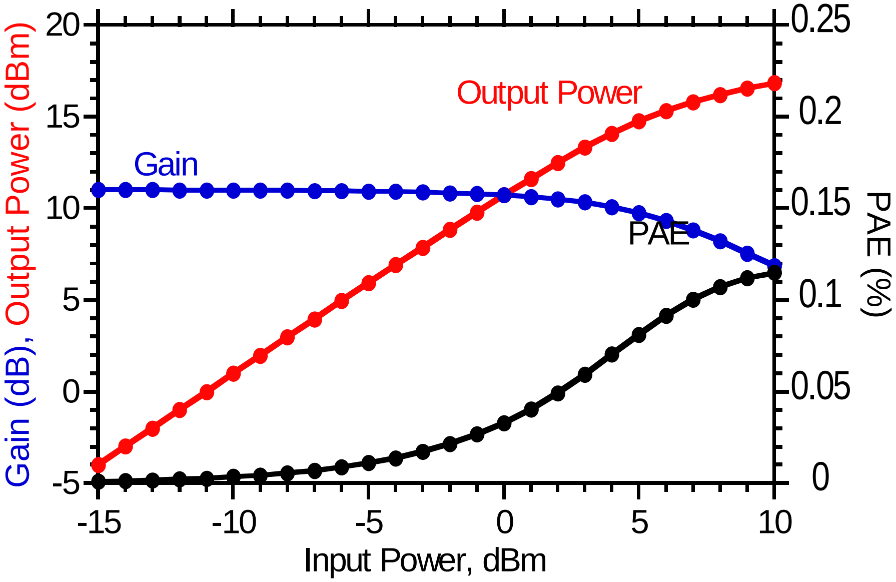
330 GHz Cascode Power Amplifiers In Design

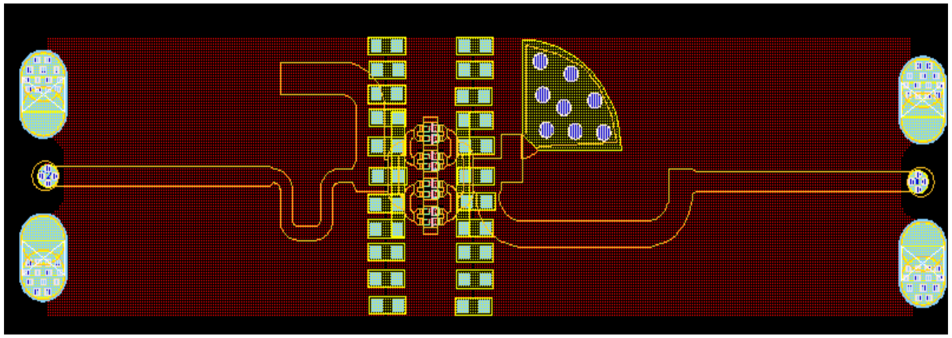
Thin-film microstrip lines

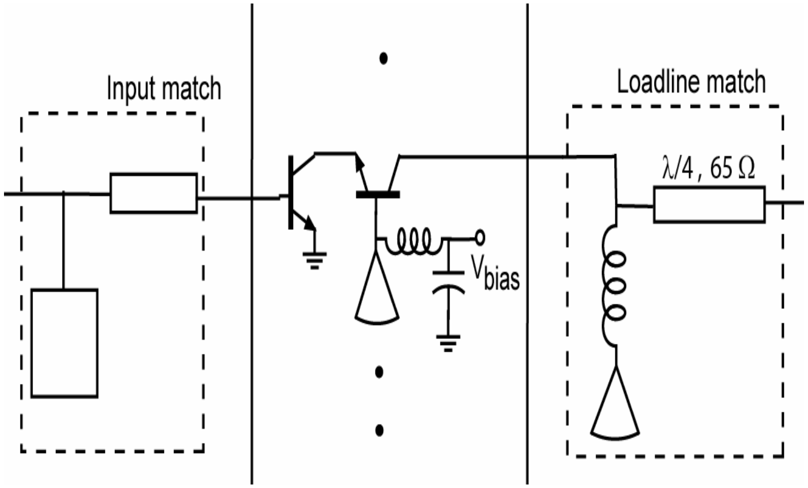
Output P_{sat} = 50 mW (17 dBm)

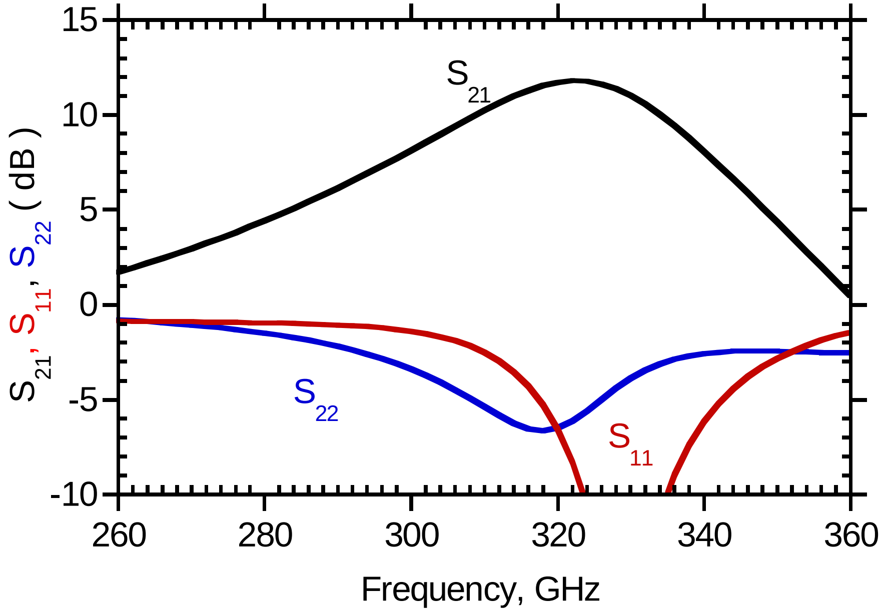
10-dB associated power gain

use the 650 GHz f_{max} transistors









Frequency Limits of Bipolar Integrated Ciruits

Done:

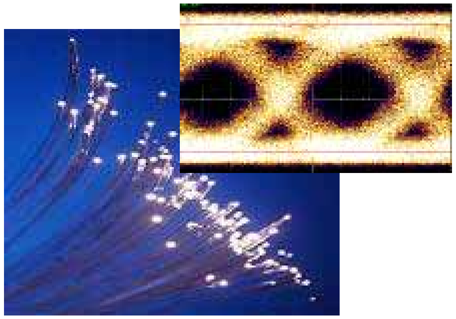
~475 GHz f_t & f_{max}
150 GHz static dividers
160 Gb/s MUX & DMUX (Chalmers/Vitesse)

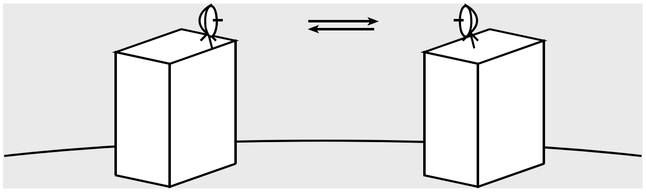
250 nm results coming very soon.

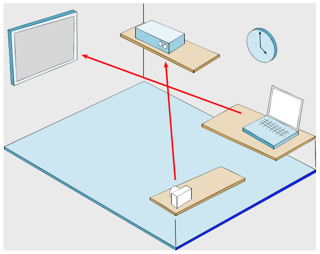
expect ~200 GHz digital clock rate, 340 GHz amplifiers

THz transistors will come

The approach is scaling.
The limits are contact and thermal resistance.







Performance Parameters for Fast Logic & Mixed-Signal

Gate Delay Determined by :

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C}\right)\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Depletion capacitance charging through the base resistance

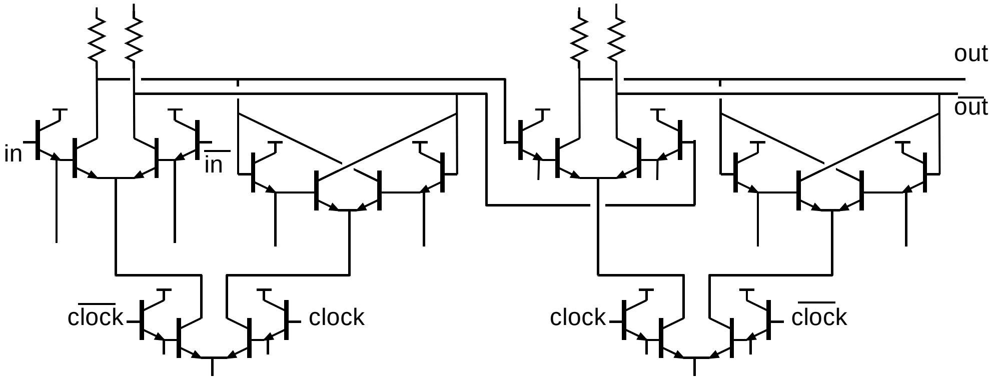
$$R_{\text{bb}}\left(C_{cbi}+C_{be,\text{depletion}}\right)$$

Supplying base + collector stored charge through the base resistance

$$R_{\text{bb}}\left(\tau_b+\tau_c\right)\left(\frac{I_C}{\Delta V_{LOGIC}}\right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 4\cdot\left(\frac{kT}{q}+R_{ex}I_c\right)$$



$(\tau_b+\tau_c)$ typically 10 - 25% of total delay;
Delay not well correlated with f_τ

$(\Delta V_{LOGIC}/I_C)(C_{cb}+C_{be,\text{depl}})$ is 55% - 80% of total.

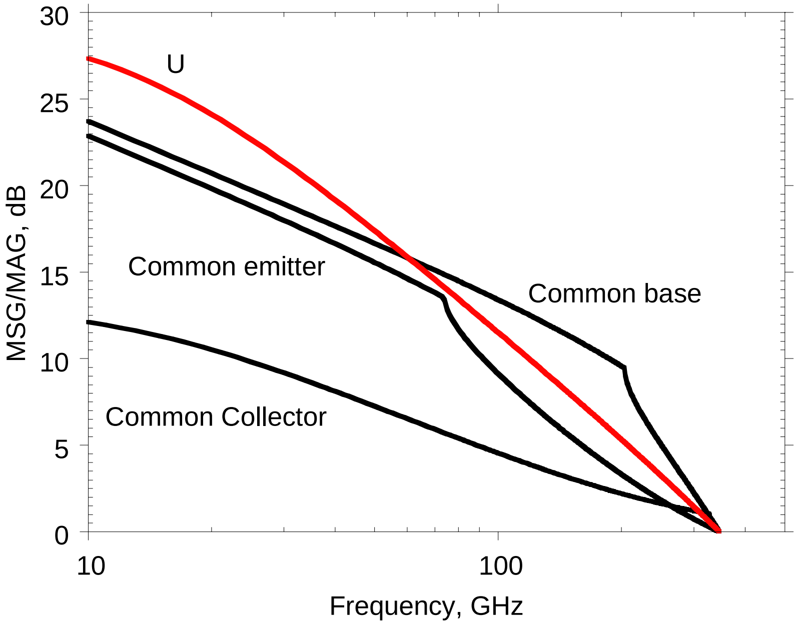
High (I_C/C_{cb}) is a key HBT design objective.

R_{ex} must be very low for low ΔV_{logic} at high J

Design HBTs for fast logic, not for high f_t & f_{max}

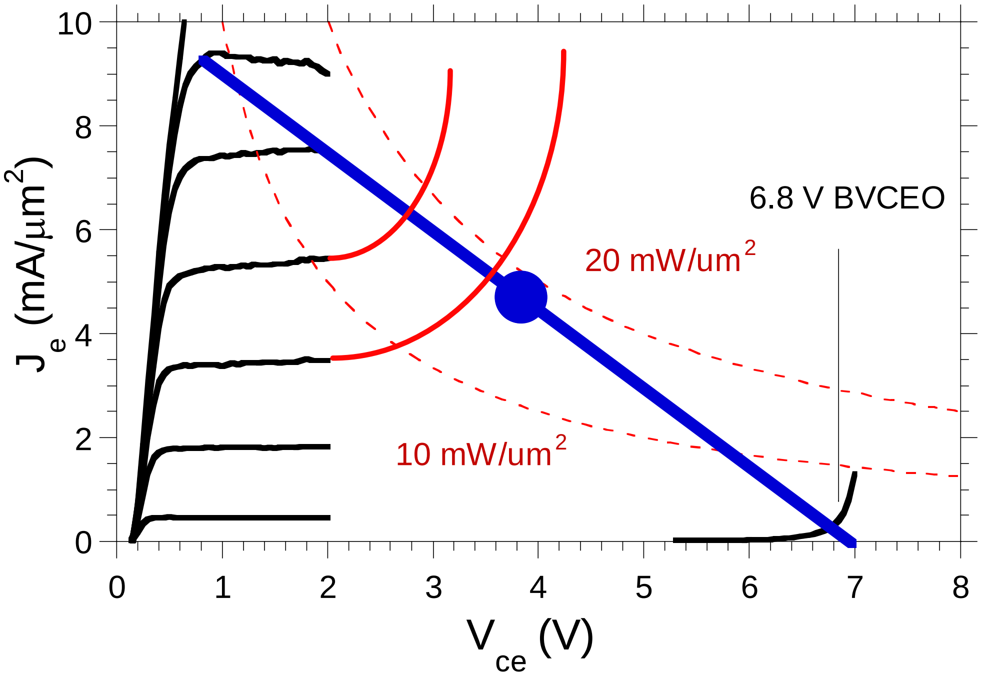
Performance Parameters for mm-wave Power

Gain.....under large-signal conditions



...gain is less than MAG/MSG...

Breakdown AND power density



$$P_{\max} = (1/8)(V_{\max} - V_{\min})I_{\max}$$