InP HBTs: Process Technologies and Integrated Circuits

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Acknowledgments

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Sponsors

US DARPA*: John Zolper, Steve Pappert*
US ONR*: Dan Purdy, Ingham Mack, Max Yoder*
US ARO*,*
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Thanks To Prof. Bill Frensley, UT Dallas, for the use of BandProf

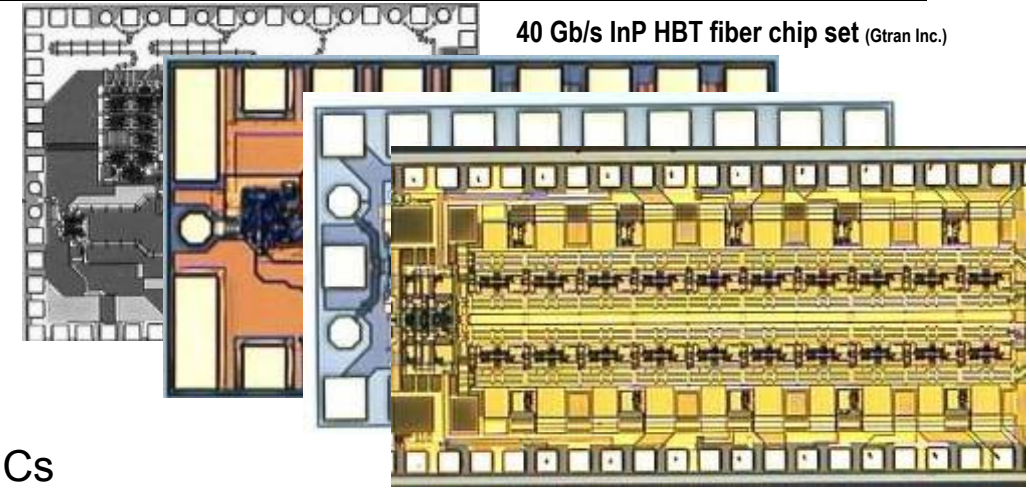
Applications

High Frequency Electronics: Applications

Optical Fiber Transmission

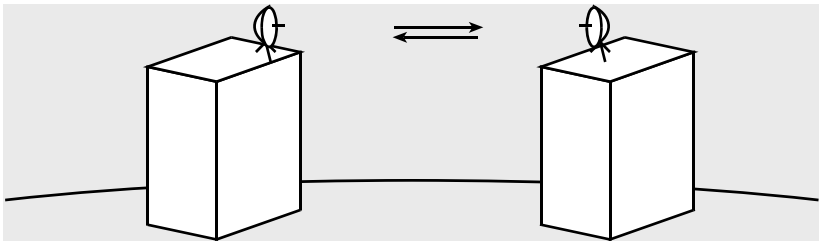
40 Gb/s: InP and SiGe ICs commercially available

80 & 160 Gb/s is feasible
80-160 Gb/s InP ICs now clearly feasible
~100 GHz modulators demonstrated (KTH Stockholm)
100 + GHz photodiodes demonstrated in 1980's
challenge: limit to range due to fiber dispersion
challenge: competition with WDM using 10 Gb CMOS ICs



40 Gb/s InP HBT fiber chip set (Gtran Inc.)

250 GHz digital radio: 100 Gb/s over 1 km in heavy rain

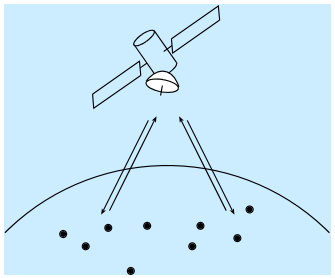


Radio-wave Transmission / Radar / Imaging

65-80 GHz, 120-160 GHz, 220-300 GHz
100 Gb/s transmission over 1 km in heavy rain
300 GHz imaging for foul-weather aviation

science
spectroscopy, radio astronomy

mm-wave sensor networks

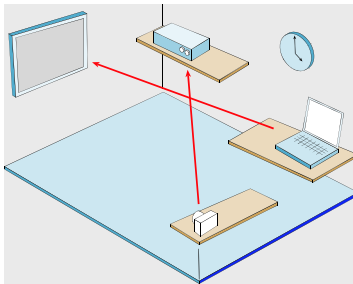


300 GHz imaging

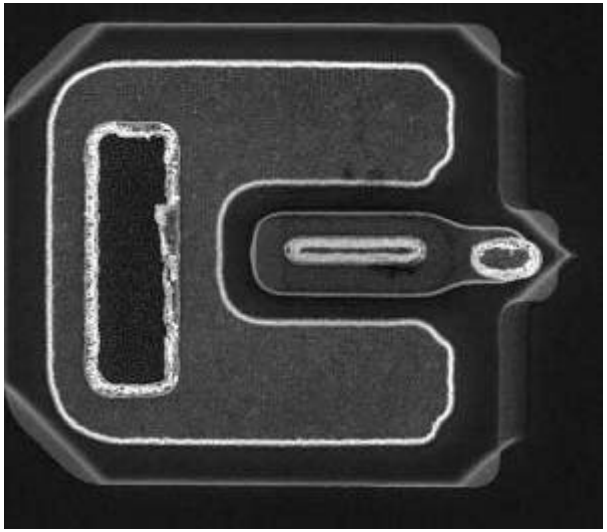
Mixed-Signal ICs for Military Radar/Comms

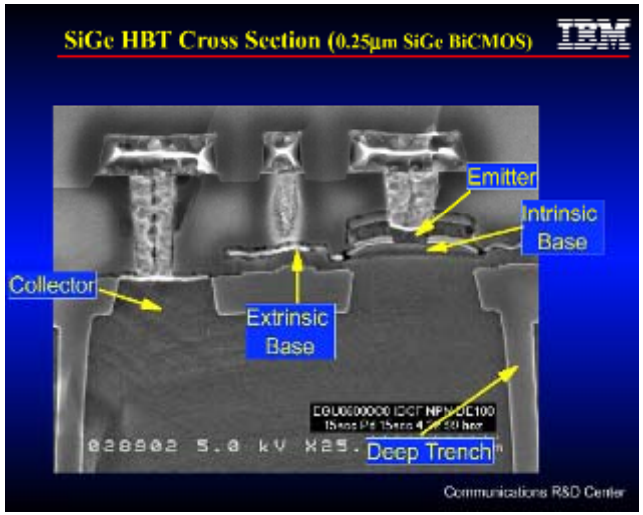
direct digital frequency synthesis, ADCs, DACs
high resolution at very high bandwidths sought

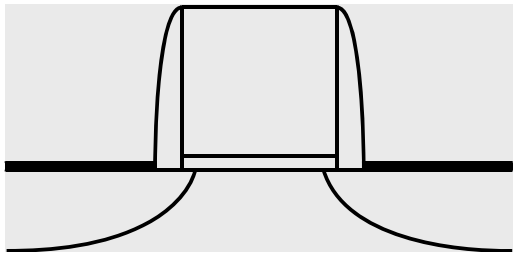
Gb/s Wireless Home Networks



Fast IC Technologies







InP HBT: 500 nm emitter
455 GHz f_τ / 485 GHz f_{max}
~4 V breakdown
150 GHz static dividers
178 GHz amplifiers

SiGe HBT: 130 nm emitter
300 GHz f_τ / 350 GHz f_{max}
96 GHz static dividers
77 GHz amplifiers
150 GHz push-push VCO- 75 GHz fundamental

CMOS: 90 nm node:
~200 GHz f_τ / 250 GHz f_{max}
~1-1.5 V breakdown
60 GHz 2:1 mux
91 GHz amplifiers

InP HBTs as ultra high speed technology:

~500 GHz bandwidth even at 500 nm scaling with minimal parasitic reduction

Potential for much wider bandwidths at ~100 nm scaling

InP HBTs for radio astronomy

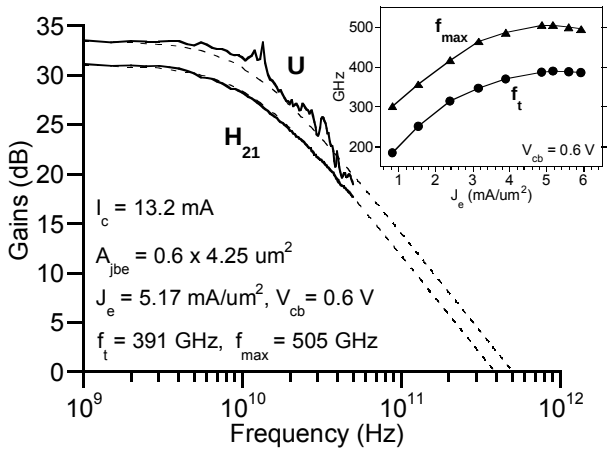
feasibility of 100 mW power amplifiers at 200 GHz & perhaps 300 GHz

→ aid in developing THz diode frequency multiplier chains

InP DHBTs for 33 / 45 / 60 / 77 / . . . / 94 GHz power ?

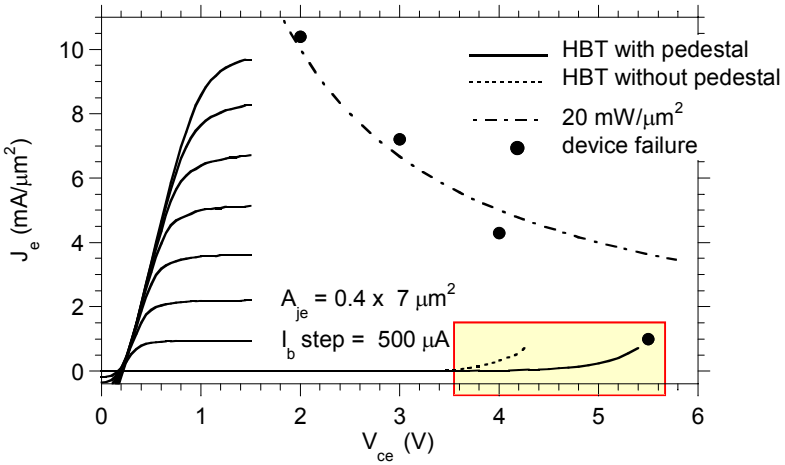
InP HBTs have the necessary bandwidth

W-band amps need 200 GHz f_t & fmax
Today's InP HBTs: 400-500 GHz f_t & fmax



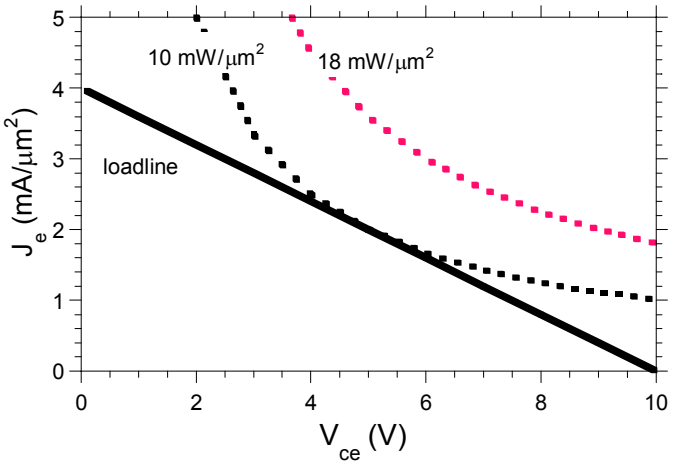
InP HBTs can handle the necessary voltage

10 V breakdown → adequate power
370 GHz HBTs have 5.6 V breakdown
200 GHz (W-band) HBTs will have 10 V



InP HBTs can handle the necessary power density

10 mW/um² DC dissipation is reliable
→ 5 mW/um² RF output power
→ 2.5 mW/um in 0.5 um technology



2 THz-Volt breakdown-bandwidth product
*$E_{max}V_{sat}$=2*10¹³ Volt/second*

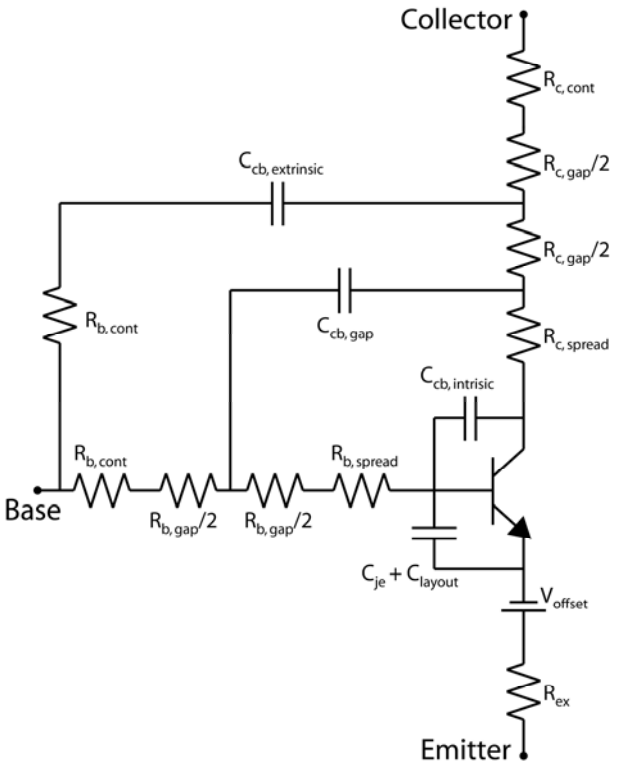
→ Power amplifiers to ~80 GHz in 1 um processes
1 um GaAs HBT processes are cheap, why not so InP ?

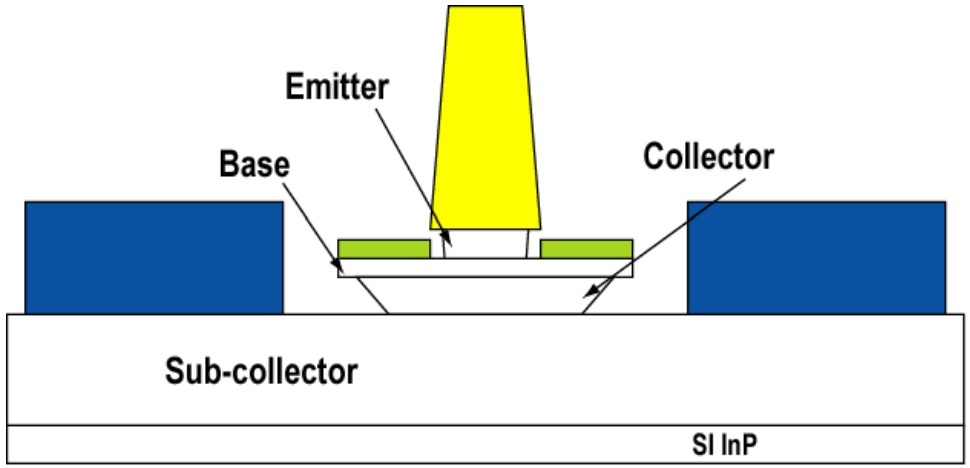
→ Power amplifiers to ~350 GHz in 250 nm processes
mm-wave & sub-mm-wave systems for radio astronomy

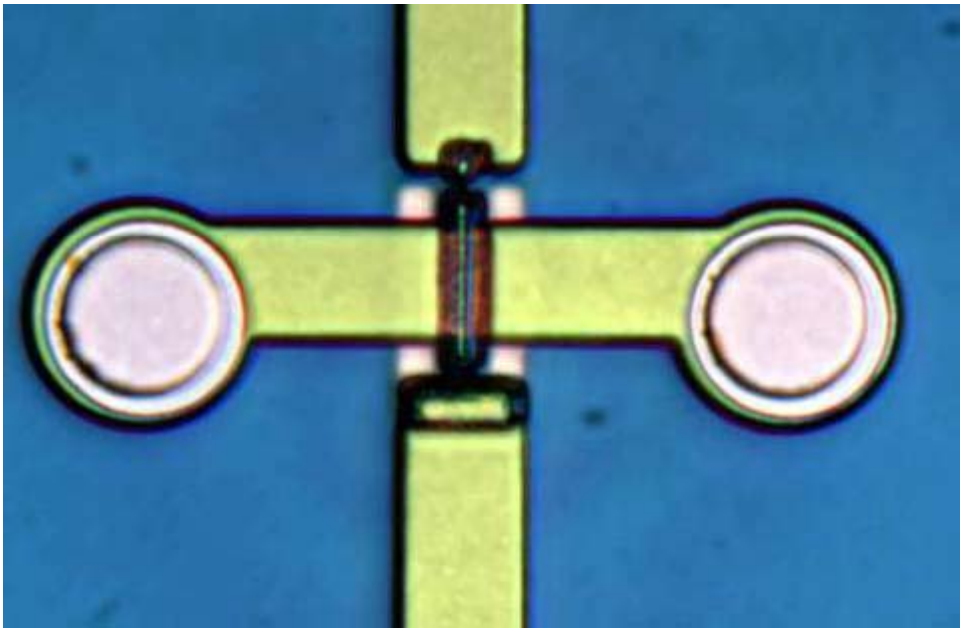
HBT technology

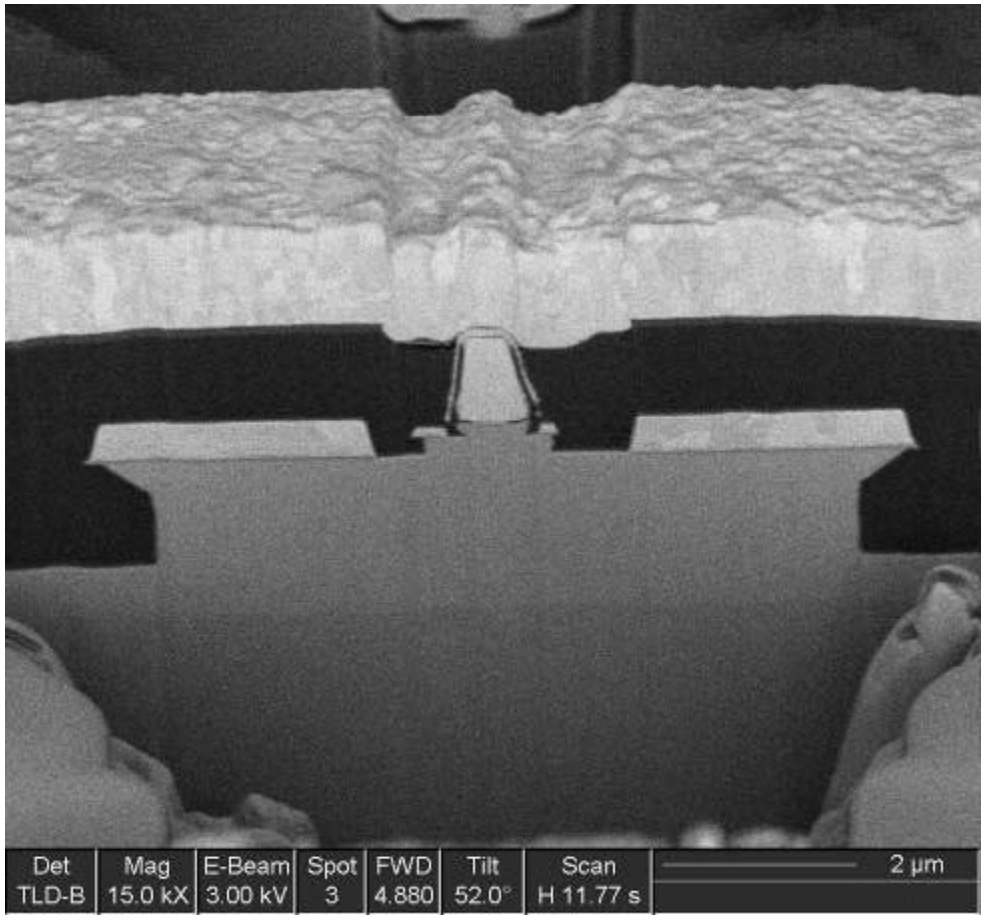
Z. Griffith

Indium Phosphide Heterojunction Bipolar Transistors









epitaxial layer designs

DHBT epitaxy: Graded InAlAs Emitter, InGaAs base, InAlGaAs Grades

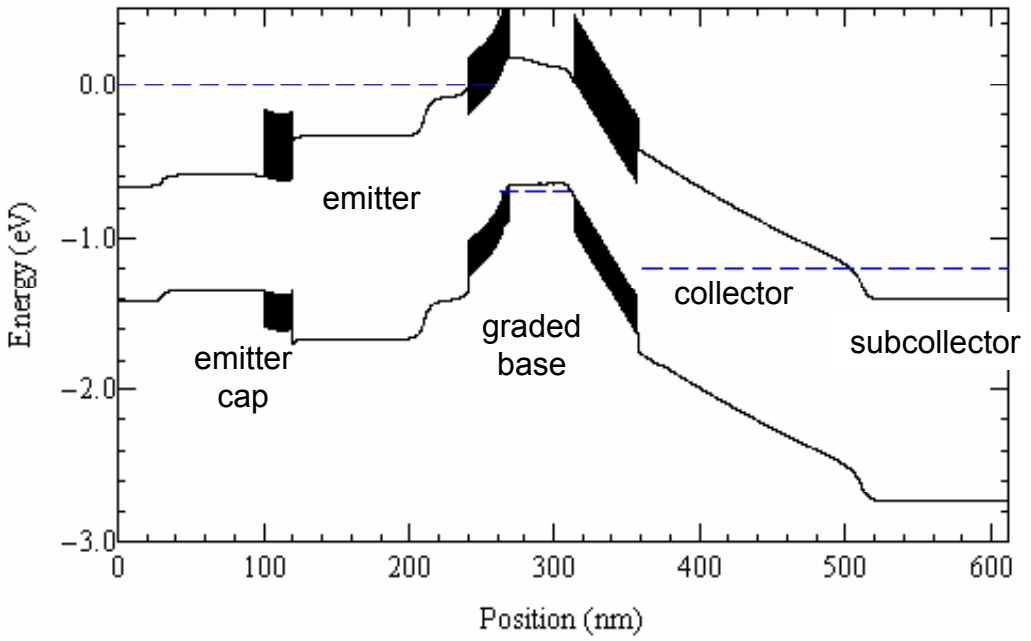
InAlAs emitter
InAlAs/InGaAs CSL grade
bandgap-graded InGaAs base
InAlAs/InGaAs CSL grade
InP collector

high breakdown
important for microwave power
important for logic

low thermal resistance
necessary for high power density
essential for microwave power
essential for logic

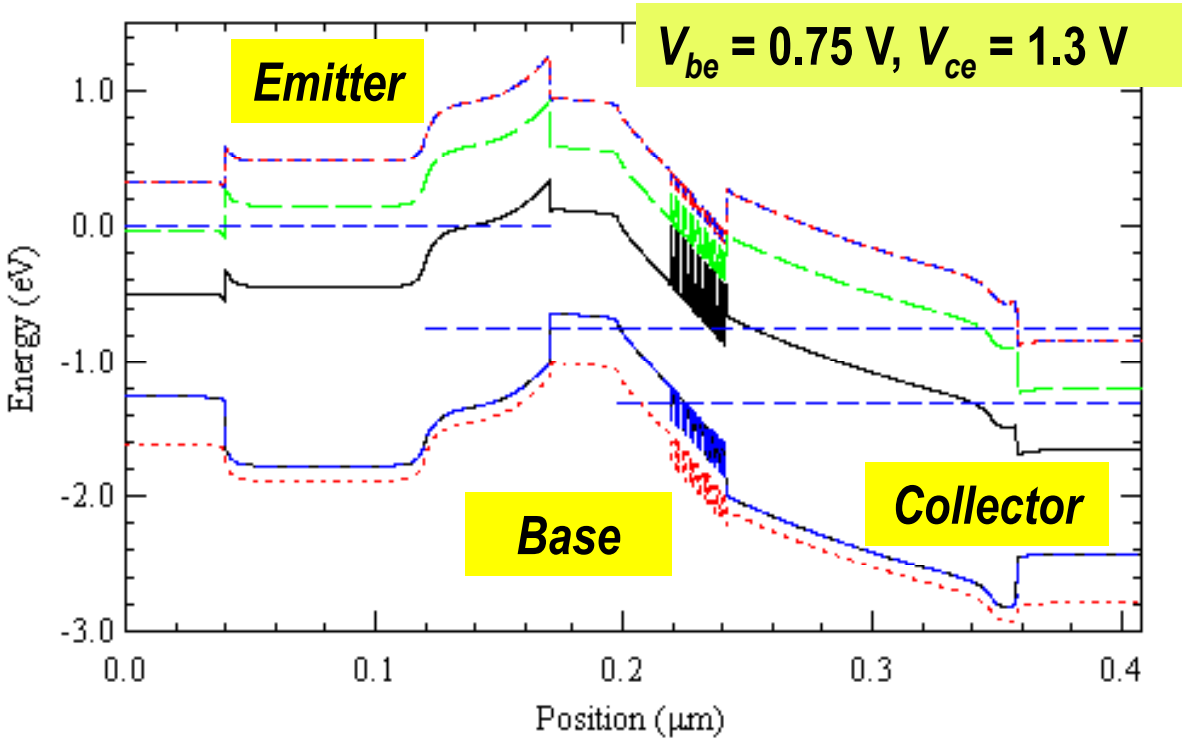
Performance
ft and fmax good or better than SHBTs

Layer	Material	Doping	Thickness (Å)
Emitter cap	$In_{0.53}Ga_{0.47}As$	2×10^{19} cm^{-3}: Si	300
N^+ emitter	InP	2×10^{19} cm^{-3}: Si	700
N^- emitter	InP	8×10^{17} cm^{-3}: Si	500
Emitter-base grade	$In_{0.53}Ga_{0.26}Al_{0.21}As$ to $In_{0.455}Ga_{0.545}As$	P: 4×10^{17} cm^{-3}: Si N: 8×10^{17} cm^{-3}: C	233 47
Base	$In_{0.53}Ga_{0.47}As$	N: 4×10^{19} cm^{-3}: C	400
Base-collector grade	$In_{0.53}Ga_{0.47}As$ to $In_{0.53}Ga_{0.26}Al_{0.21}As$	N: 2×10^{16} cm^{-3}: Si	240
Pulse doping	InP	5.6×10^{18} cm^{-3}: Si	30
Collector	InP	N: 2×10^{16} cm^{-3}: Si	1,630
Subcollector	InP	N: 1×10^{19} cm^{-3}: Si	~1000 Å



DHBT epitaxy: Abrupt InP Emitter, InGaAs base, InAlGaAs C/B Grade

InGaAs 3E19 Si 400 Å
InP 3E19 Si 800 Å
InP 8E17 Si 100 Å
InP 3E17 Si 300 Å
InGaAs 8E19 → 5E19 C 300 Å
Setback 3E16 Si 200 Å
Grade 3E16 Si 240 Å
InP 3E18 Si 30 Å
InP 3E16 Si **1030** Å
InP 1.5E19 Si 500 Å
InGaAs 2E19 Si **125** Å
InP 3E19 Si **3000** Å
SI-InP substrate



Key Features:

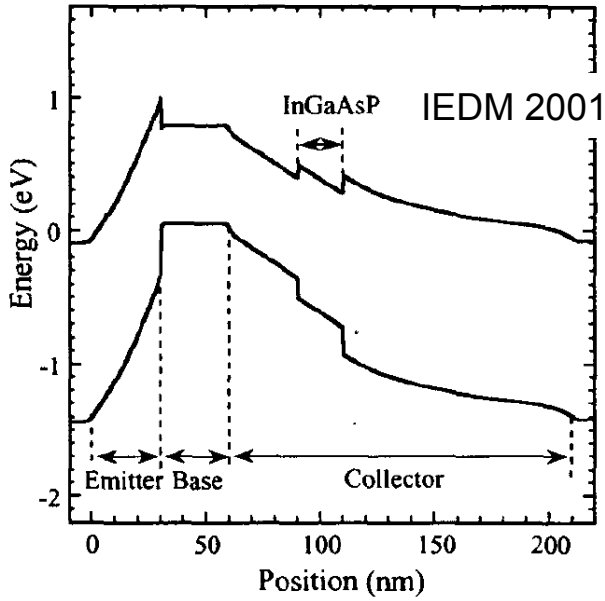
- Abrupt InP emitter—***benefit unclear***
- Collector setback—***eases grade design***
- Thin InGaAs in subcollector—***remove heat***
- Thick InP subcollector—***decrease $R_{c,sheet}$***

Other InP DHBT Layer Structures

InGaAs/InGaAsP/InP grade

InP/InGaAs DHBTs with 341-GHz f_T at high current density of over 800 kA/cm^2

Minoru Ida, Kenji Kurishima, Noriyuki Watanabe, and Takatomo Enoki



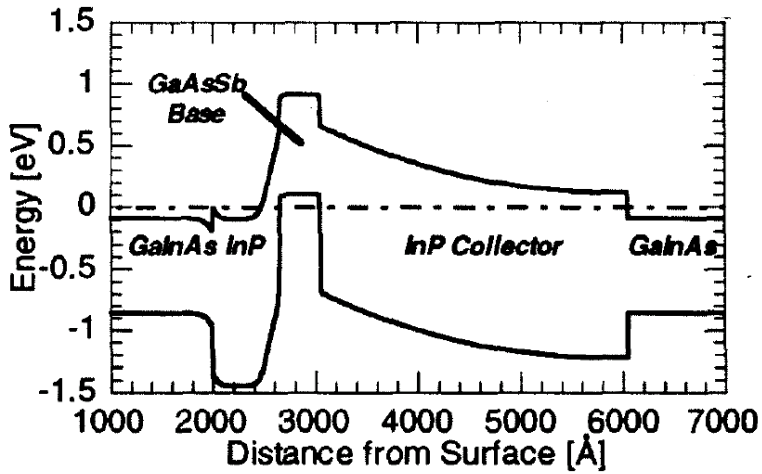
-suitable for MOCVD growth
- excellent results

InP/GaAsSb/InP DHBT

11th International Conference on Indium Phosphide and Related Materials
16-20 May 1999 Davos, Switzerland

InP/GaAsSb/InP DOUBLE HETEROJUNCTION BIPOLAR TRANSISTORS WITH HIGH CUT-OFF FREQUENCIES AND BREAKDOWN VOLTAGES

N. Matine, M. W. Dvorak, X. G. Xu, S. P. Watkins, and C. R. Bolognesi



- does not need B/C grading
- E/B band alignment through
  GaAsSb alloy ratio (strain)
  or InAlAs emitter
- somewhat poorer transport parameters to date for GaAsSb base

Single-HBTs: InGaAs base and InGaAs collector

low breakdown:
scaling beyond ~75 GHz
digital clock rate very difficult

high collector-base leakage
particularly at elevated temperatures.
Serious difficulties in real applications

very high thermal resistance
InGaAs collector and subcollector
can reduce with InP subcollector
limits power density
limits both digital and mm-wave application

Layer	Material	Doping	Thickness (Å)
Emitter cap	$In_{0.53}Ga_{0.47}As$	2×10^{19} cm^{-3}: Si	300
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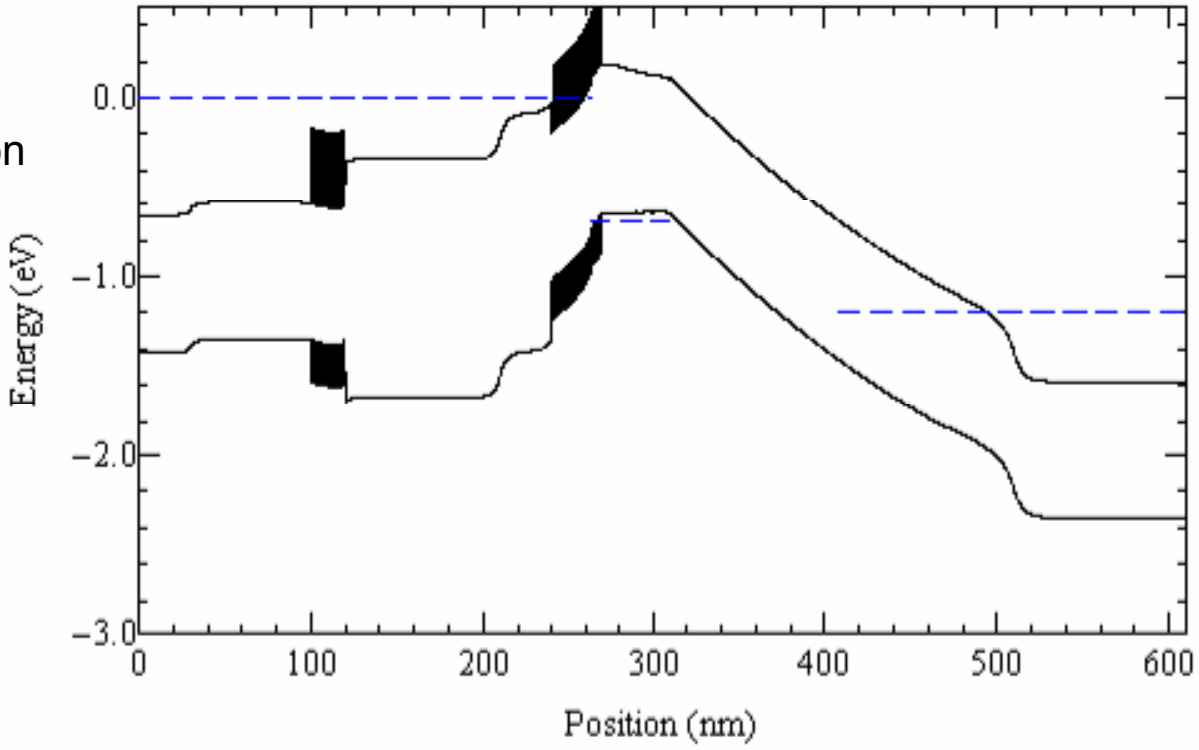
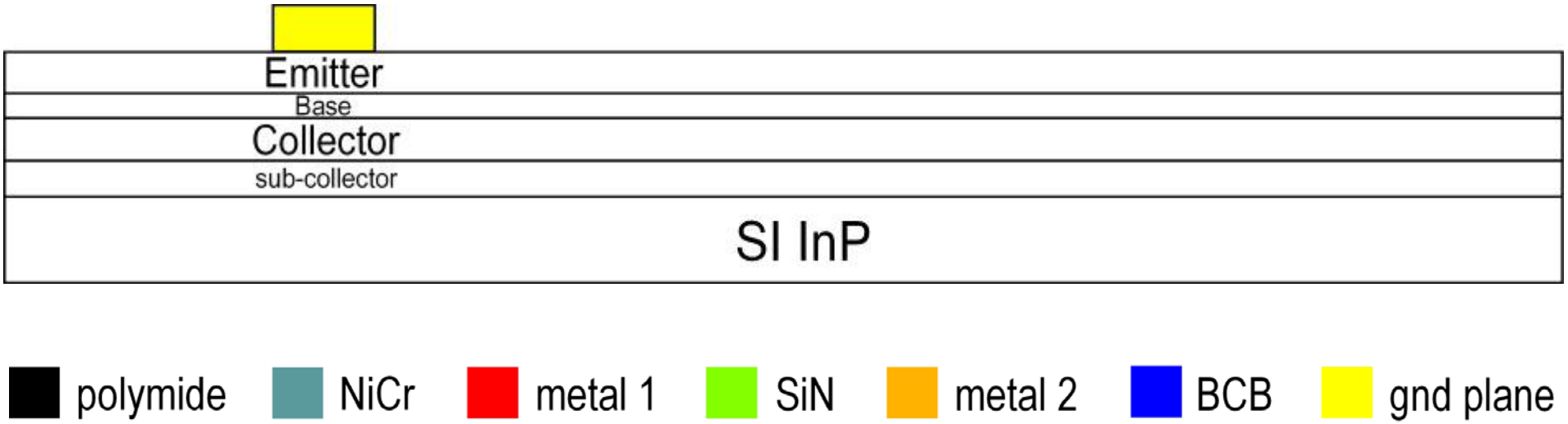
Emitter-base grade	$In_{0.53}Ga_{0.26}Al_{0.21}As$ to $In_{0.455}Ga_{0.545}As$	P: 4×10^{17} cm^{-3}: Si N: 8×10^{17} cm^{-3}: C	233 47
Base	$In_{0.53}Ga_{0.47}As$	N: 4×10^{19} cm^{-3}: C	400
Collector	$In_{0.53}Ga_{0.47}As$	N: 2×10^{16} cm^{-3}: Si	2000
Subcollector	InP	N: 1×10^{19} cm^{-3}: Si	~1000 Å



process flow

Basic Mesa IC Process

Z. Griffith
PK Sundararajan



Basic Mesa IC Process

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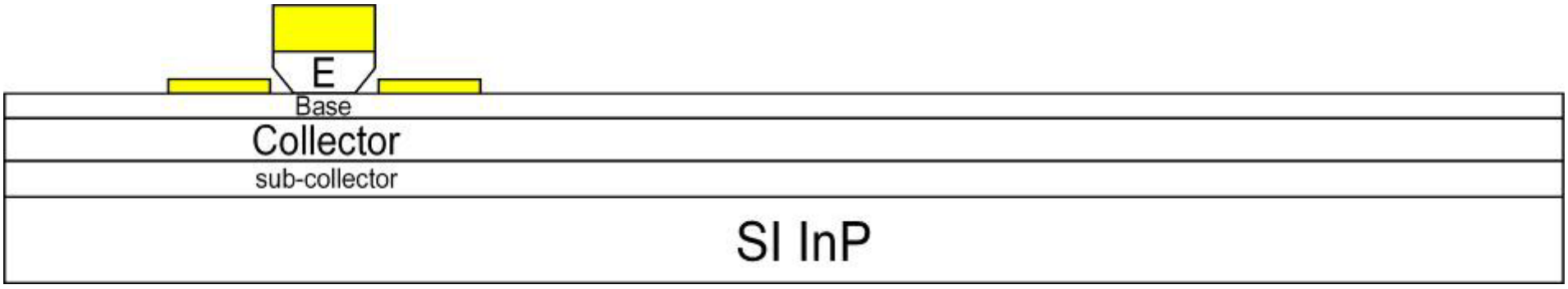
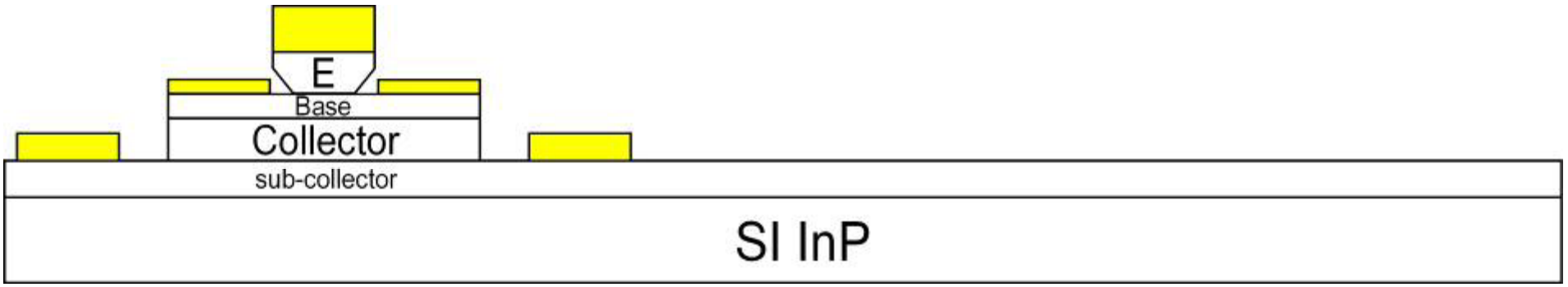
PK Sundararajan



polymide NiCr metal 1 SiN metal 2 BCB gnd plane

Basic Mesa IC Process

Z. Griffith
PK Sundararajan



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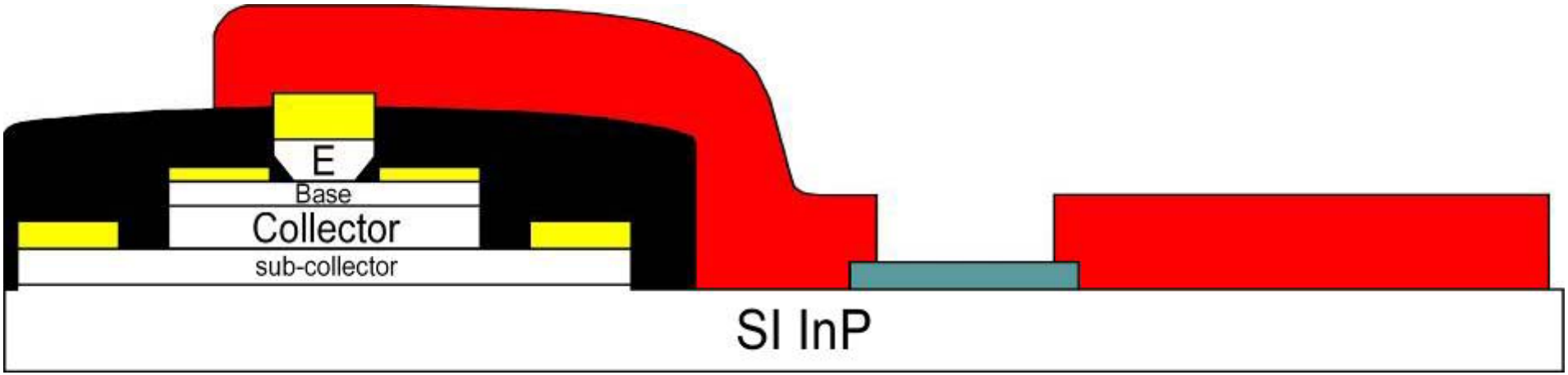

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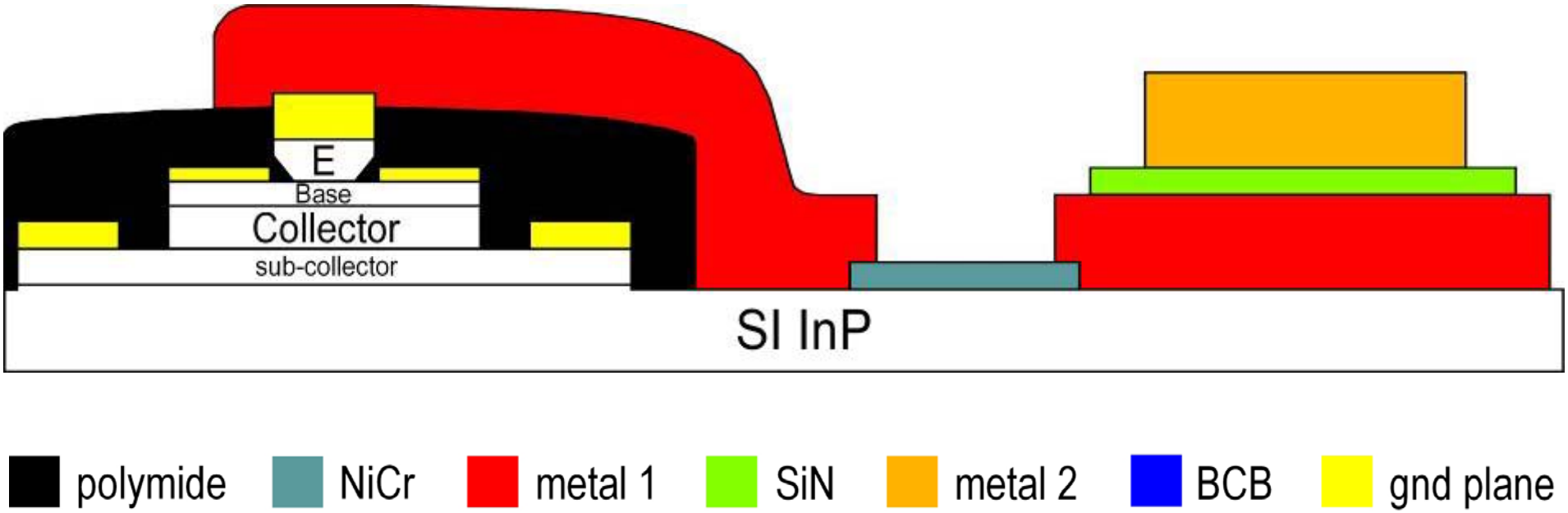

Basic Mesa IC Process

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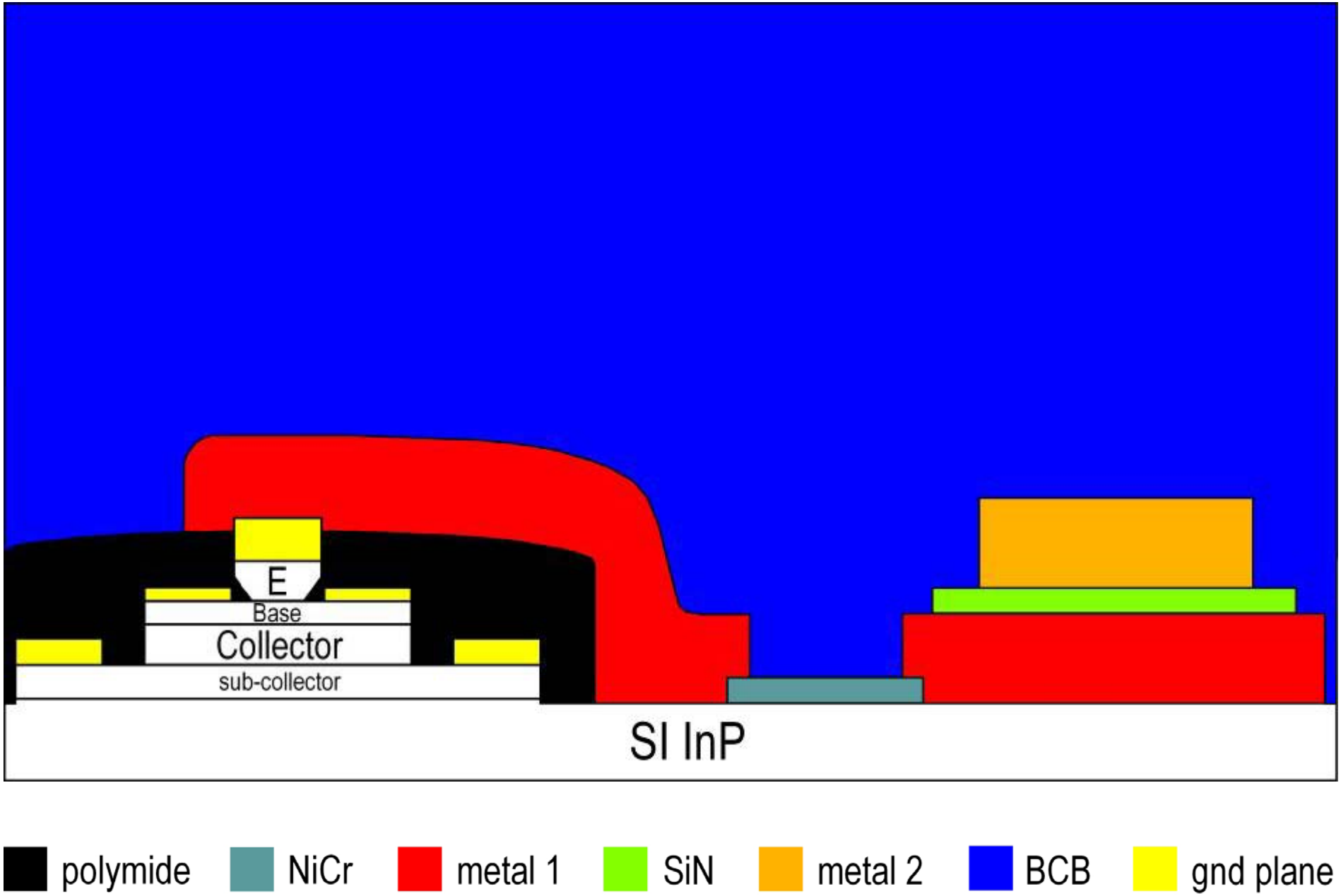

Basic Mesa IC Process

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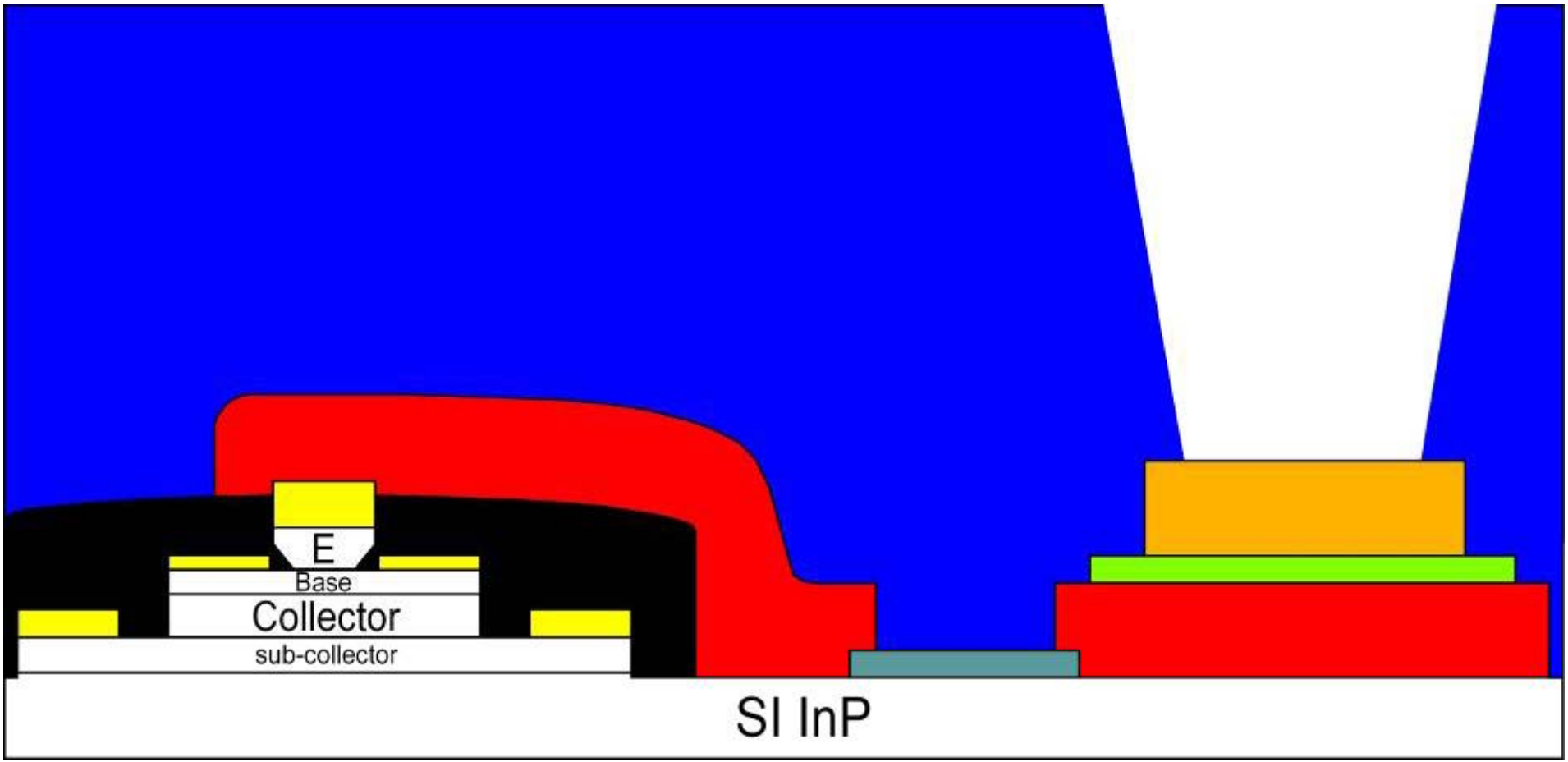

polymide NiCr metal 1 SiN metal 2 BCB gnd plane

Basic Mesa IC Process

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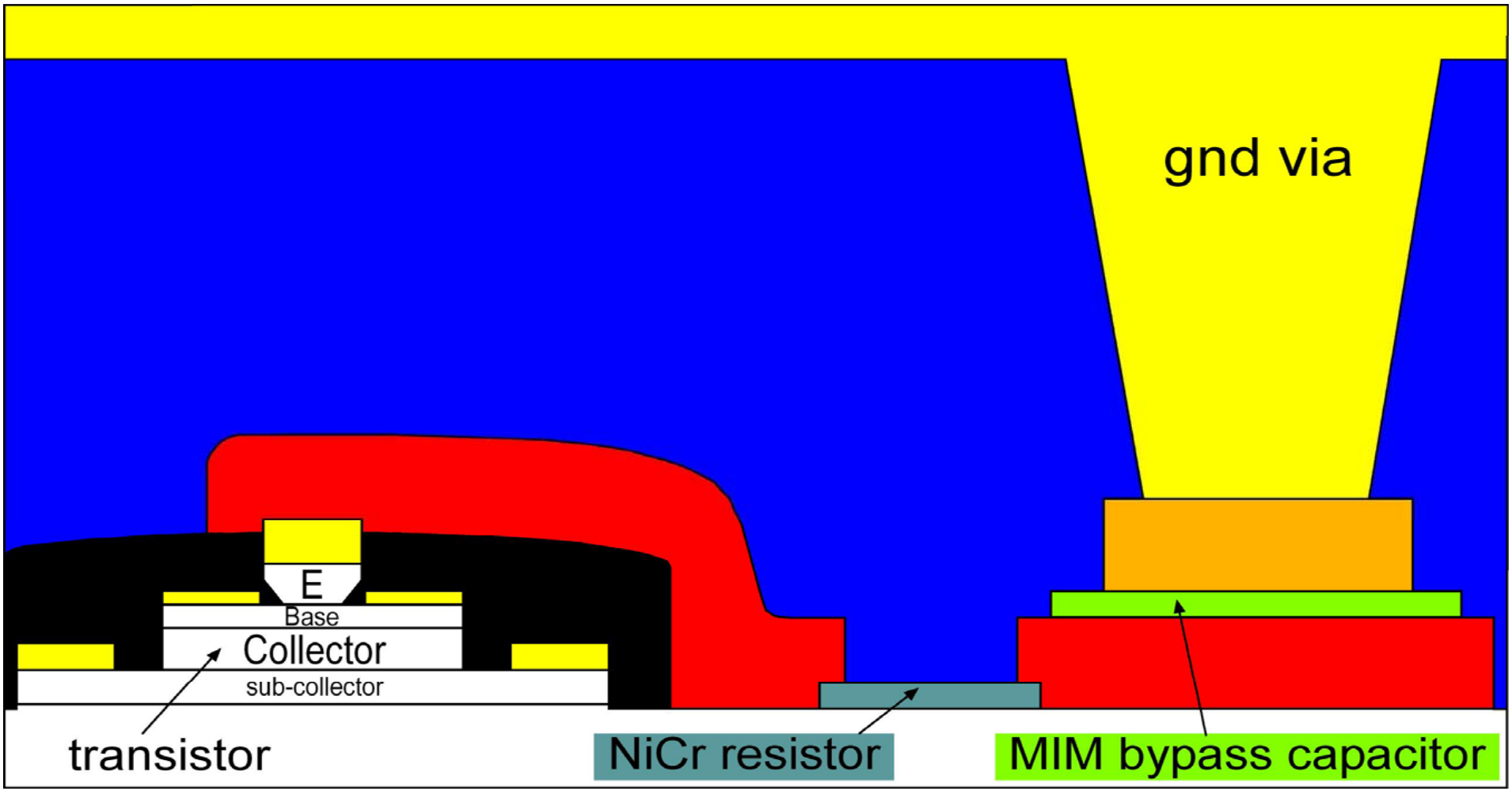
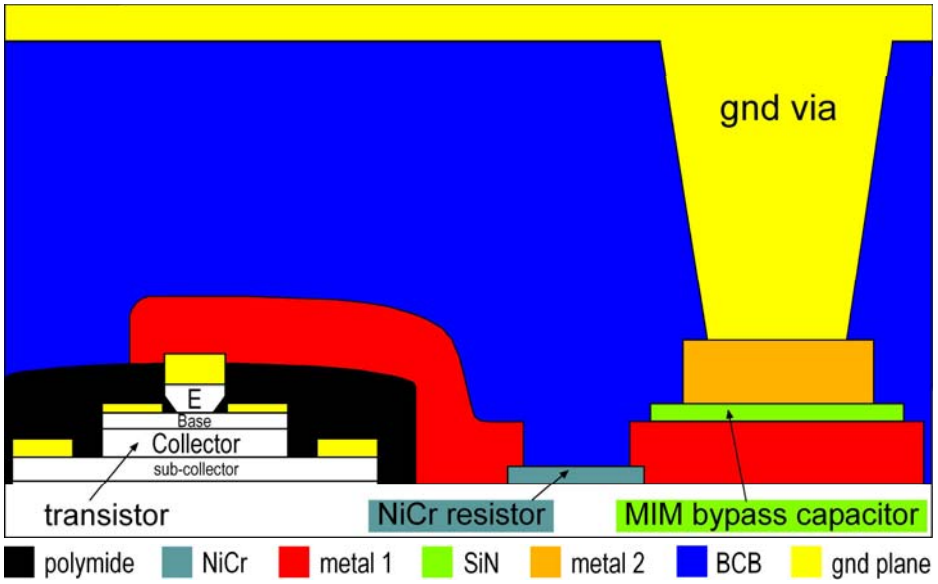


Basic Mesa IC Process

- Both junctions defined by selective wet-etch chemistry
- Narrow base mesa allows for low A_C to A_E ratio
- Low base contact resistance—
  Pd based ohmics with $\rho_C < 10^{-7}\ \Omega\cdot cm^2$
- Collector contact metal and metal '1' used as interconnect metal
- NiCr thin film resistors = 40 Ω / $\square$
- MIM capacitor, with SiN dielectric…
  -- used only for bypass capacitors
- Low loss, low ε_r = 2.7 microstrip wiring environment



- *Microstrip wiring environment*….
  - has predictable characteristic impedance
  - controlled-impedance interconnects within dense mixed signal IC's
  - ground plane eliminates signal coupling that occurs through on-wafer gnd-return inductance

Completed mesa HBTs & ICs

Mesa Process -- Without Passives & Interconnects

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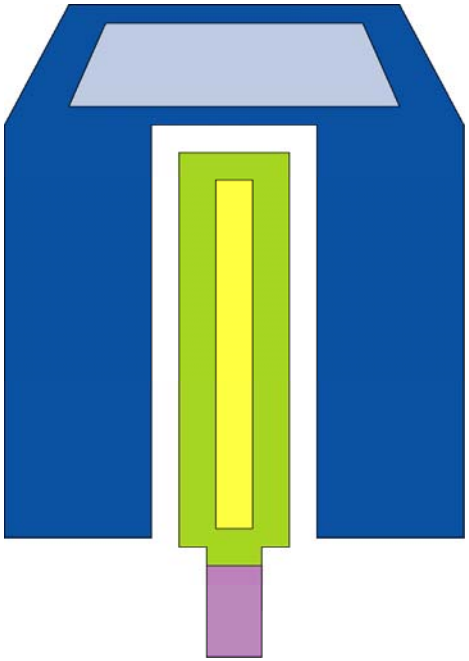
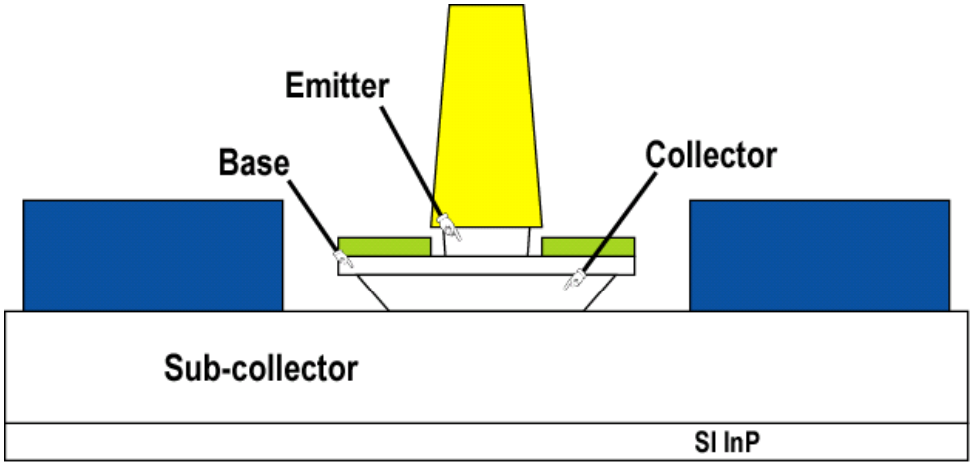
PK Sundararajan

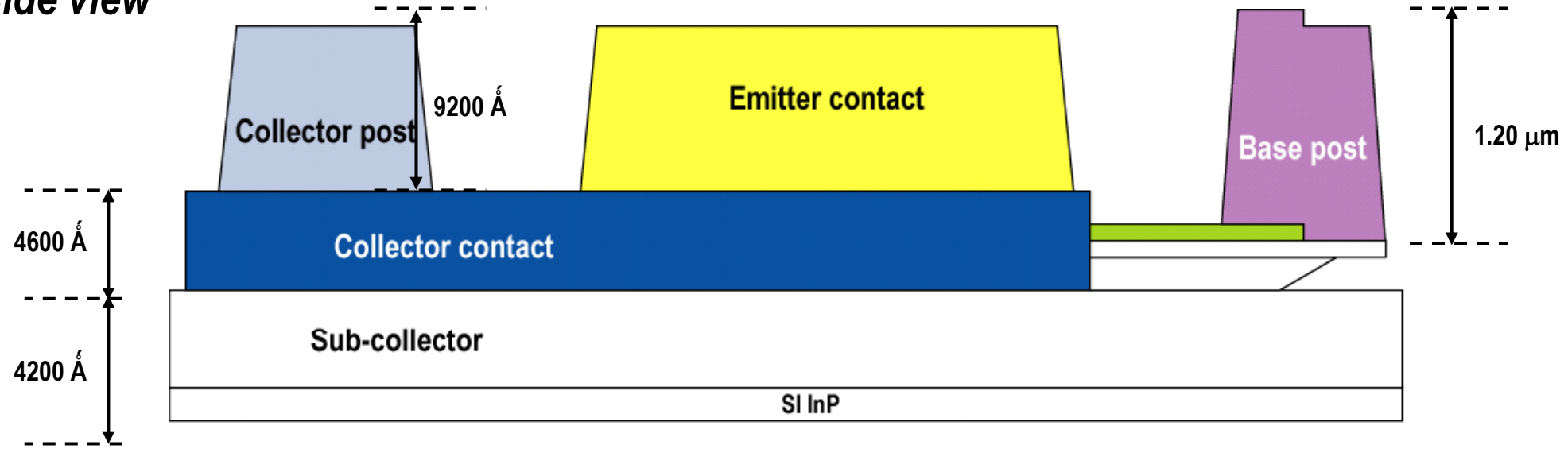
Top view



End view



Side view

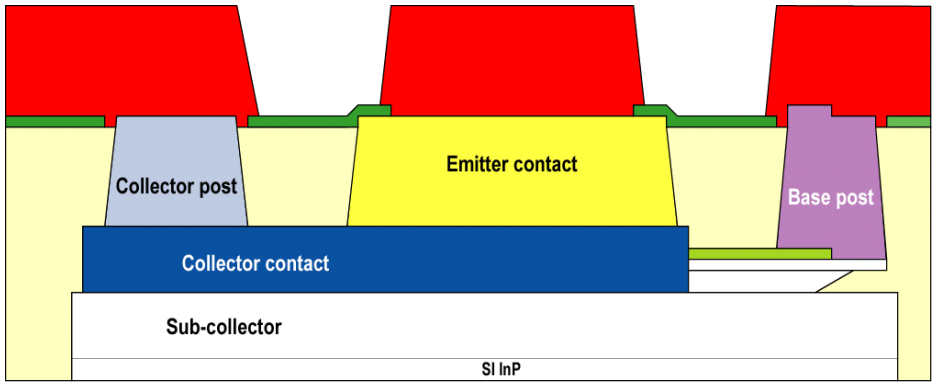


Mesa Process -- With Passives & Interconnects

Z. Griffith
PK Sundararajan

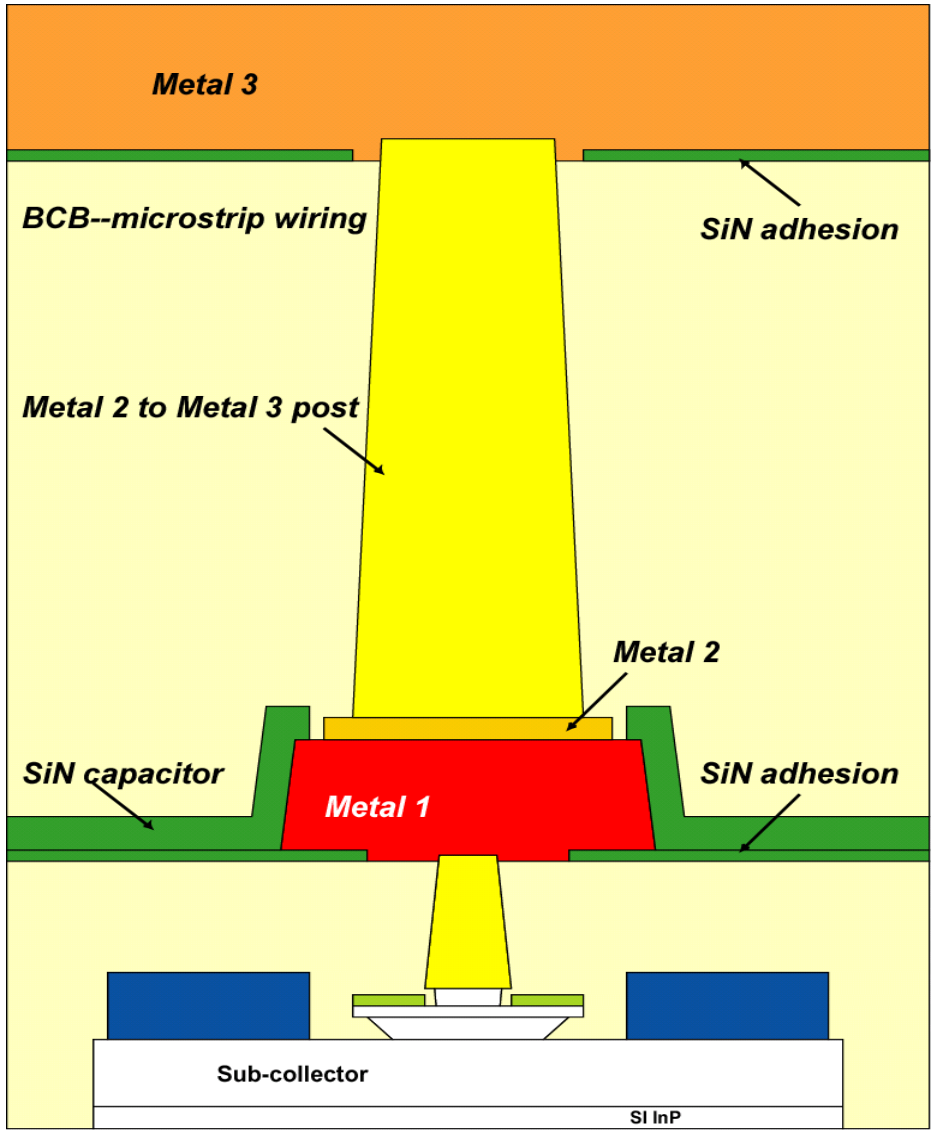
Process front end

- transistors, resistors, and M1 interconnects



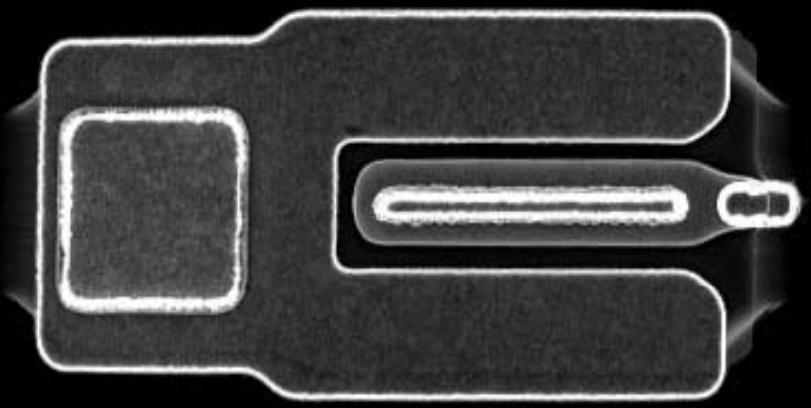
Process back end

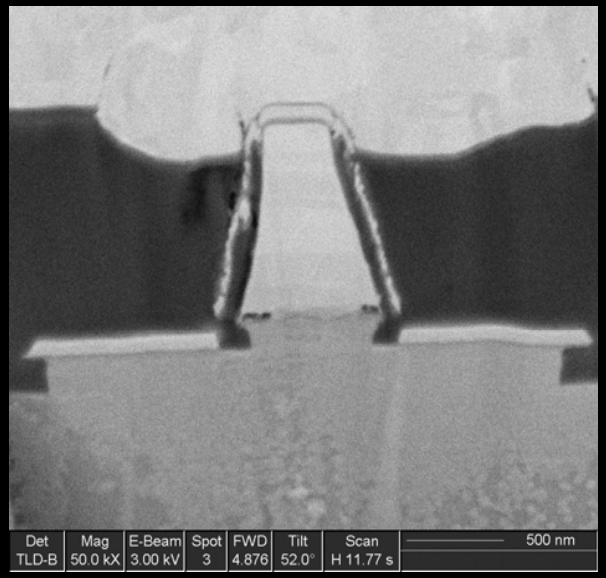
- capacitors, M2, and ground plane formation (M3)

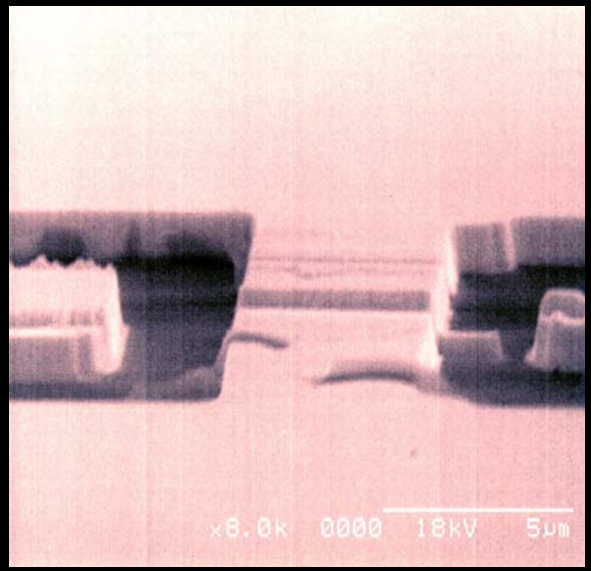


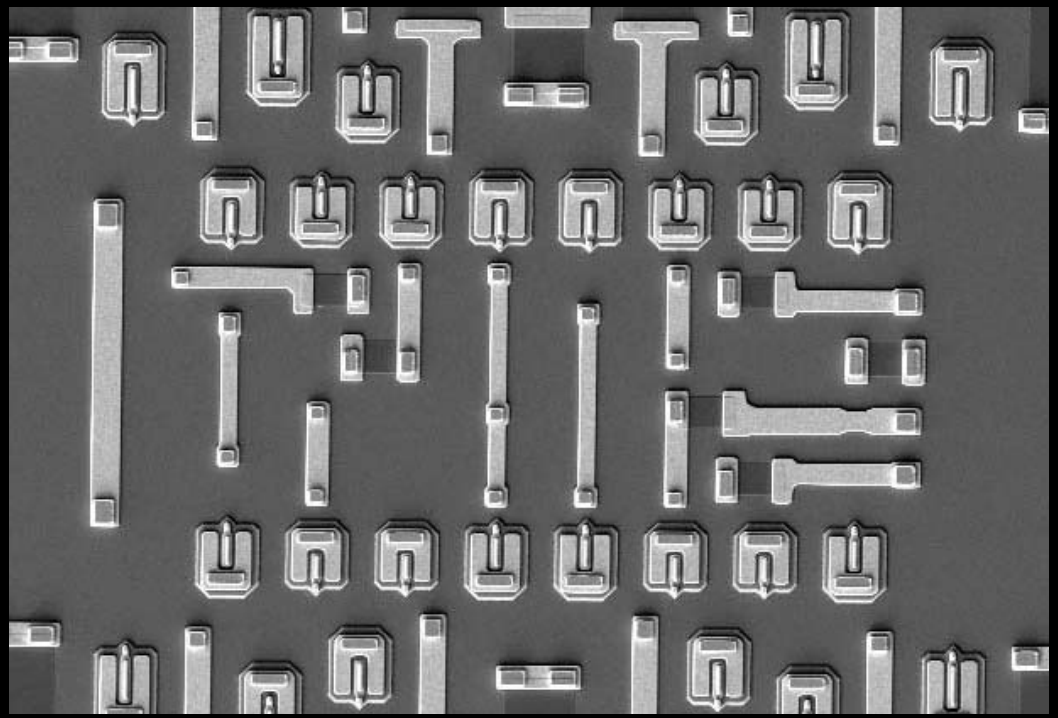
Zach Griffith

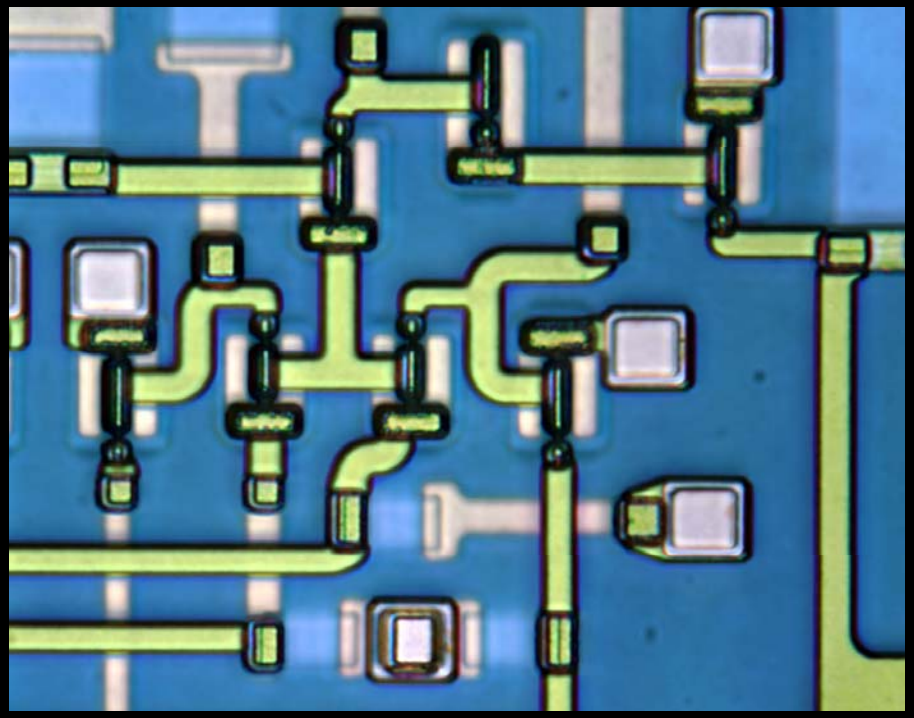
Mesa Process -- Some Pictures





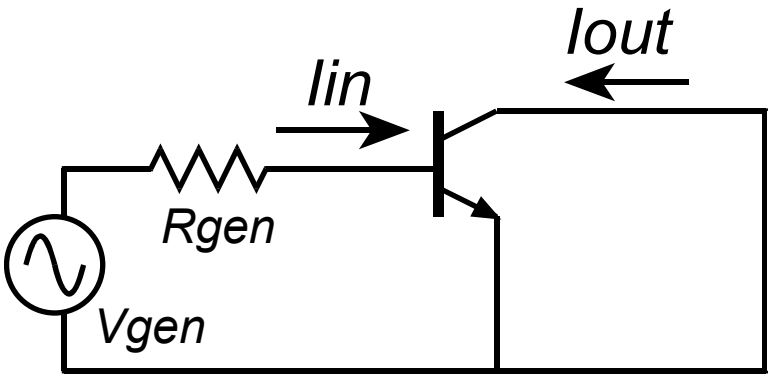






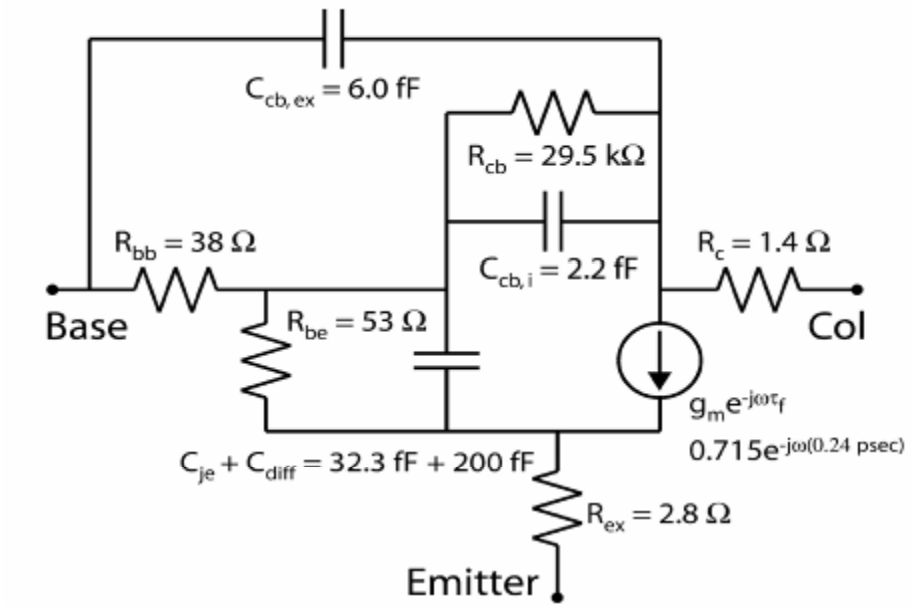
Transistor Figures of Merit

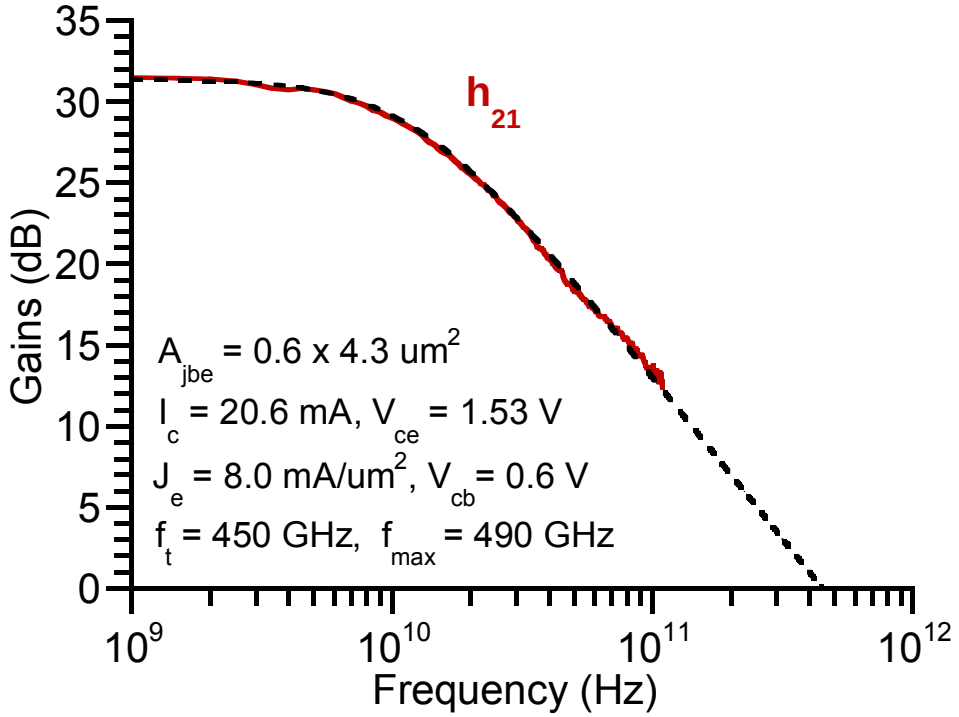
Short-circuit current-gain cutoff frequency



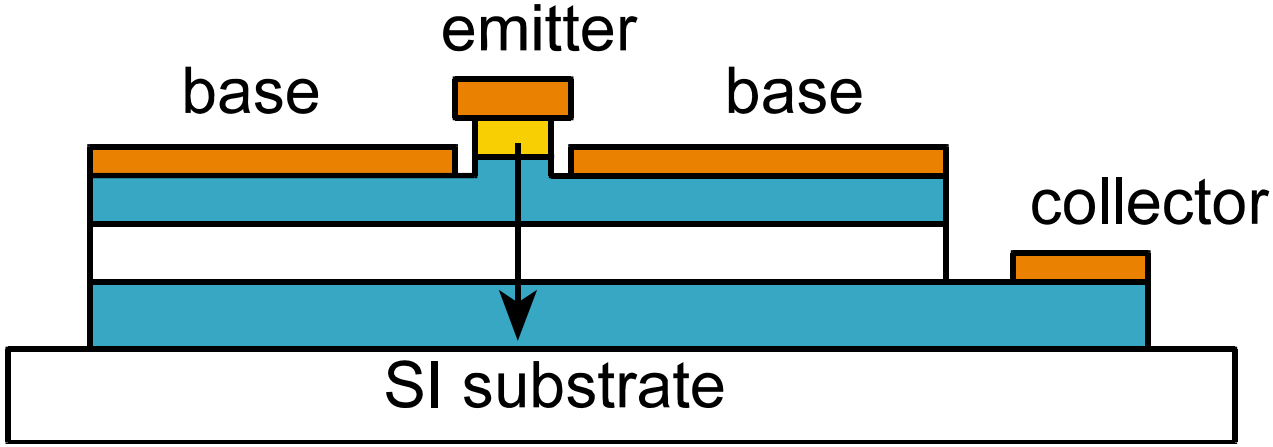
short-circuit current gain: drive input, short output, measure $H_{21}=I_{out}/I_{in}$

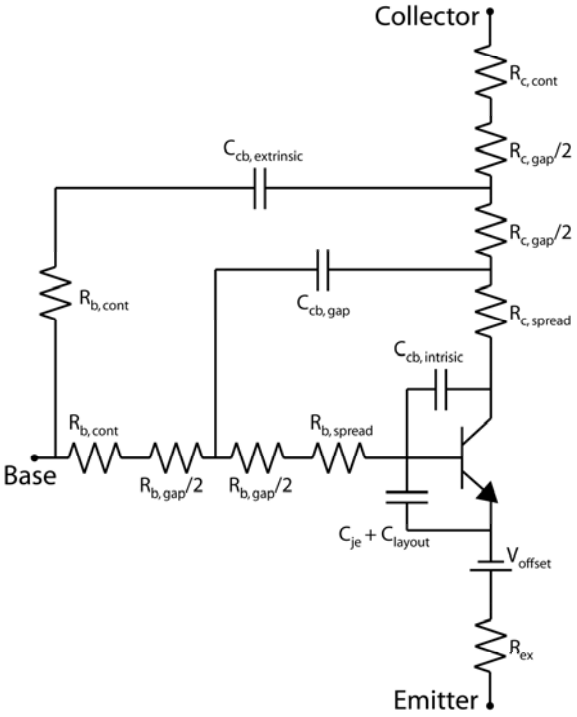
$$H_{21}(f) \approx \frac{1}{(1/\beta)+(jf/f_\tau)}$$





Current-gain cutoff frequency in HBTs





$$\frac{1}{2\pi f_\tau} = \tau_{base} + \tau_{collector} + C_{je}\frac{kT}{qI_E} + C_{bc}\left(\frac{kT}{qI_E} + R_{ex} + R_{coll}\right)$$

$$\tau_{base} \approx T_b^2 / 2D_n \qquad \tau_{collector} \approx T_c / 2v_{eff}$$

RC terms are quite important for high bandwidth devices

...layers can always be thinned until RC terms dominate !

Definition of power gains and f_{max}

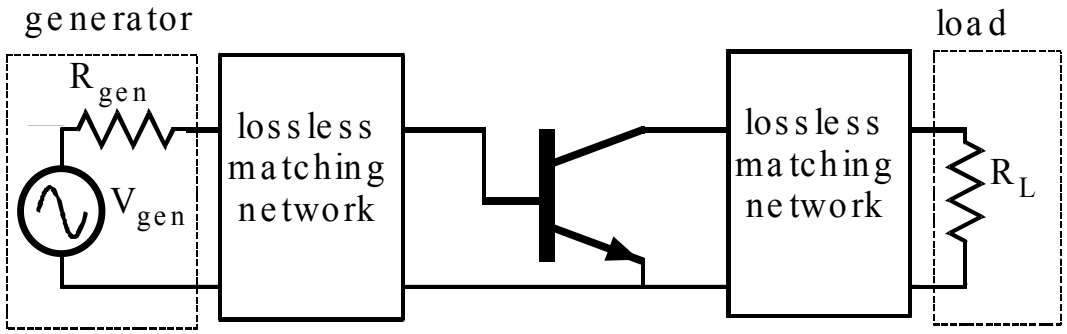
MSG/MAG is of direct relevance in tuned RF amplifier design

Maximum Available Gain

Simultaneously match input and output of device

$$\mathbf{MAG} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right)$$

K = Rollet stability factor



Transistor must be unconditionally stable or MAG does not exist

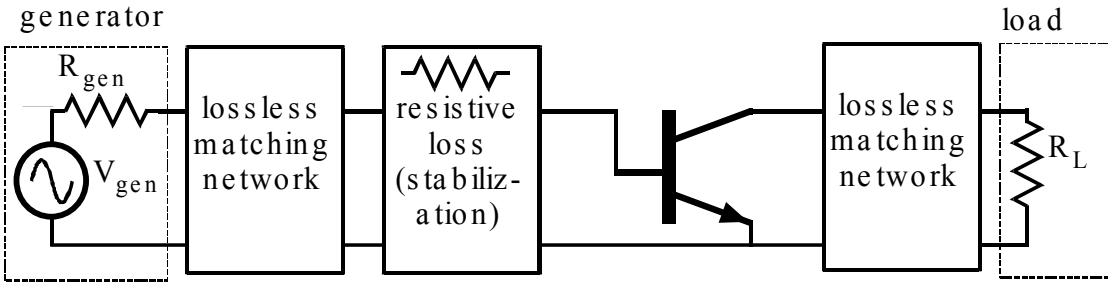
Maximum Stable Gain

Stabilize transistor and simultaneously match input and output of device

$$\mathbf{MSG} = \frac{|S_{21}|}{|S_{12}|} = \frac{|Y_{21}|}{|Y_{12}|} \approx \frac{1}{\omega C_{cb}\left(R_{ex} + kT/qI_c\right)}$$

Approximate value for hybrid-π model

To first order MSG does not depend on f_τ or R_{bb}



For Hybrid- π model, MSG rolls off at 10 dB/decade, while MAG has no fixed slope. So, NEITHER can be used to accurately extrapolate f_{max}

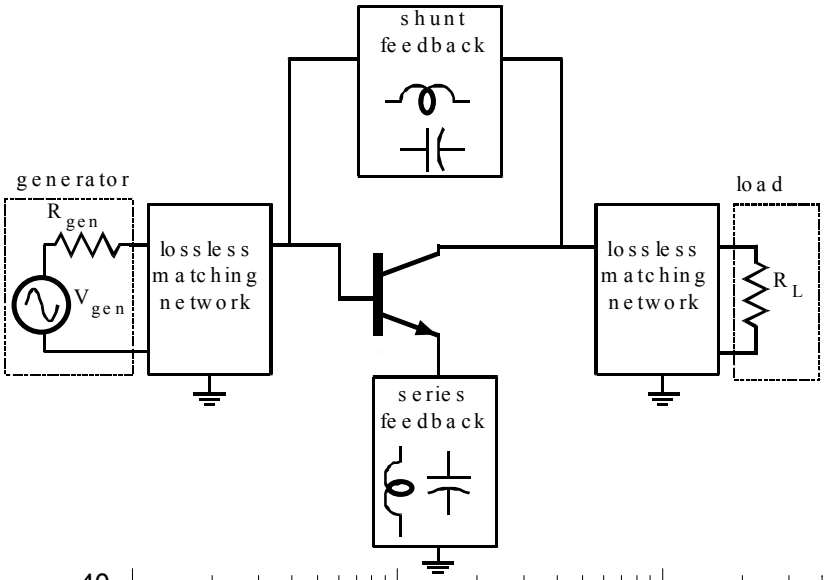
Unilateral Power Gain

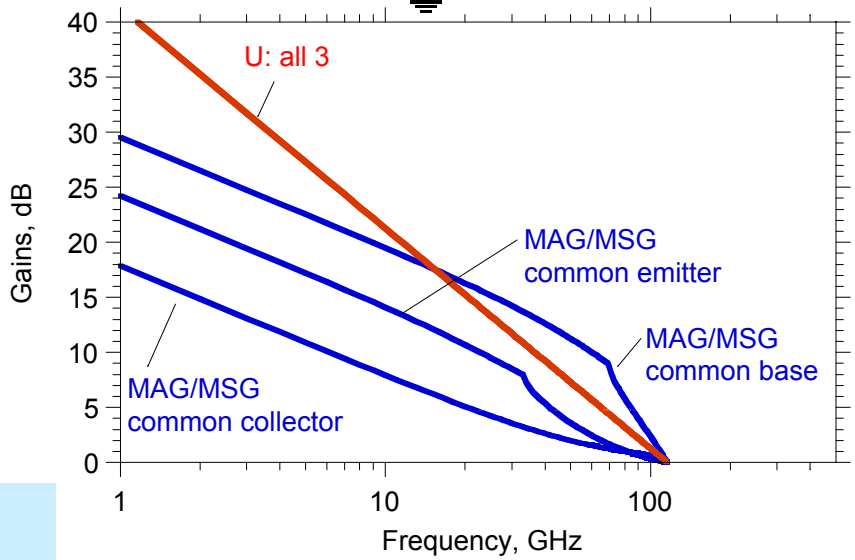
Mason's Unilateral Power Gain

Use lossless reactive feedback to cancel device feedback and stabilize the device, then match input/output.

$$\mathbf{U} = \frac{\left|Y_{21} - Y_{12}\right|^2}{4\left(G_{11}G_{22} - G_{21}G_{12}\right)}$$

U is not changed by pad reactances



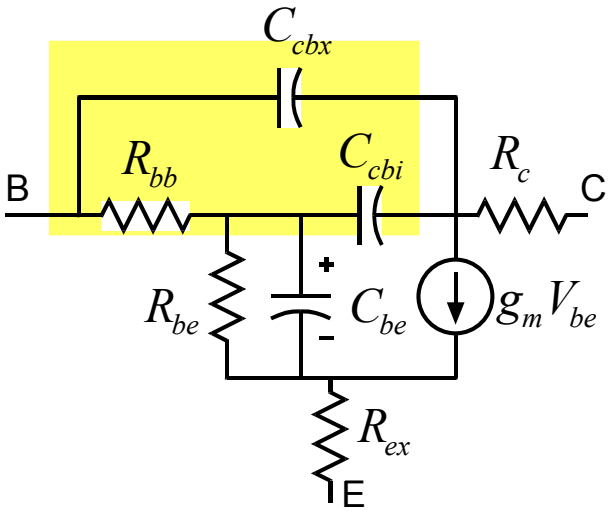


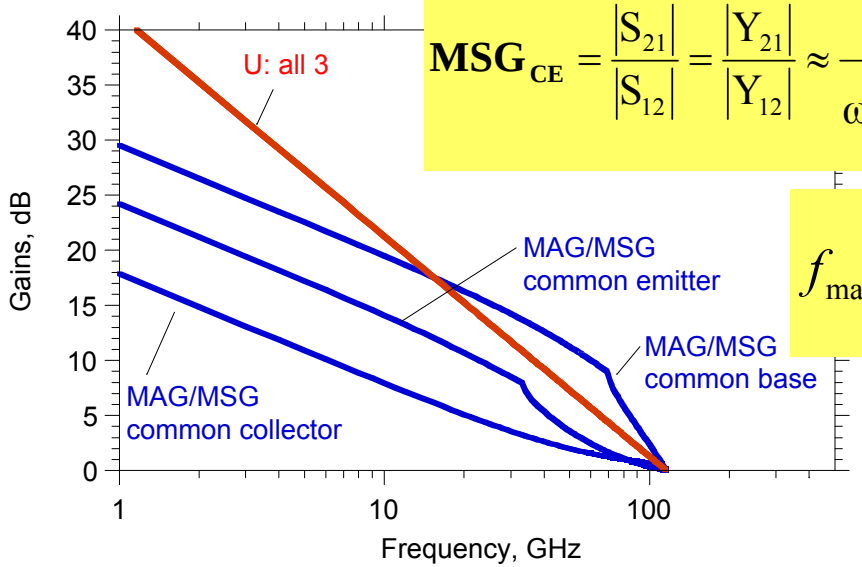
For Hybrid- π model,
U rolls off at 20 dB/decade

ALL Power Gains must be unity at f_{max}

Monolithic amplifiers are not easily made unilateral, so U of only historical relevance to IC design.
U is *usually* valuable for f_{max} extrapolation

Excess Collector Capacitance, Fmax, and Device Utility





$$\mathbf{MSG_{CE}} = \frac{|S_{21}|}{|S_{12}|} = \frac{|Y_{21}|}{|Y_{12}|} \approx \frac{1}{\omega C_{cb}\left(R_{ex} + kT/qI_c\right)}$$

$$f_{max} \cong \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cbi}}}$$

The partitioning between C_{cbi} and C_{cbx} will be discussed later.

C_{cbx} has no effect upon f_{max} or U.

C_{cbx} has a large impact upon common - emitter MSG,

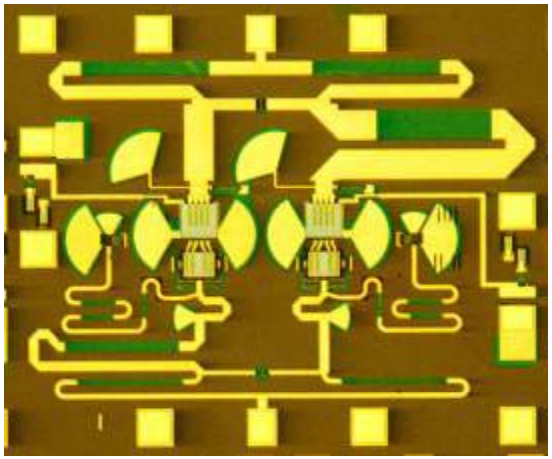
hence has large impact on usable gain in mm - wave circuits.

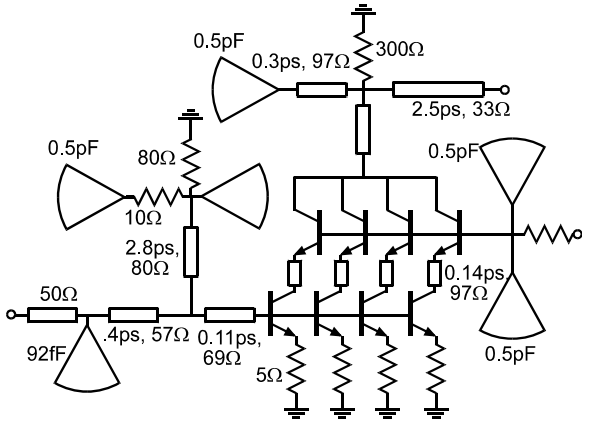
C_{cbx} has a large impact upon digital logic speed.

high f_{max} does not mean low C_{cb} or fast logic

What do we need: f_t , f_{max} , or … ?

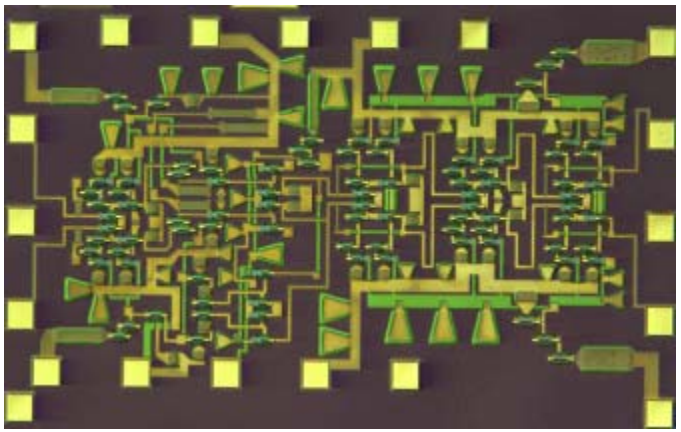
Tuned ICs (MIMICs, RF):
fmax sets gain,
& max frequency, not ft.
…low ft/fmax ratio makes tuning design hard (high Q)
high C_{cbx} reduces MSG

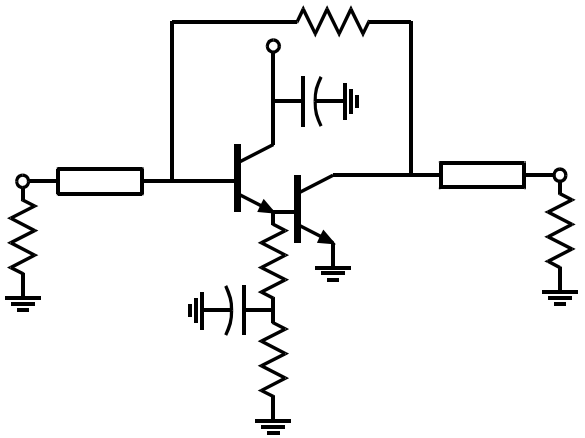




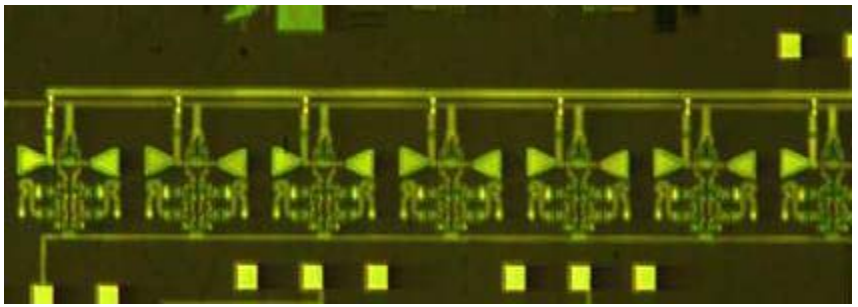
Lumped analog circuits
need high & comparable ft and fmax.

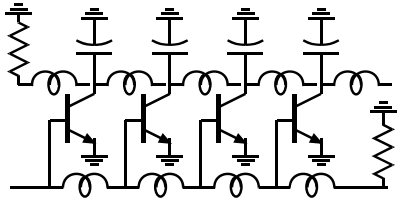
C_{cb}/I_c has major impact upon bandwidth





Distributed Amplifiers
in principle, fmax-limited,
ft not relevant….
(low ft makes design hard)

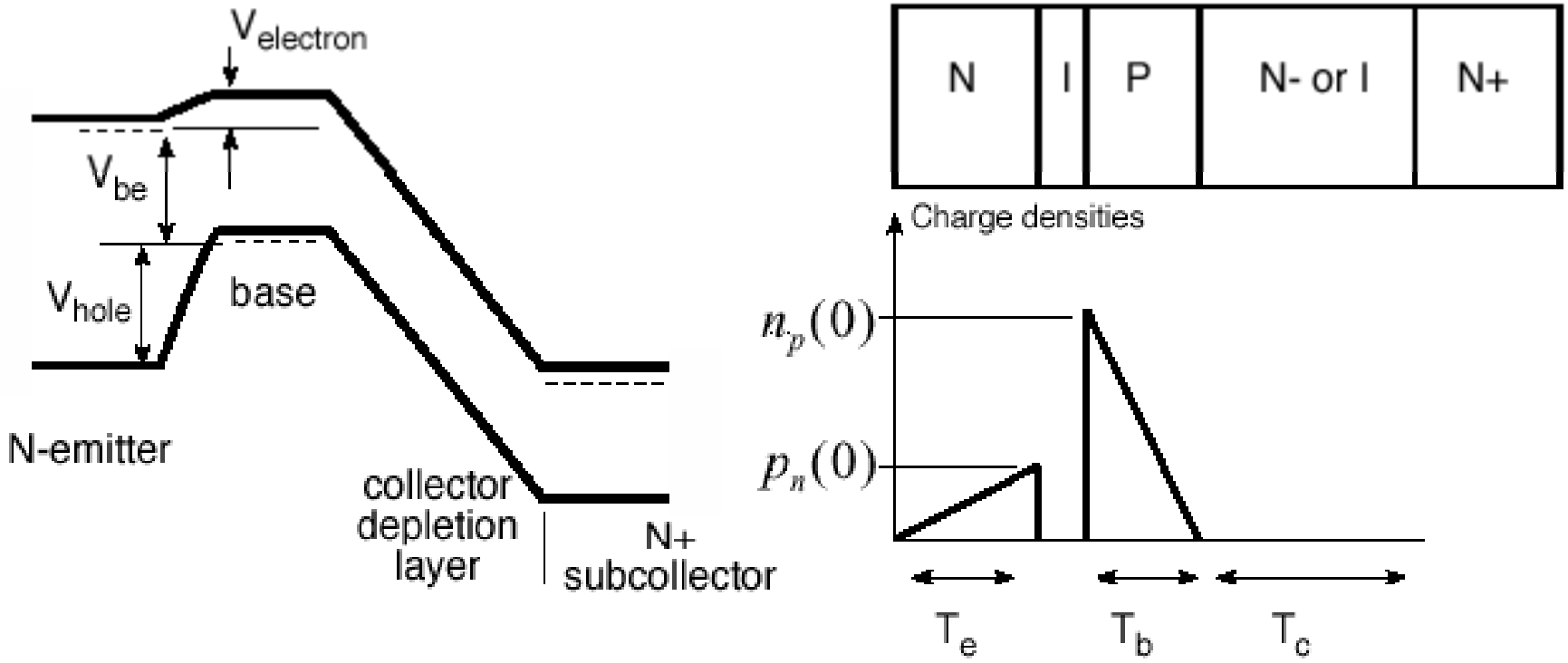




digital ICs will be discussed in detail later

transistor electrical parameters

HBT DC Characteristics



$$n_p(0) = qN_c e^{-qV_{electron}/kT} \propto e^{+qV_{be}/kT}$$ electron concentration at emitter edge of base

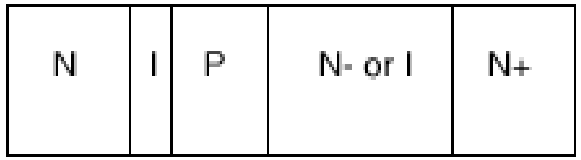
$$p_n(0) = qN_v e^{-qV_{hole}/kT} \propto e^{+qV_{be}/kT}$$ hole concentration at base edge of emitter
heterojunction makes this small

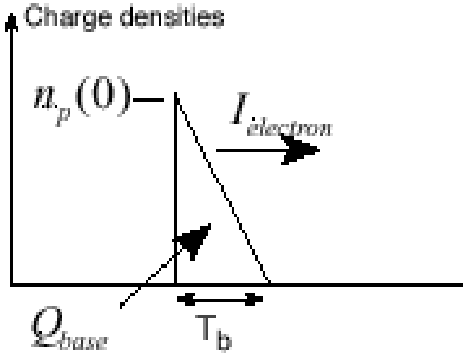
$$I_{electron} = \frac{D_n q A_e N_c}{T_b} e^{-qV_{electron}/kT} \propto e^{+qV_{be}/kT}$$ electron current from emitter to collector

$$g_m \equiv \frac{dI_c}{dV_{be}} = \frac{qI_c}{kT}$$ transconductance

HBT transit times

Base Transit Time





electron concentration at emitter edge of base

$$n_p(0) = qN_c e^{-qV_{electron}/kT} \propto e^{+qV_{be}/kT}$$

electron current from emitter to collector

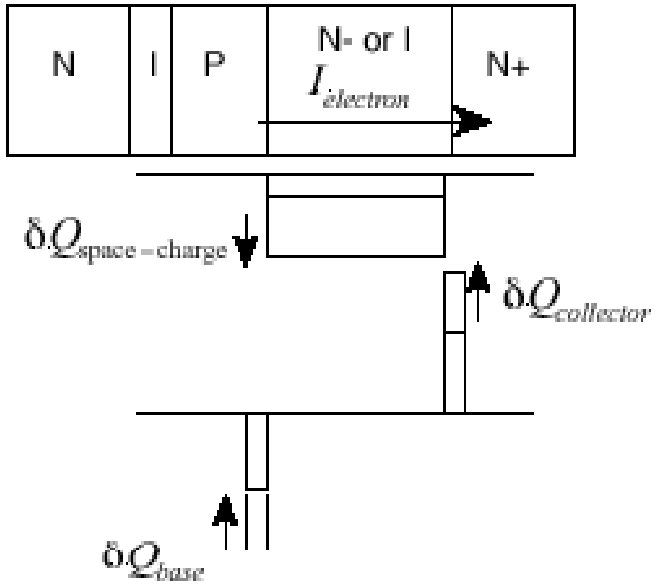
$$I_{electron} = qn_p(0)D_n / T_b$$

stored base charge

$$Q_{base} = qA_e n_p(0)T_b / 2$$

$$.. \quad = I_{electron}T_b^2 / 2D_n = \tau_b I_{electron}$$

Collector Transit Time



depletion-layer space-charge

$$\delta Q_{space-charge} = \frac{T_c}{v_{sat}} \delta I_{collector}$$

change in base stored charge

$$\delta Q_{base} = \delta Q_{collector} = \delta Q_{space-charge} / 2$$

$$.. \quad = \delta I_{collector}\left(T_c / 2v_{sat}\right) = \tau_c \delta I_{collector}$$

"Diffusion Capacitance"

$$C_{diffusion} \equiv \frac{dQ_{base}}{dV_{be}} = \frac{dQ_{base}}{dI_c}\frac{dI_c}{dV_{be}} = \left(\tau_b + \tau_c\right)g_m$$

$C_{be,\ diffusion} = g_m\left(\tau_b + \tau_c\right)$ fictitious capacitance between base & emitter modelling charge storage

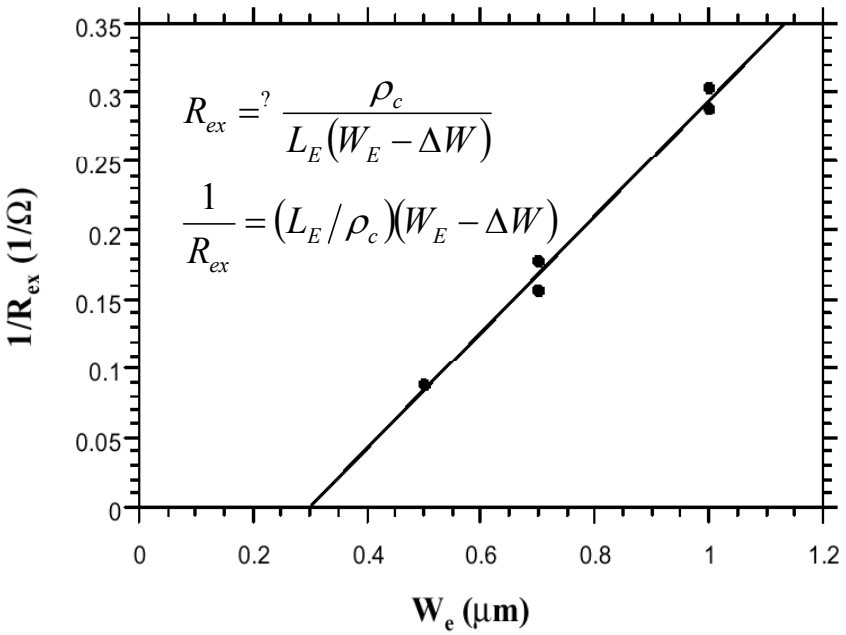
Emitter Resistance

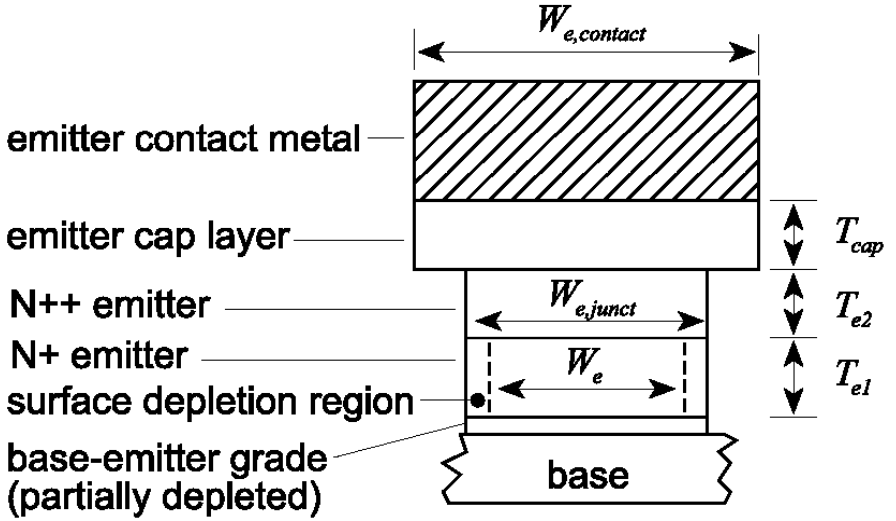
Emitter resistance : one limiting factor in scaling for speed

high speed devices : high $J \rightarrow$ low $\left(C_{cb}/I_c\right)$

but high $J \rightarrow$ excessive $\left(I_E R_{ex}\right)$ voltage drop

evidence of edge depletion or damage





Low resistance obtained with $In_xGa_{1-x}As$ emitter caps with high In fraction.

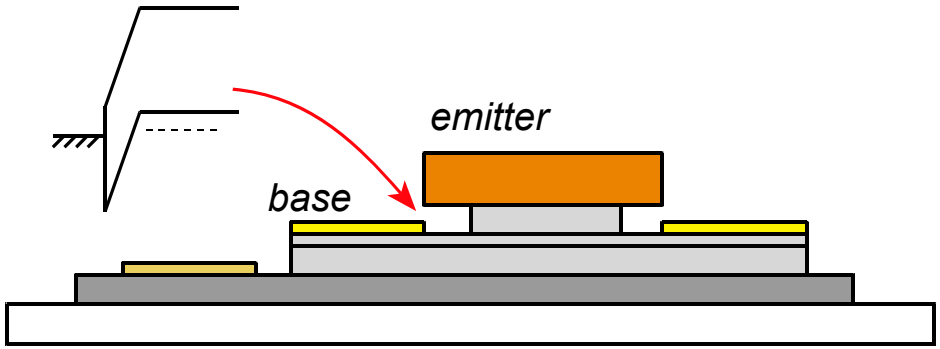
Process control for removal of surface oxides is important.

Ti/Pt/Au contacts still best at present

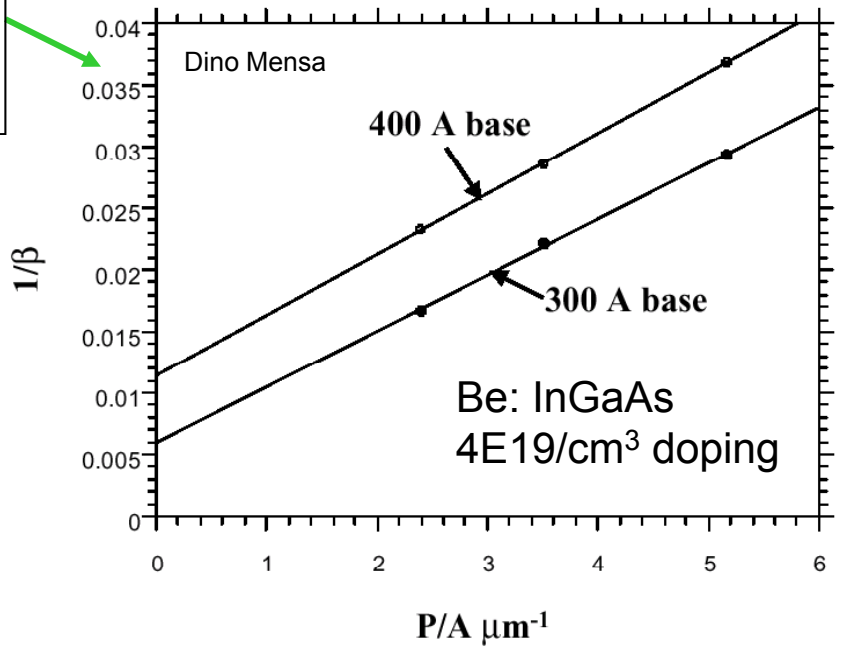
Current Gain: surface conduction, not recombination

Surface Conduction:
InGaAs has low surface recombination velocity.
InGaAs has surface pinning near conduction band.
→ weak surface inversion layer on base, surface conduction to base contact
Problem aggravated by InP emitter, as this also pins near conduction band

$$\frac{1}{\beta} = \frac{I_b}{I_c} = \frac{I_{surface}}{I_c} + \frac{I_{bulk}}{I_c}$$
$$= \frac{P_E(k_1 q n_{po})}{A_E(q n_{po} D_n / W_b)} + \frac{1}{\beta_{bulk}}$$



evidence of surface conduction

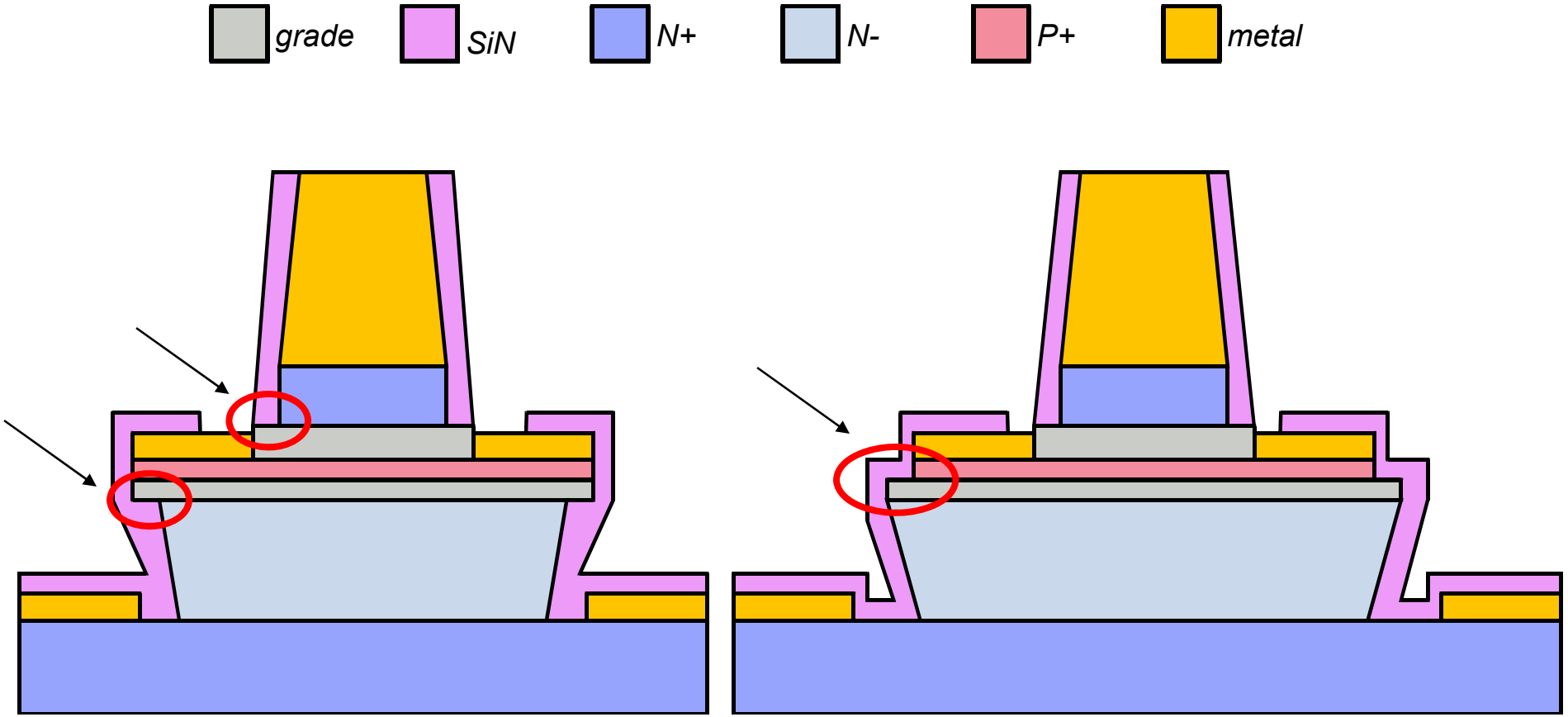


Passivation with Silicon Nitride: Ledges

Literature suggests that coating InP with Silicon Nitride produces surface states ~200 meV below conduction band edge → surface pinning → leakage

Use InGaAs/InAlAs grades (sketches below) to form ledges: surface pinning for SiN-coated InAlAs is ~400 meV below band edge.

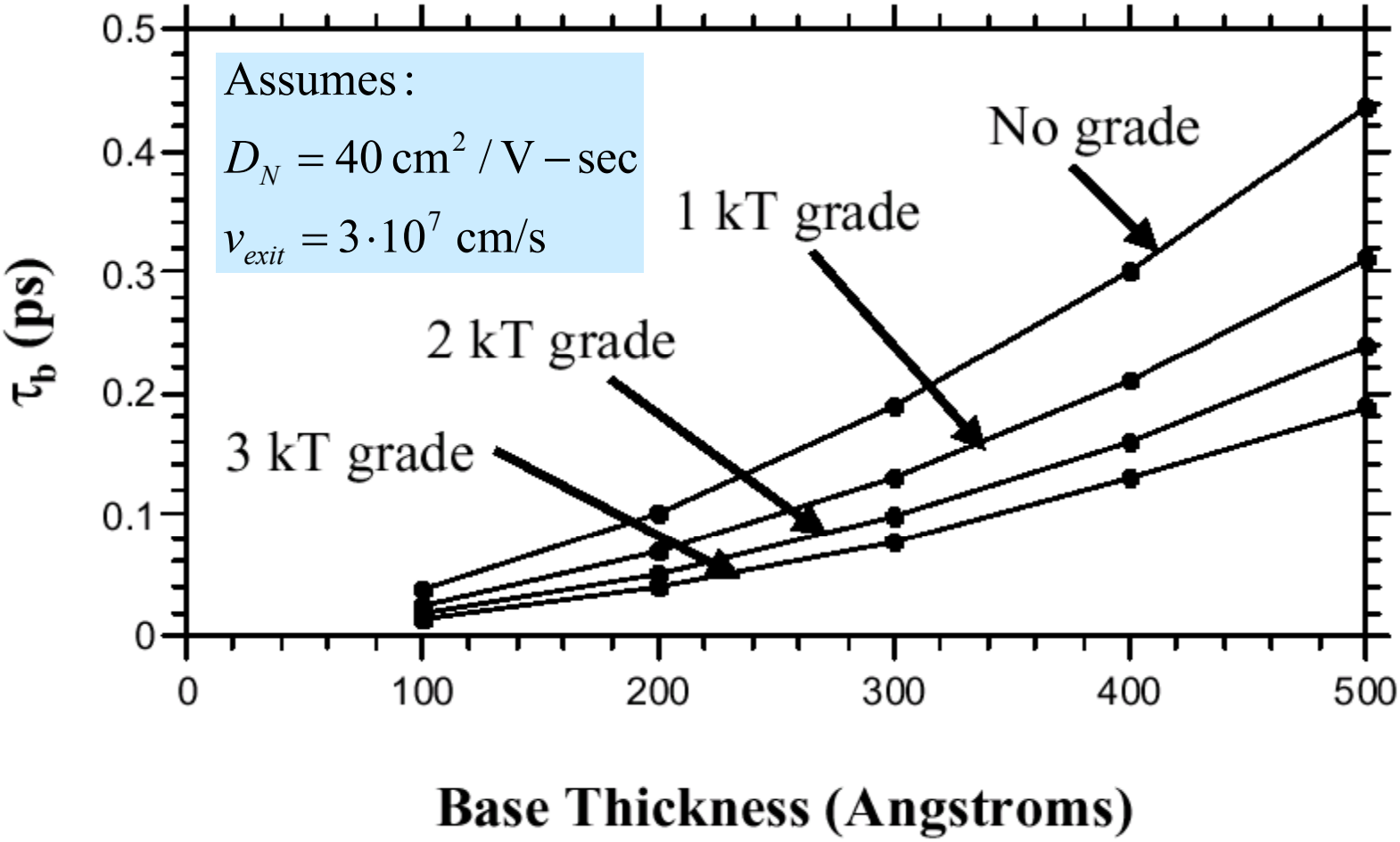
Not understood; some processes with SiN on InGaAs or InP still have low leakage.



base parameters

Base Transit Time

Dino Mensa



$$\tau_b = W_b L_g / D_n - \left(L_g^2 / D_n - L_g / v_{sat}\right)\left(1 - e^{-W_b / L_g}\right)$$

where L_g is the grading length:

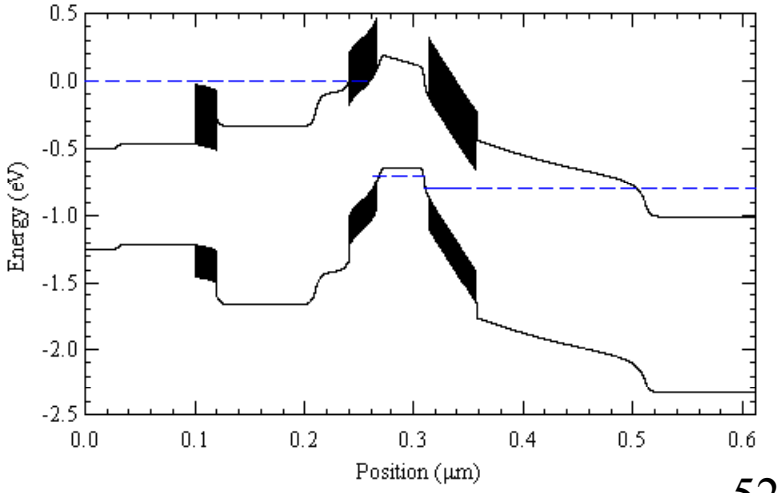
$$L_g = W_b\left(kT / \Delta E_g\right)$$

Drift - diffusion model correct if

$\tau_b >> \tau_m \approx D_n m^* / kT \approx 35$ fs

Dino Mensa
Miguel Urteaga
Mattias Dahlström

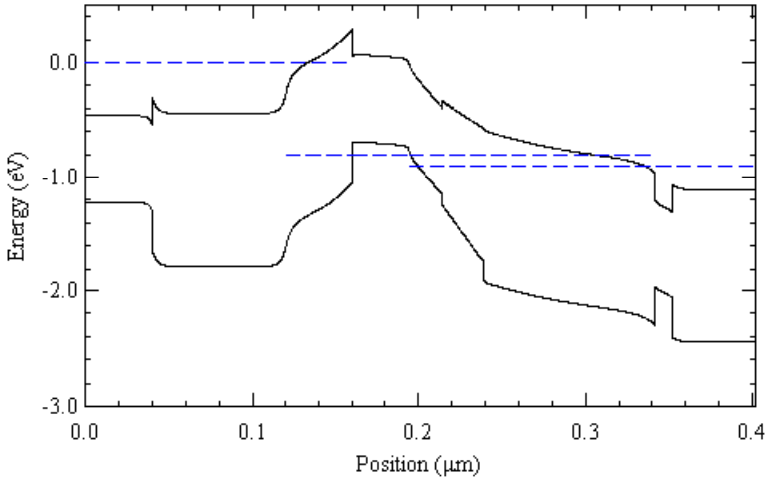
Base Transit Time: Grading Approaches



Compositional grading: strained graded InGaAs base
Base-emitter junction with InAlAs/InGaAs CSL

UCSB data showed limited improvement with > 50 meV grading
Findings similar to that of Ritter Group /Technion
Stain effects on bandgap must be included in grade design

52 meV potential drop : $In_{0.455}Ga_{0.545}As \leftrightarrow In_{0.53}Ga_{0.47}As$ (strained)



Doping grading: carbon graded from ~8 to 5E19
Abrupt (InP-InGaAs) base-emitter junction

Analyses by Ishibashi, others, suggests that abrupt launcher has minimal effect on transit time in > 30 nm bases

Doping grading is only effective for degenerate base doping; otherwise large doping change induces only small field but requires large sacrifice in base sheet resistance

UCSB has used both approaches; neither appears to be conclusively superior .

Limits on Base Doping

Loss of current gain due to Auger Recombination

At high dopings, bulk recombination dominated by Auger

$\tau_{\text{Auger}} \propto 1/N_A^2$

Since $\tau_{\text{base}} \propto 1/T_B^2 \quad \Rightarrow \beta \propto 1/(N_A T_B)^2 \propto 1/\rho_{sheet}^2$

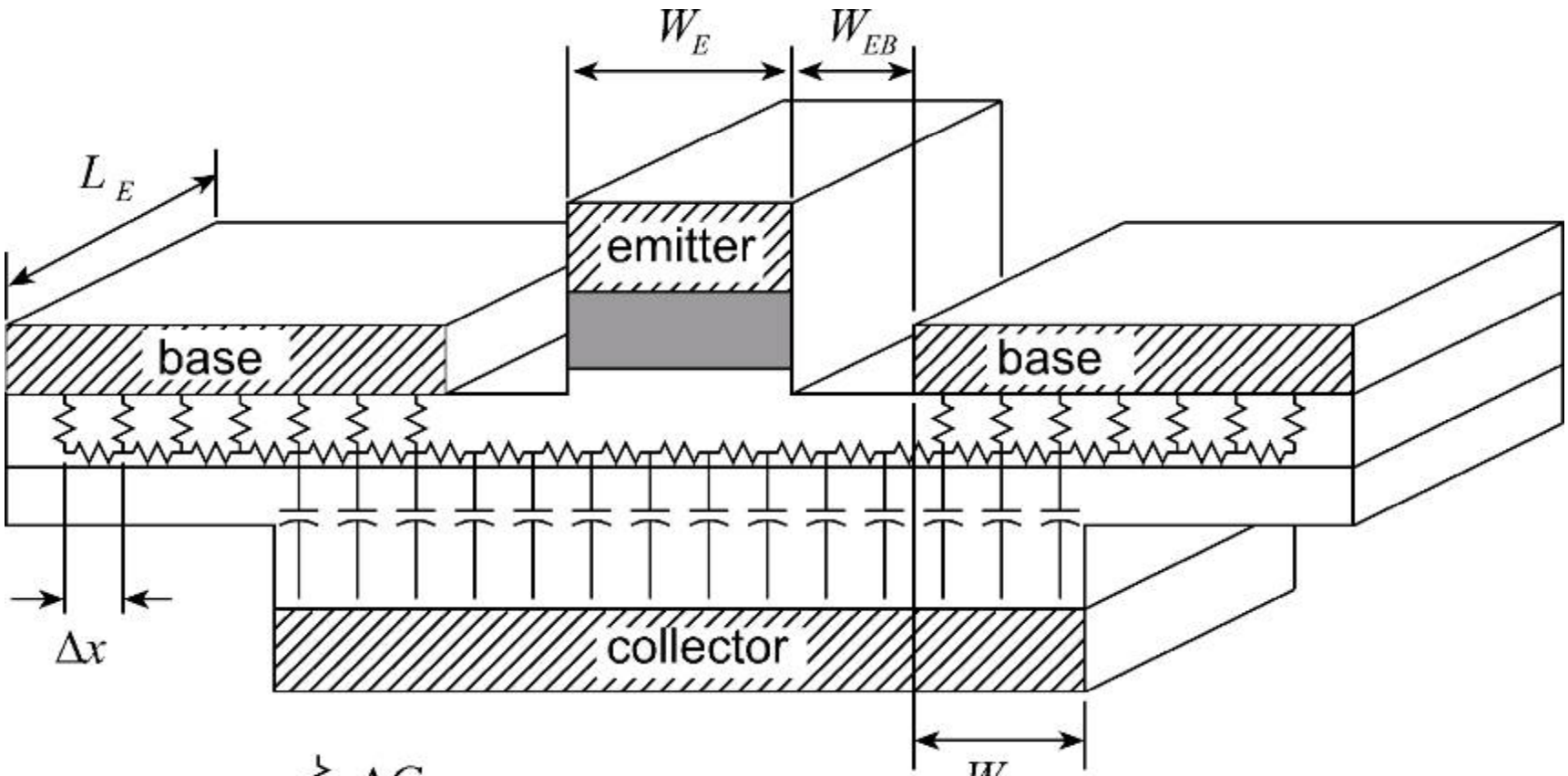
For doping $> 10^{20}/\text{cm}^3$, we observe more rapid decrease of β than $1/\rho_{sheet}^2$.

Causes : effect of high carbon concentration on strain ?

very low acceptor ionization ?

base-collector RC parasitics

Base-Collector Distributed Model: exact



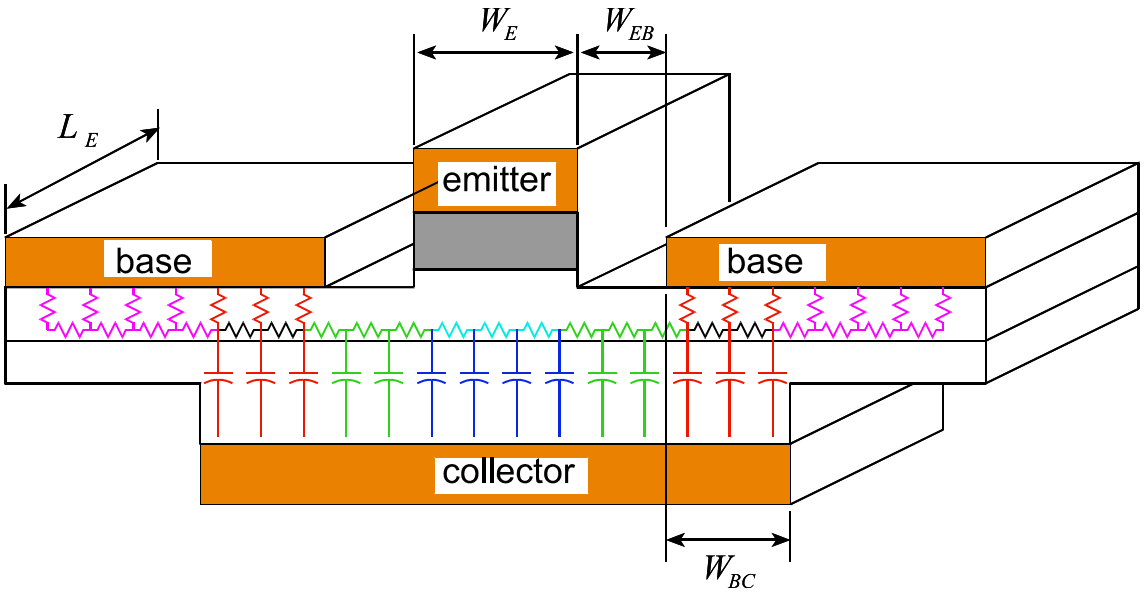
ΔG ΔR ΔC

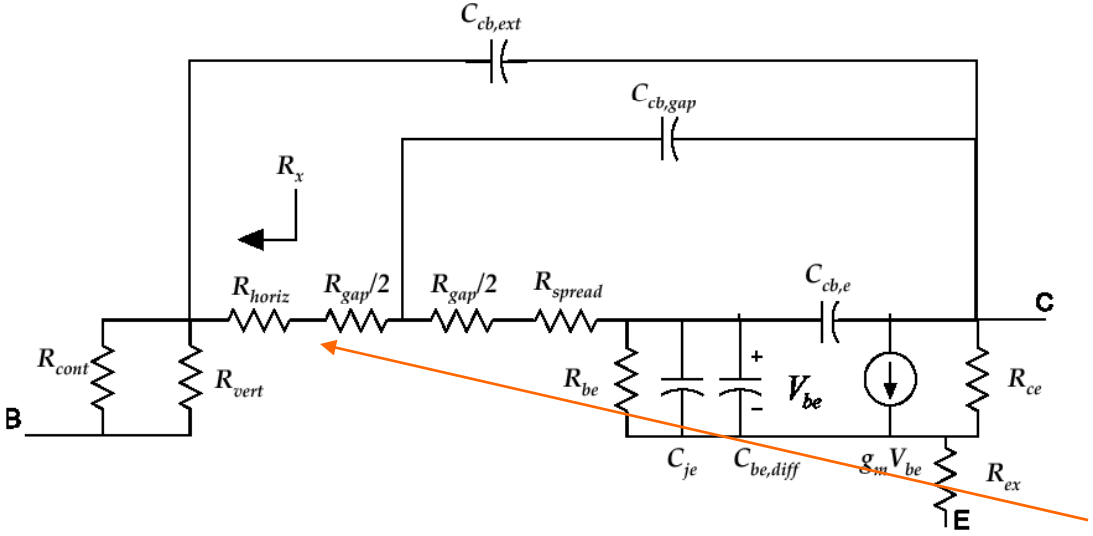
$$\Delta G = L_e \Delta x / \rho_{c;} \qquad \Delta C = \epsilon L_e \Delta x / T_c$$

$$\Delta R = \rho_s \Delta x / L_e$$

This "mesh model" can be entered into a microwave circuit simulator (e.g. Agilent ADS) to predict f_{max} , etc.

Components of Rbb and Ccb





$$R_{horiz} = \rho_s W_{bc} / 2L_E$$

$$R_{cont} = \sqrt{\rho_s \rho_v}/2L_e$$

$$R_{gap} = \rho_s W_{eb}/2L_e$$

$$R_{spread} = \rho_s W_e/12L_e.$$

$$C_{cb,ext} = 2\epsilon L_e W_{cb}/T_c$$

$$C_{cb,gap} = 2\epsilon L_e W_{eb}/T_c$$

$$C_{cb,e} = \varepsilon L_e W_e / T_c$$

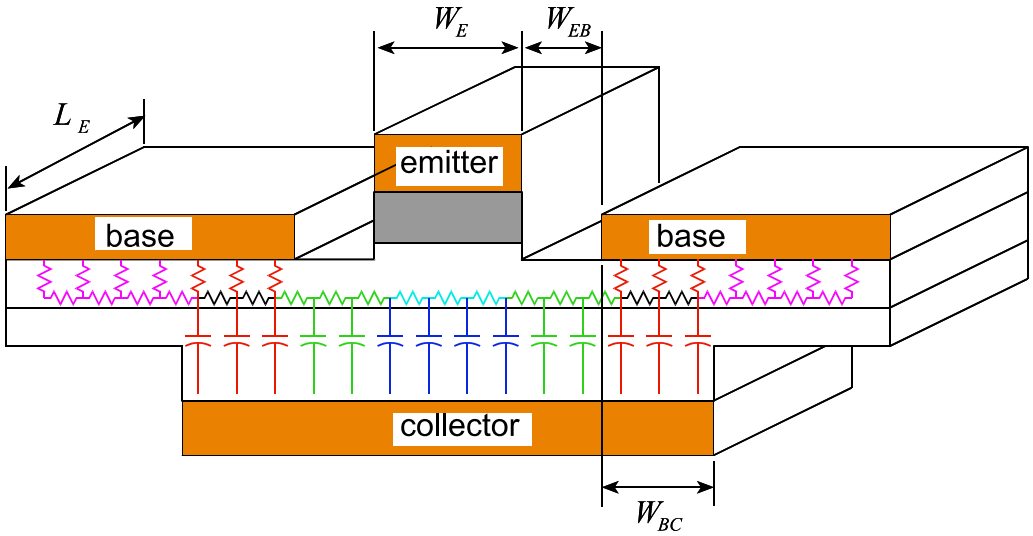
$$R_x = R_{horiz} + R_{vert} \| R_{cont} = R_{cont}!$$

Pulfrey / Vaidyanathan fmax model

$$f_{max} = \sqrt{\frac{f'_\tau}{8\pi\tau_{cb}}},$$

$$\frac{1}{2\pi f'_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}\,(C_{je} + C_{cb}),$$

$$\begin{aligned}\tau_{cb} &= C_{cb,e}\,(R_{cont} + R_{gap} + R_{spread}) \\ &+ C_{cb,gap}\,(R_{cont} + R_{gap}/2) \\ &+ (R_{cont} \| R_{vert})\,C_{cb,ext}\end{aligned}$$



Note that the external capacitance $C_{cb,ext}$ is charged through a relatively low resistance, less than R_{vert}.

$$C_{cb,ext}\left(R_{cont} \| R_{vert}\right) < C_{cb,ext} R_{vert} = \frac{\varepsilon}{T_c}\frac{1}{\rho_{contact}}$$

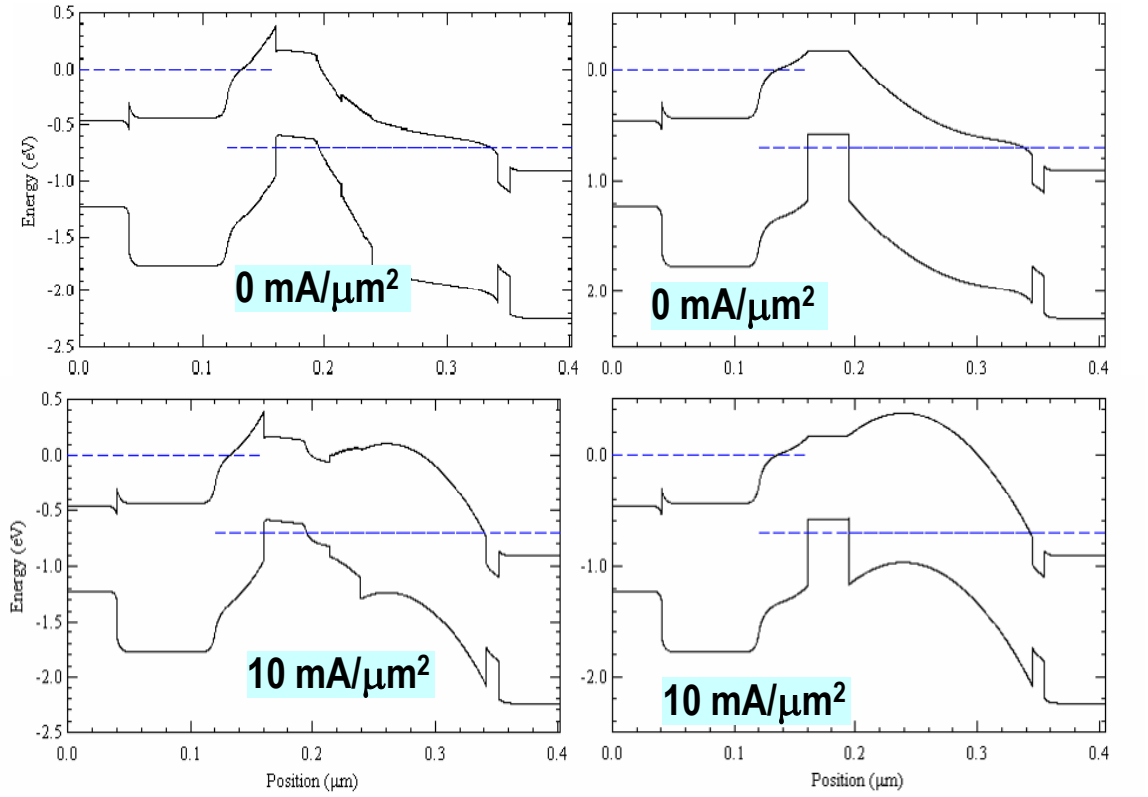
...the associated charging time is relatively small

$C_{cb,ext}$ has moderate effect upon $f_{\max}$, but big impact upon digital and analog speed

collector space-charge effects

Scaling Laws, Collector Current Density, C_{cb} charging time

InGaAs base GaAsSb base



Collector Depletion Layer Collapse

$$V_{cb,\min} + \phi > +(qN_d)(T_c^2 / 2\varepsilon)$$

Collector Field Collapse (Kirk Effect)

$$V_{cb} + \phi > +(J / v_{sat} - qN_d)(T_c^2 / 2\varepsilon)$$

$$\Rightarrow \quad J_{\max} = 2\varepsilon v_{eff}(V_{cb} + V_{cb,\min} + 2\phi) / T_c^2$$

Note that $V_{be} \cong \phi$, hence $(V_{cb} + \phi) \cong V_{ce}$

$$C_{cb}\Delta V_{LOGIC} / I_C = (\varepsilon A_{\text{collector}} / T_c)(\Delta V_{LOGIC} / I_C) = \frac{\Delta V_{LOGIC}}{(V_{CE} + V_{CE,\min})}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2v_{eff}}\right)$$

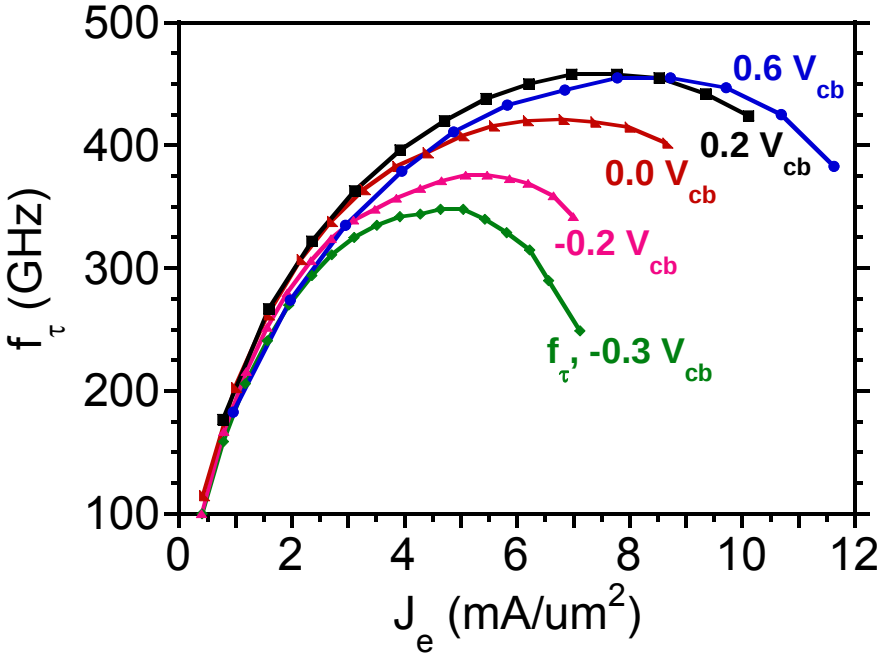
Collector capacitance charging time scales linearly with collector thickness if $J = J_{max}$

Kirk effect in DHBTs

Decrease in f_τ and $f_{\max}$ at high J

Kirk - effect threshold increases with increased V_{ce}

$$J_{\max} = 2\varepsilon v_{sat}(V_{cb} + V_{cb,\min} + 2\phi)/T_c^2$$
$$\cong 2\varepsilon v_{sat}(V_{ce} + V_{ce,\min})/T_c^2$$

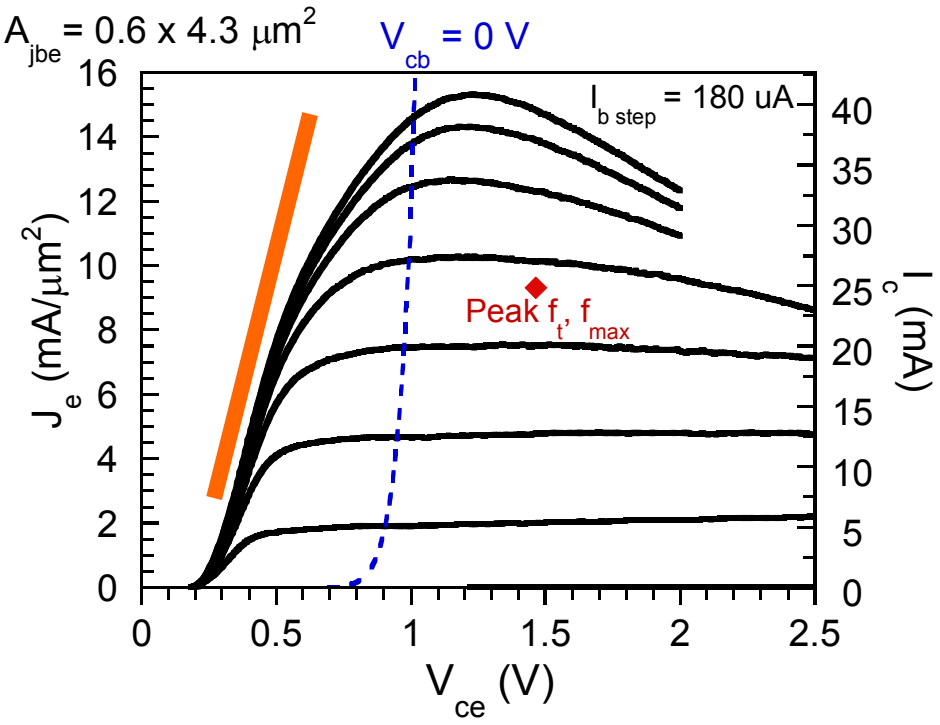


Increase in $V_{ce,sat}$ with increased J

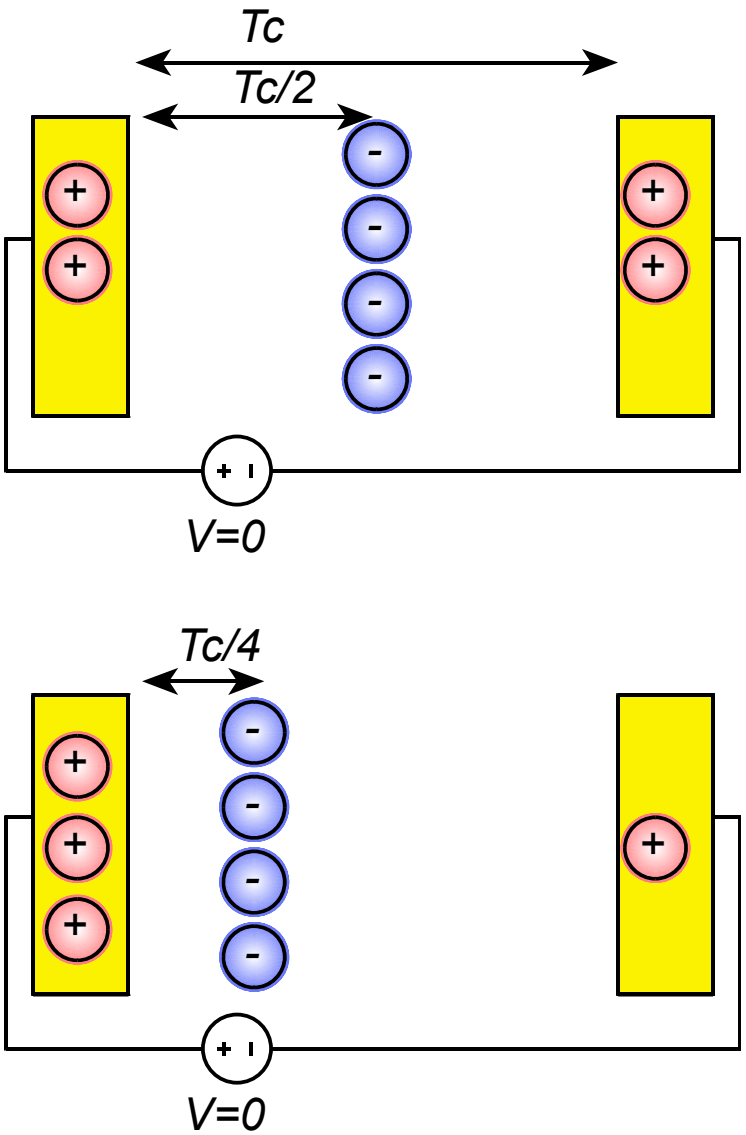
$$\frac{dV_{ce}}{dI_c} = R_{\text{space-charge}} = \frac{T_c^2}{2\varepsilon v_{sat} A_{effective}}$$

where the effective collector current flux area is

$$A_{effective} \approx L_E(W_E + 2T_C)$$



Collector Transit Time

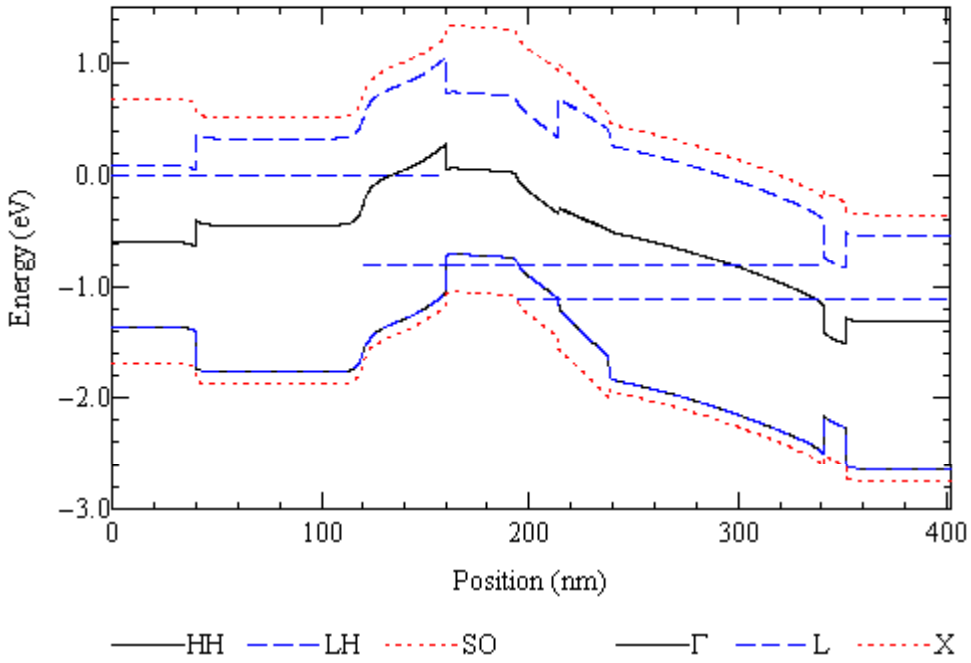


From elementary electrostatics (refer to sketch)

$$\tau_c = \int_0^{T_C} \frac{(1 - x/T_c)}{v(x)}\,dx \equiv \frac{T_c}{2v_{eff}}$$

τ_c is more sensitive to velocity near base.

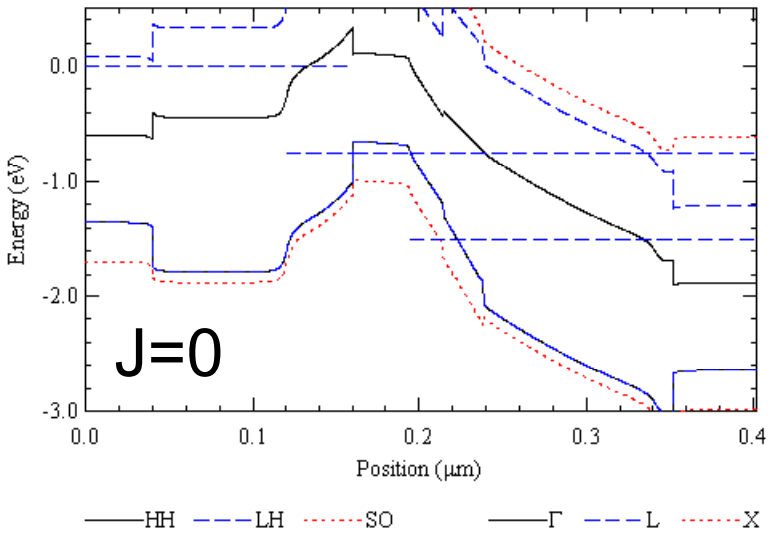
Fortuitous, as initial velocity is high,
then decreases due to Γ - L scattering.

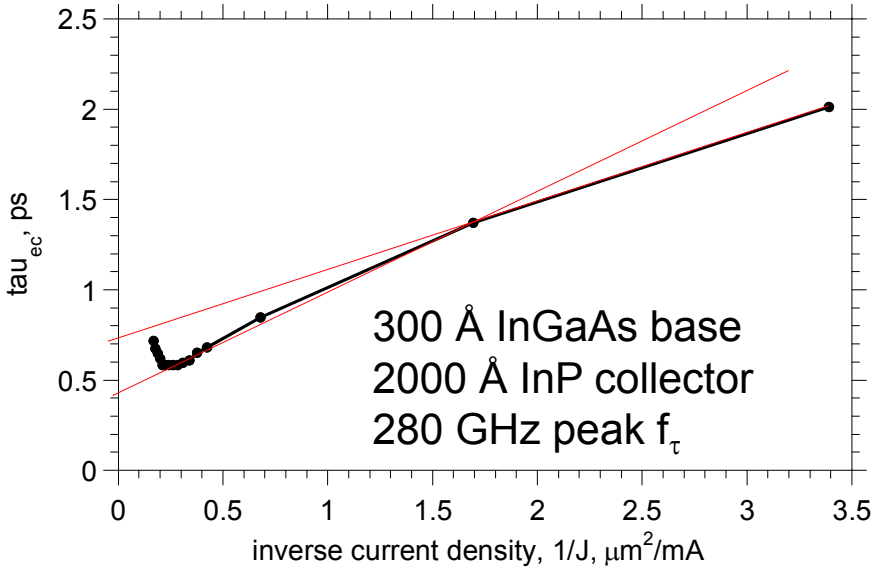


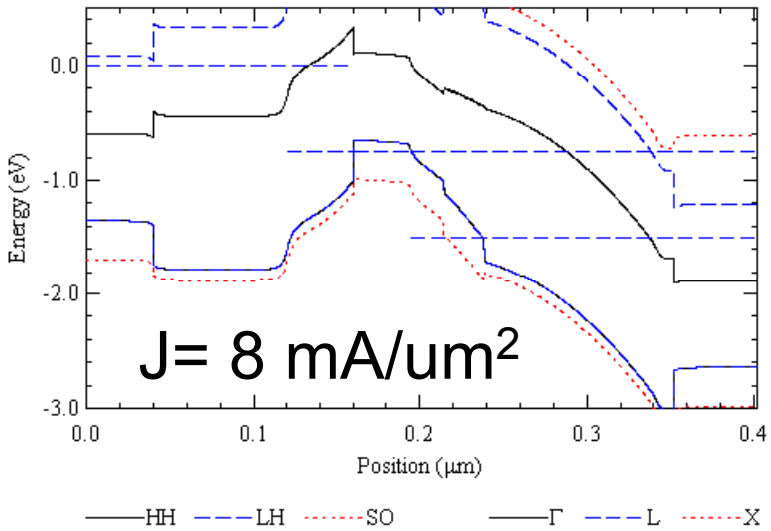
From best fit to RF data, or from Kirk current density vs. collector voltage :

InGaAs : $v_{eff} \approx 3.5 \cdot 10^7$ cm/s for ~ 200 nm layers. InP : $\approx 3.5 \cdot 10^7$ cm/s for ~ 100 - 200 nm layers

Current-induced Collector Velocity Overshoot







Increased current reduces Γ - L scattering,

increases $v(x)$ in early part of collector

⇒ reduced collector transit time

$Q_{base} = I_c \cdot \int_0^{T_C} \frac{(1 - x/T_c)}{v(x)} dx$ is not exactly proportional to I_c

correct definition of collector transit time is

$$\tau_c = \frac{\partial Q_{base}}{\partial I_c} \quad \text{not } \tau_c = \frac{Q_{base}}{I_c}$$

Nakajima, H. "A generalized expression for collector transit time of HBTs taking account of electron velocity modulation," Japanese Journal of Applied Physics, vo. 36, Feb. 1997, pp. 667-668

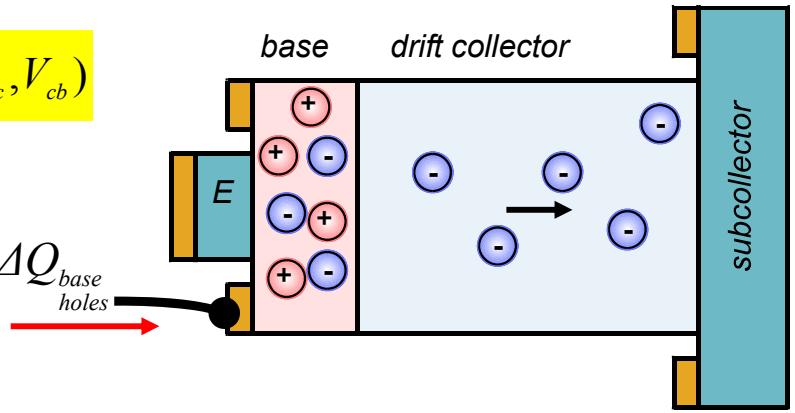
CAUTION : observed nonlinear τ_{ec} variation is also in part due to modulation in emitter ideality factor with bias current ($1/g_m$ often does not vary as $R_{ex} + nkT/qI_E$), and due to variation of C_{je} with bias.

Transit time Modulation Causes C_{cb} Modulation

$$Q_{\substack{base\\holes}} = \text{constant} + Q_{\substack{base\\electrons}} + \int_0^{T_c} qn(x)A(1-x/T_c)dx + V_{bc}\varepsilon A/T_c = f(I_c, V_{cb})$$

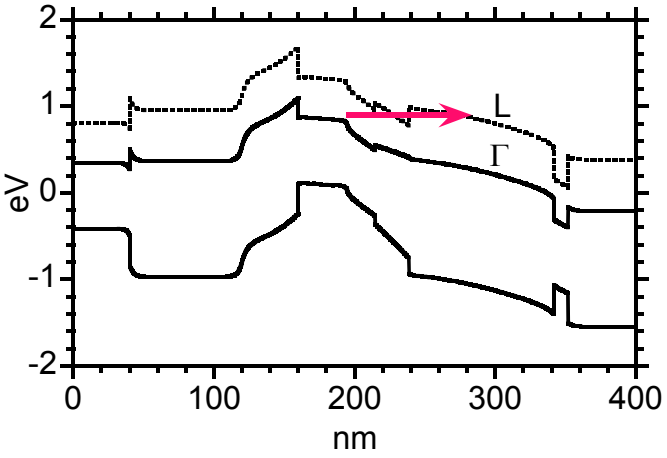
$$C_{cb} \equiv -\frac{\partial Q_{base\,holes}}{\partial V_{cb}} \qquad \tau_f \equiv \frac{\partial Q_{base\,holes}}{\partial I_c} \Rightarrow \frac{\partial C_{cb}}{\partial I_c} = -\frac{\partial \tau_f}{\partial V_{cb}}$$

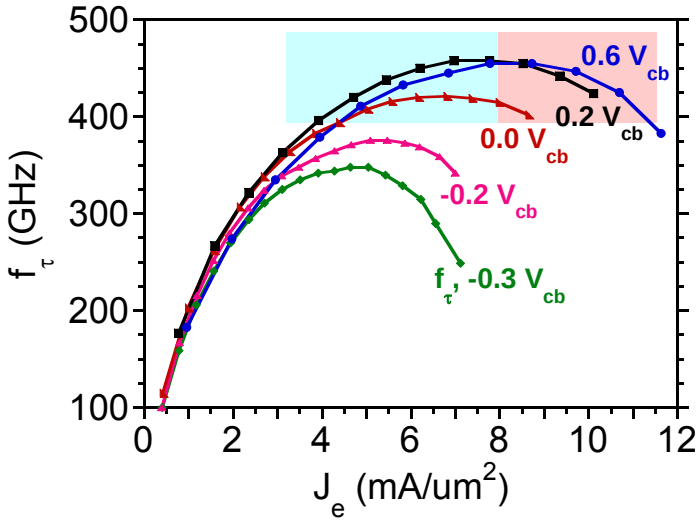
Camnitz and Moll, Betser & Ritter, ***D. Root***

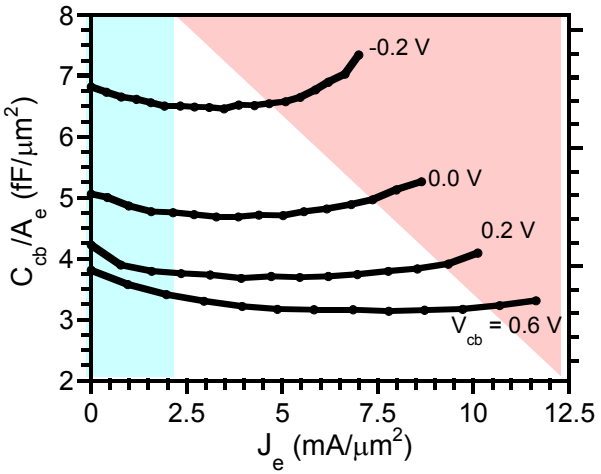


Collector Velocity Modulation :

$$\partial\tau_f/\partial V_{cb} > 0 \Rightarrow \partial C_{cb}/\partial I_c < 0$$







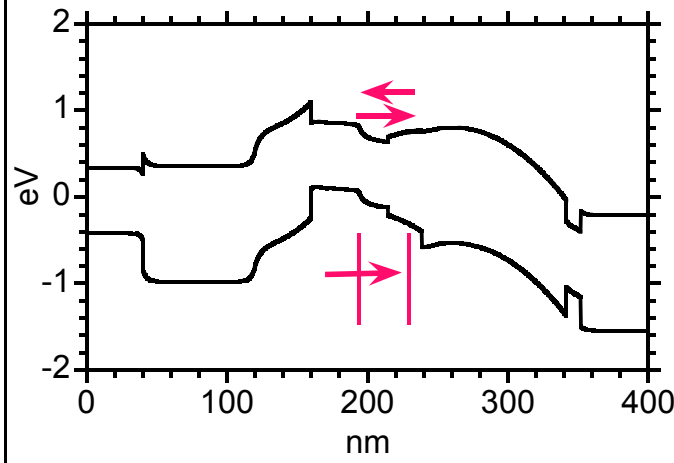
Increase in τ_c with V_{cb} → reduced C_{cb}

- strong effect in InGaAs SHBTs

- weak effect in InP DHBTs

Kirk Effect :

$$\partial\tau_f/\partial V_{cb} < 0 \Rightarrow \partial C_{cb}/\partial I_c > 0$$

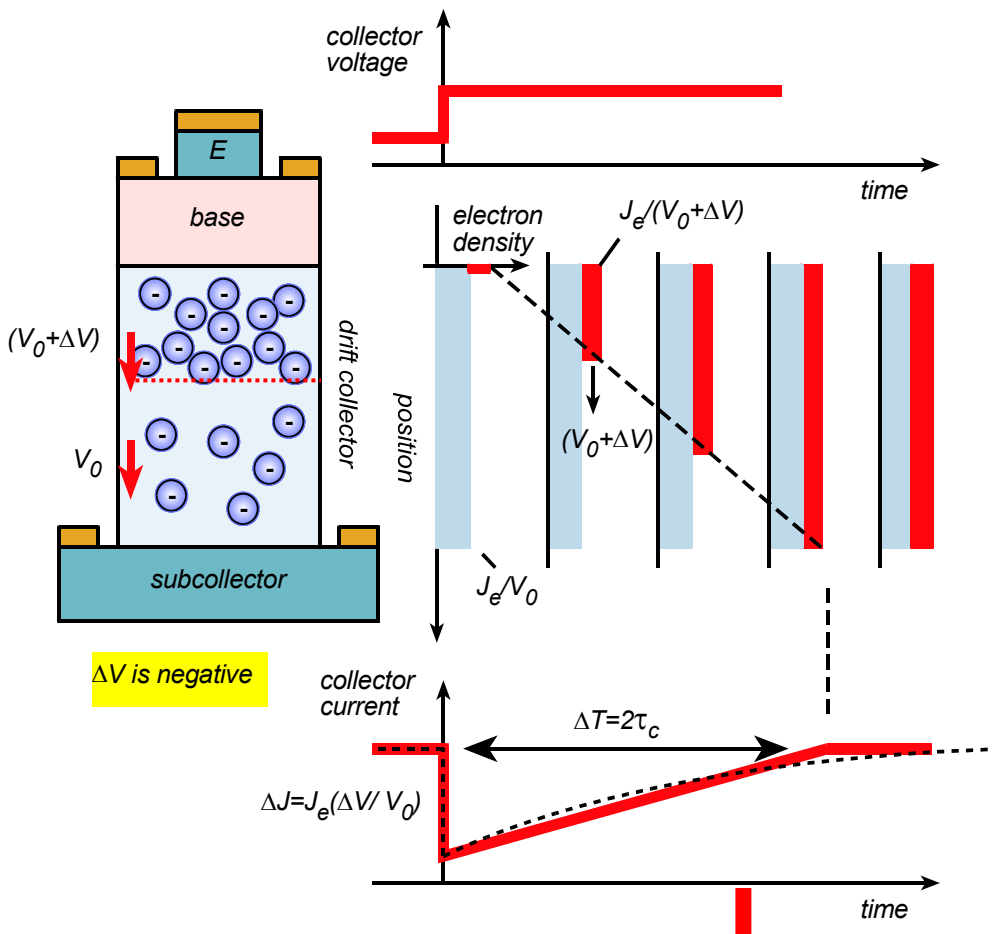


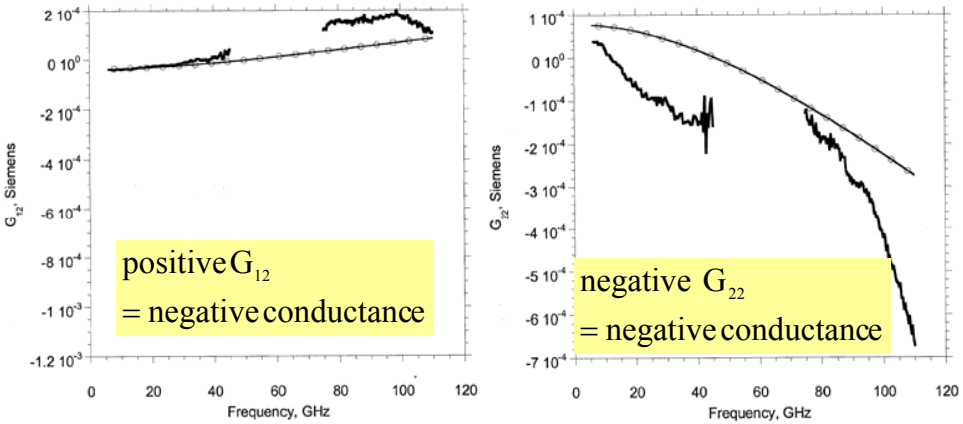
Increase in C_{cb} is due to both

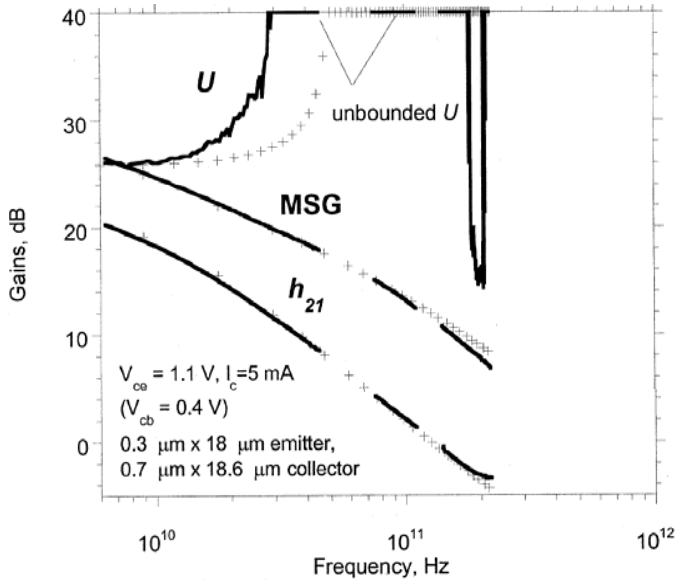
- base pushout into collector

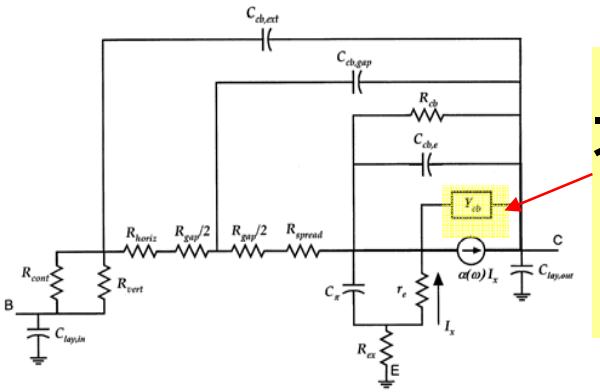
- and modulation of τ_b by V_{cb}

Transit time Modulation → Negative Resistance → Infinite Gain







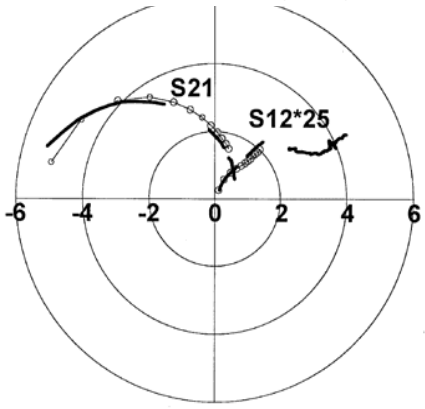


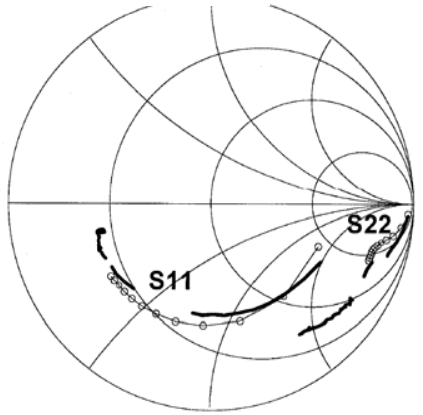
negative capacitance

$$C_{cb,canc} = -I_c\left(\partial\tau_f / \partial V_{cb}\right)$$

negative resistance

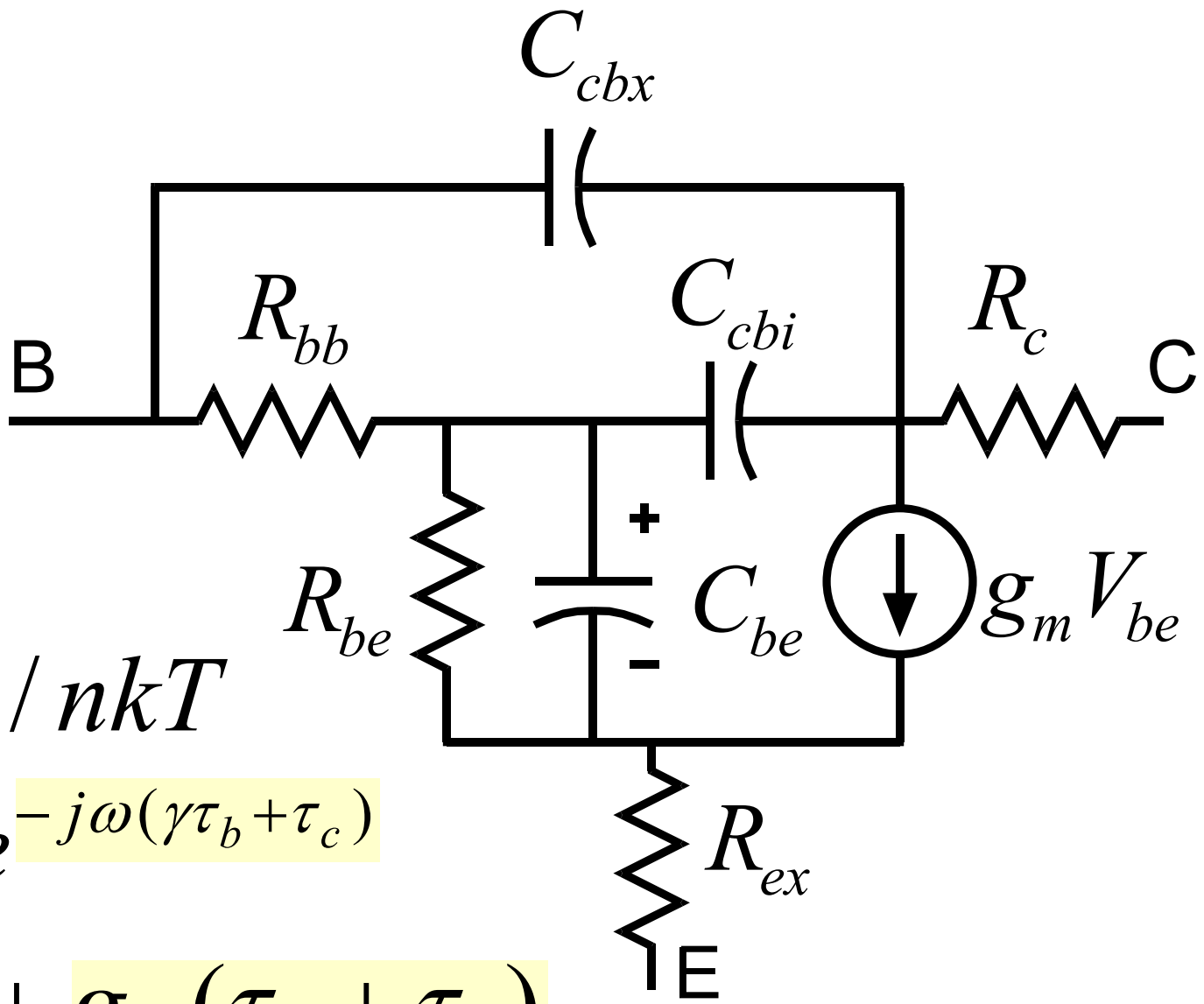
$$R = 2(\tau_c / 3C_{cb,canc})$$





equivalent
circuit
model

Transistor Hybrid-Pi equivalent circuit model



$$g_{m0} = qI_E / nkT$$

$$g_m = g_{m0} e^{-j\omega(\gamma\tau_b + \tau_c)}$$

$$C_{be} = C_{je} + g_m(\tau_b + \tau_c)$$

Comments regarding the Hybrid-Pi model

The common - base (T) model directly models
frequency - dependent transport

The hybrid - pi model results from a fit to the T to first order in ω.

The capacitance $C_{be,diff}$ models the effect of $(\tau_b + \tau_c)$
on input impedance

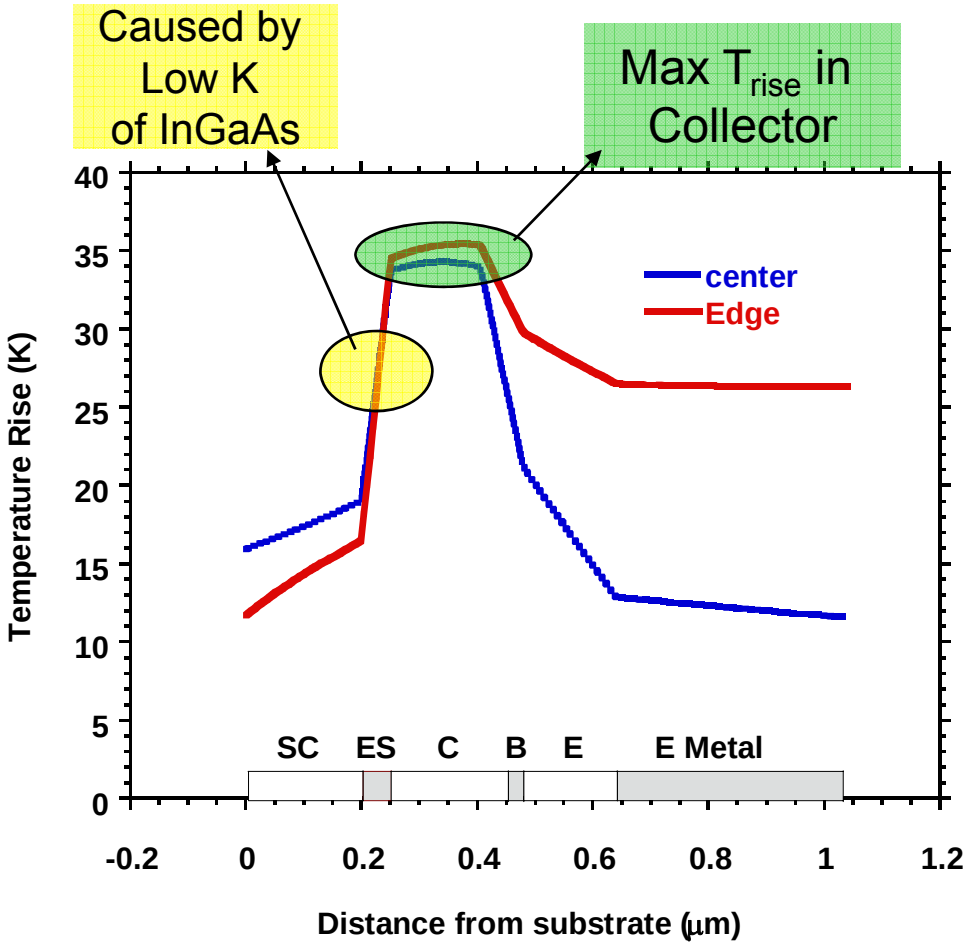
The g_m generator nevertheless also requires
an associated $\sim (0.2 \cdot \tau_b + \tau_c)$ delay (important in fast IC design)

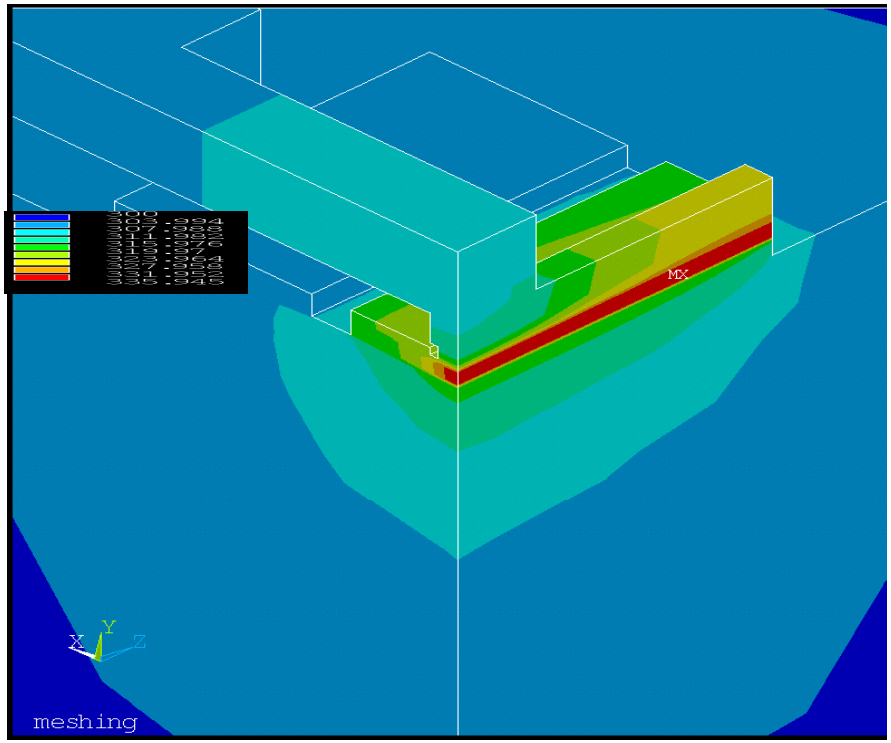
$R_{bb}C_{cbi}$ and C_{cbx} represent fits
to the distributed RC base - collector network

thermal considerations

Fast DHBTs: high current density → high temperature

Ian Harrison
U. Nottingham





- Thermal conductivity of InGaAs ~ ***5 W/mK***
- Thermal conductivity of InP ~ ***68 W/mK***

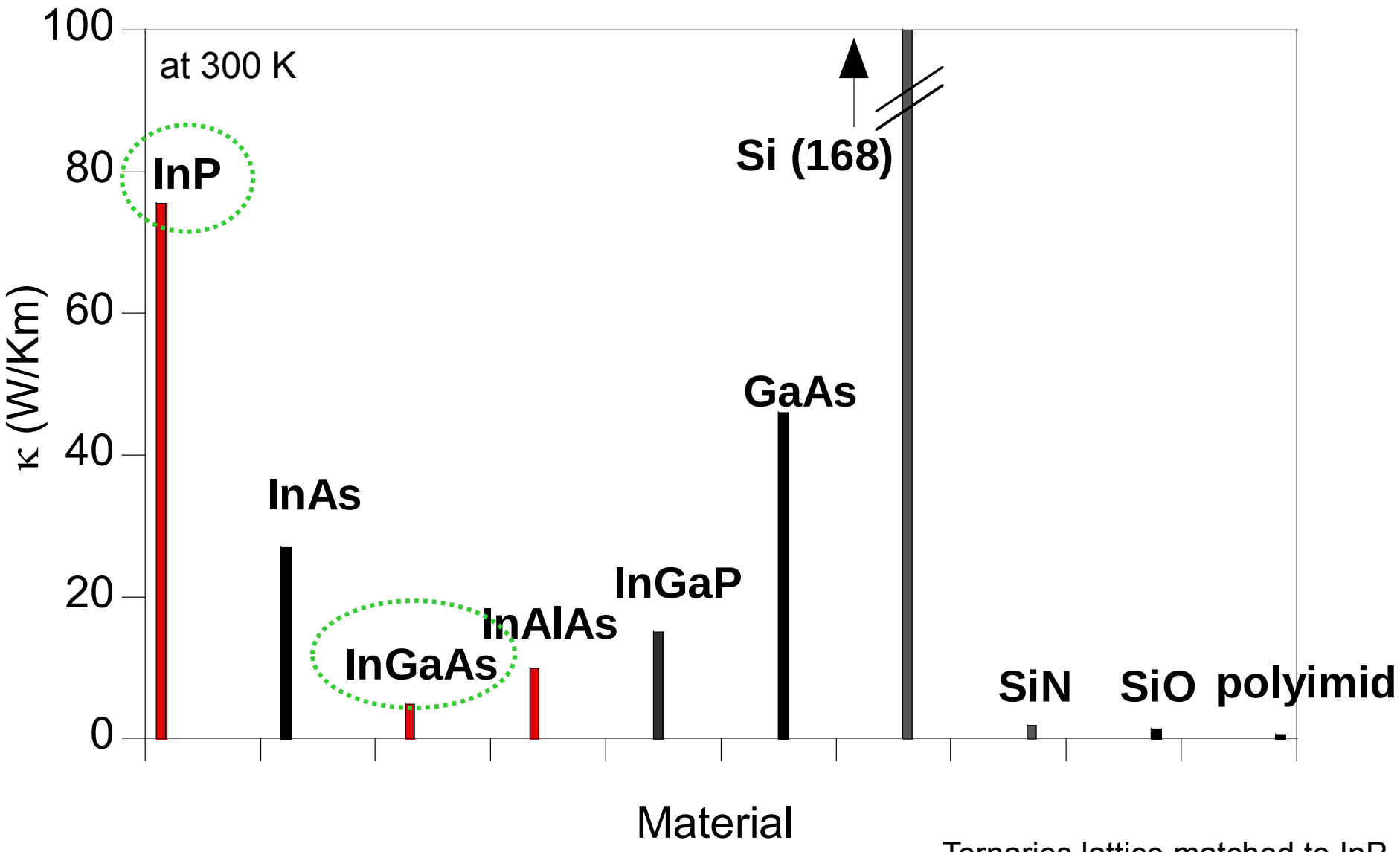
- Average Tj (Base-Emitter) =26.20°C
- Measured Tj=26°C—good agreement

Conclusions…

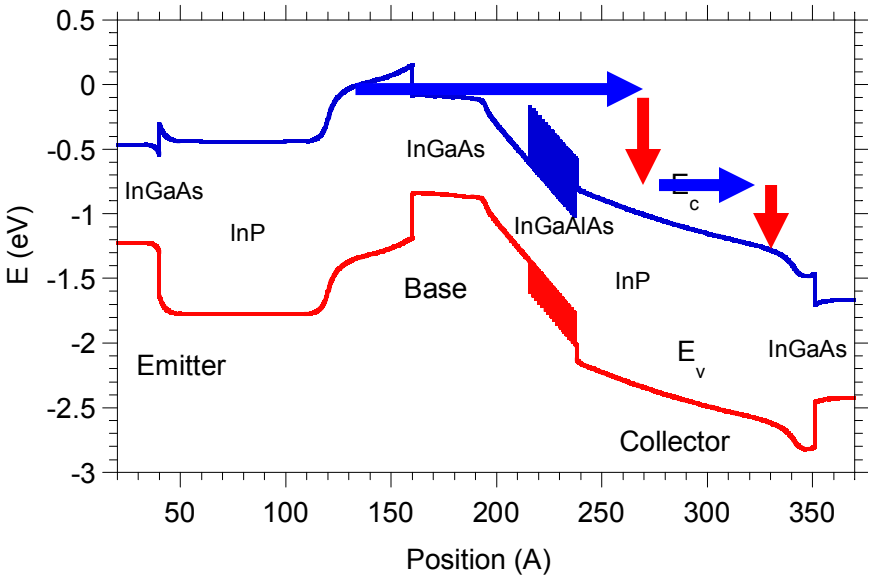
Minimize InGaAs thickness in subcollector
Use narrow emitter stripes

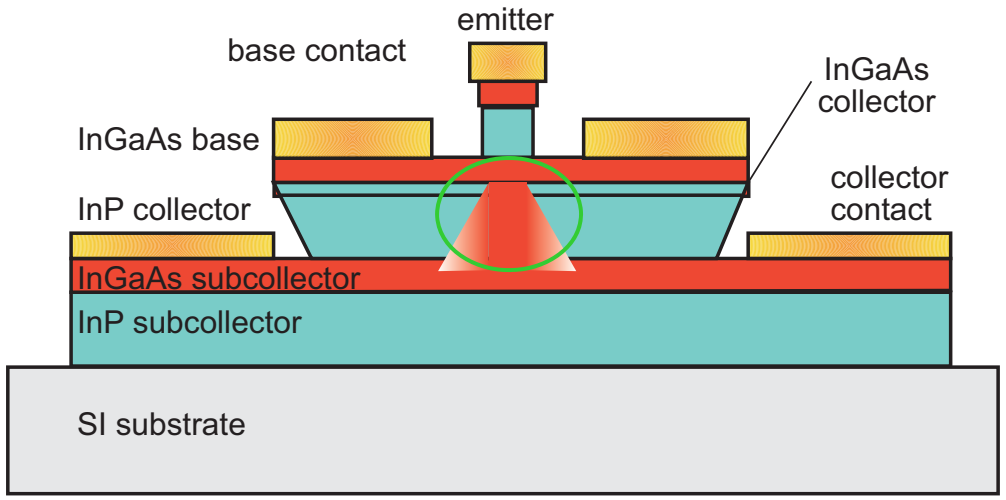
Mattias Dahlström

Thermal conductivity of common materials

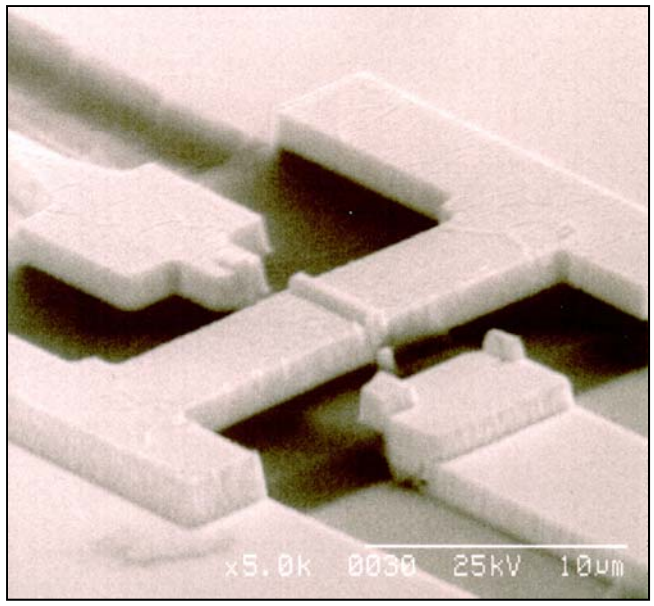


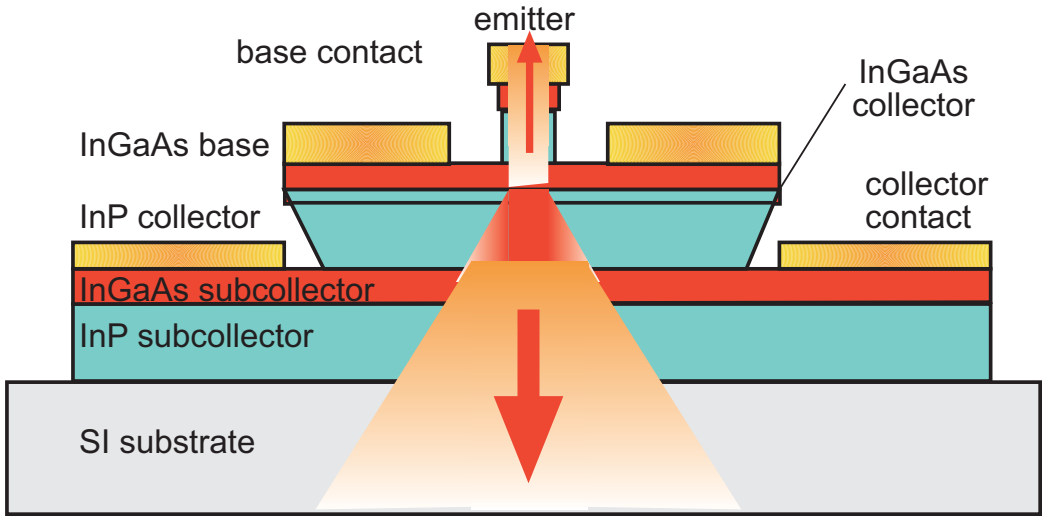
Where is the heat generated, how is it removed ?





$J_E \times V_{CE} = 6 \times 1.5\ V = 9\ mW/\mu m^2$ *In the intrinsic collector*





Main heat transport is through the subcollector to the substrate
Up to 30 % heat transport up through the emitter contact

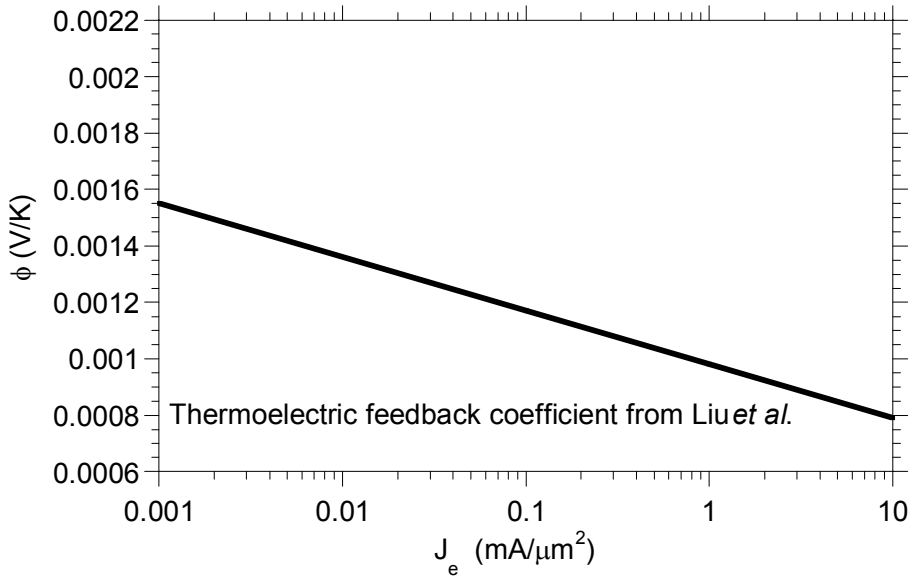
For small thermal resistance: InP collector, InP subcollector, only thin InGaAs in subcollector, InP emitter, narrow emitter junction for radial heat flow

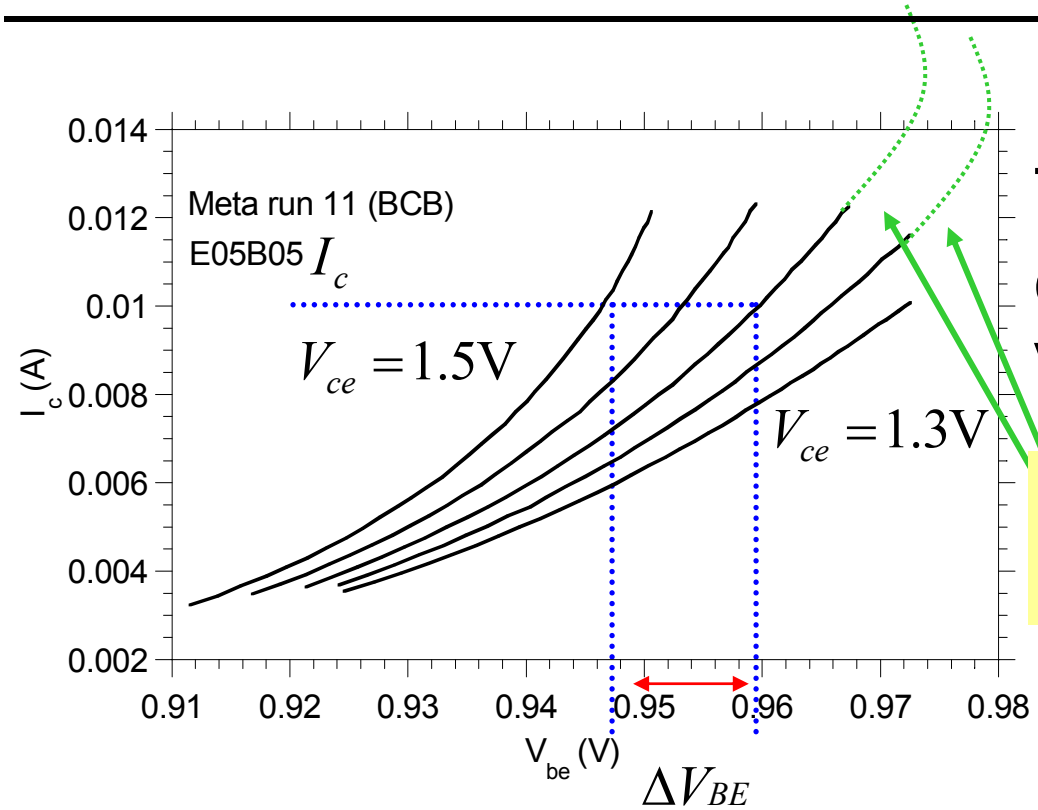
Experimental Measurement of Temperature Rise

$$\delta V_{be}\Big|_{\text{fixed } I_c} = \frac{dV_{be}}{dT}\frac{dT}{dP}\frac{dP}{dV_{CE}}\delta V_{CE}$$

$$= -\phi \cdot \theta_{JA} I_C \delta V_{CE}$$

$$\Rightarrow \theta_{JA} = \left.\frac{dV_{be}}{dV_{CE}}\right|_{\text{fixed } I_c} \times \frac{1}{I_C(\phi)}$$



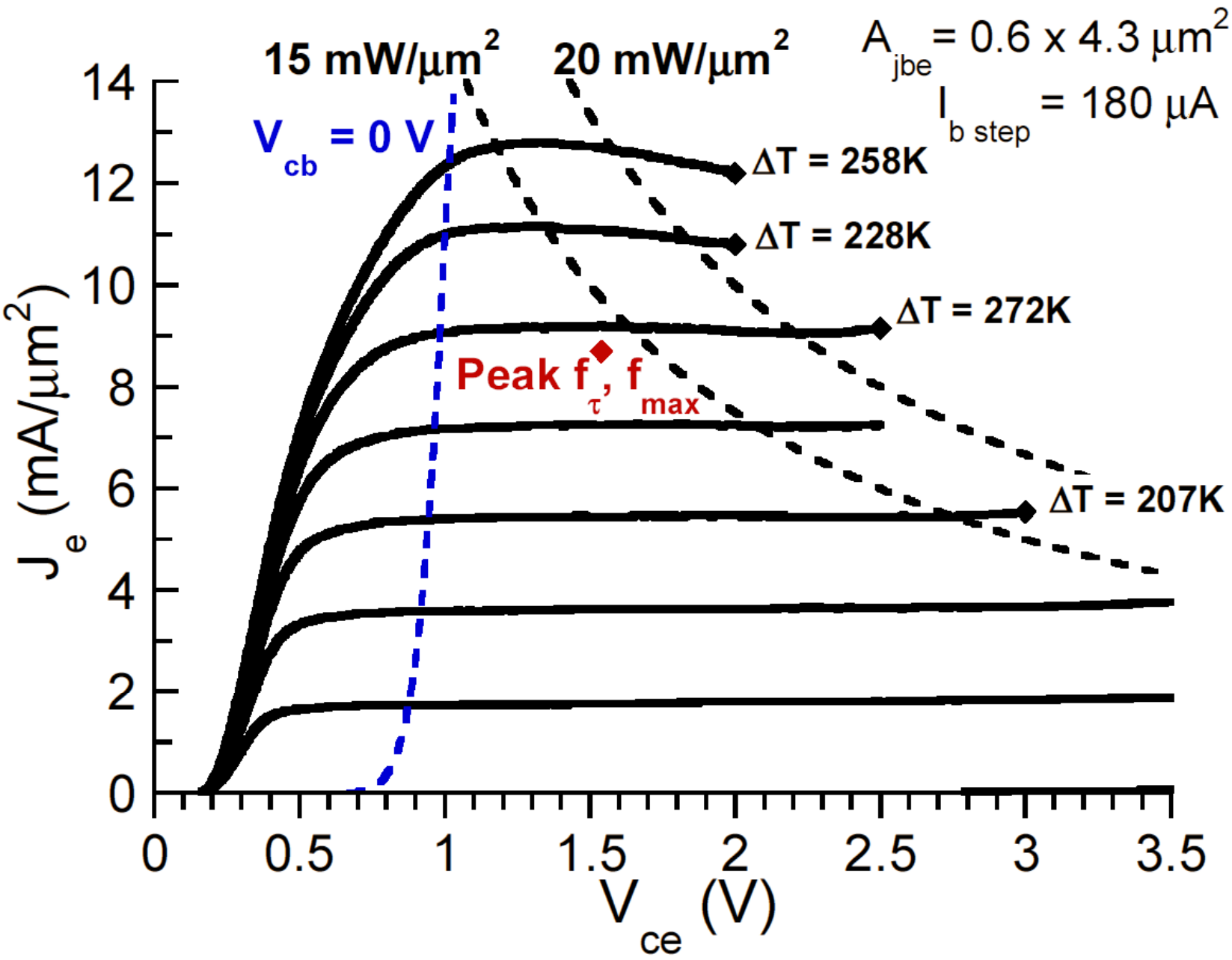


Temperature rise calculated by measuring I_C, V_{CE} and ΔV_{BE}

No thermal instability as long as slope<∞
each V_{BE} gives a unique I_C

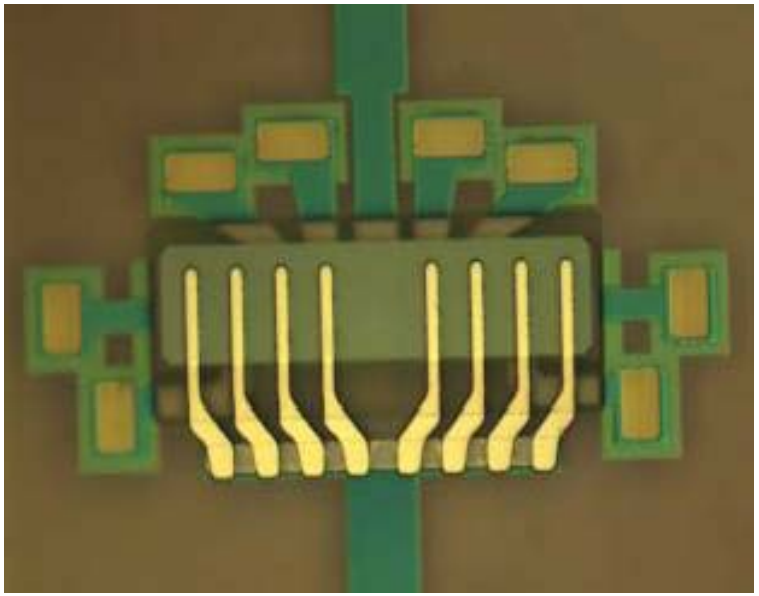
W. Liu: “Thermal Coupling in 2-Finger Heterojunction Bipolar Transistors”
, IEEE Transactions on Electron Devices, Vol 42 No6, June 1995
W. Liu: H-F. Chau, E. Beam, "Thermal properties and Thermal Instabilities of InP-Based Heterojunction Bipolar Transistors”, IEEE Transactions on Electron Devices, Vol 43 No3, March 1996

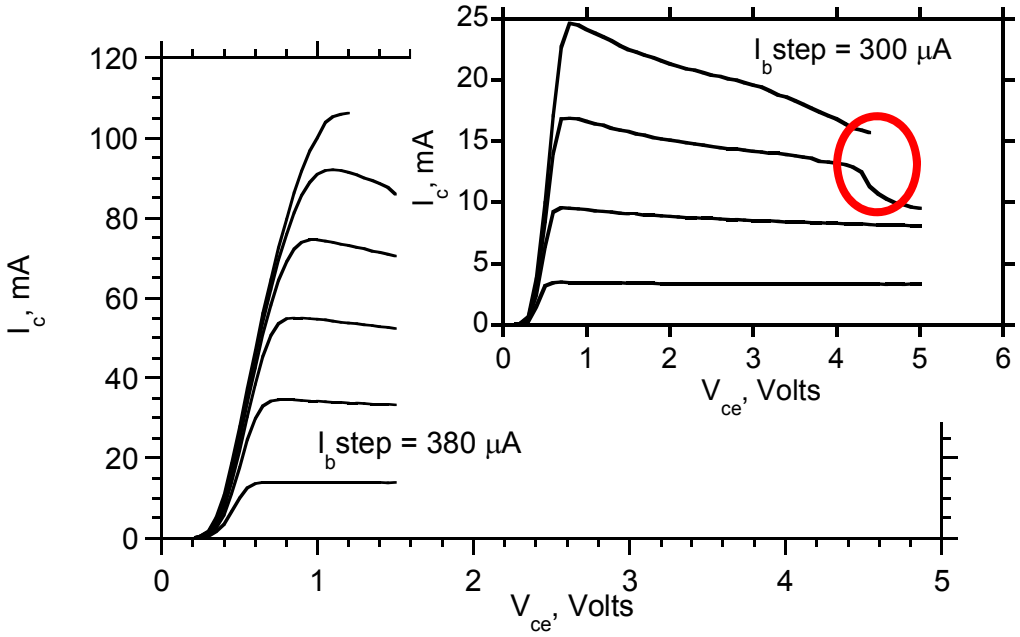
Example of Thermal Data



Current Hogging and Emitter Finger Ballasting

Yun Wei





Assume initial temperature difference δT between 2 fingers

$$\frac{dV_{be}}{dT} = -\phi \text{ at constant } I_c$$

$$\delta T \Rightarrow \delta V_{be} = \frac{dV_{be}}{dT}\delta T \Rightarrow \delta I_C = \frac{1}{R_{ex} + R_{ballast} + kT/qI_E}\delta V_{be}$$

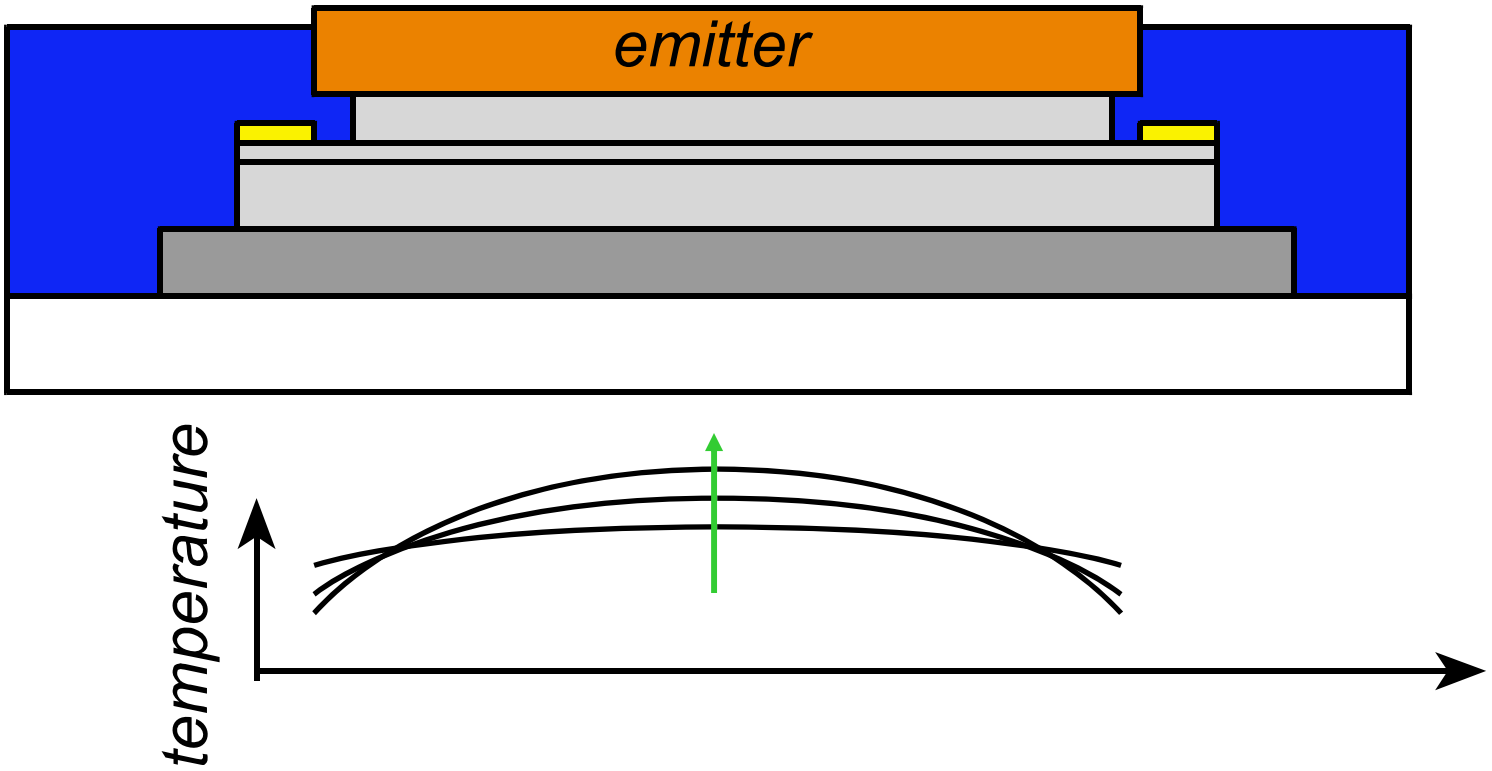
$$\Rightarrow \delta P = V_{CE}\delta I_C \Rightarrow \delta T = \theta_{JA}\delta P$$

Unstable unless

$$K_{\text{thermal stability}} = \left|\frac{dV_{be}}{dT}\right| \frac{V_{CE}\theta_{JA}}{R_{ex} + R_{ballast} + kT/qI_E} < 1$$

W. Liu, H-F Chau, E. Beam III, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors", IEEE Transactions on Electron Devices, vol.43, (no.3), IEEE, March 1996. p.388-95.

Thermal runaway within a finger

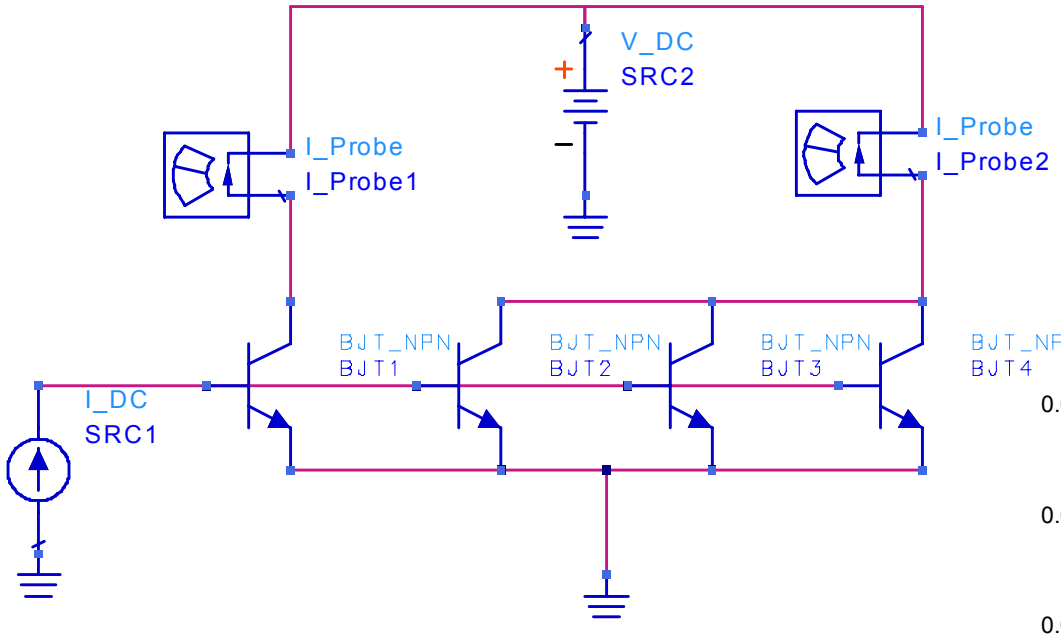


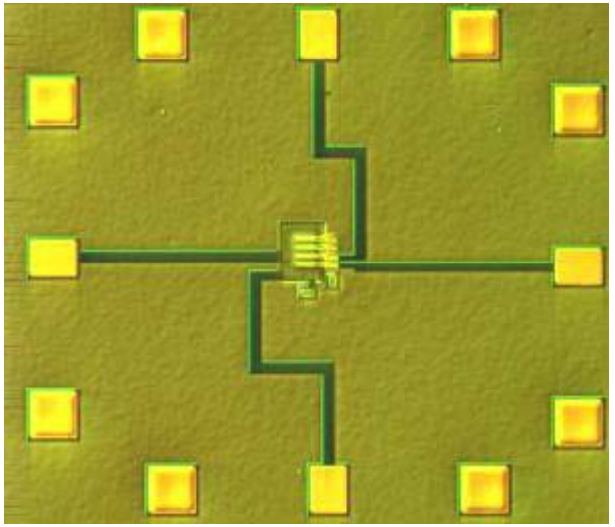
With long emitter finger, current-crowding can occur within finger

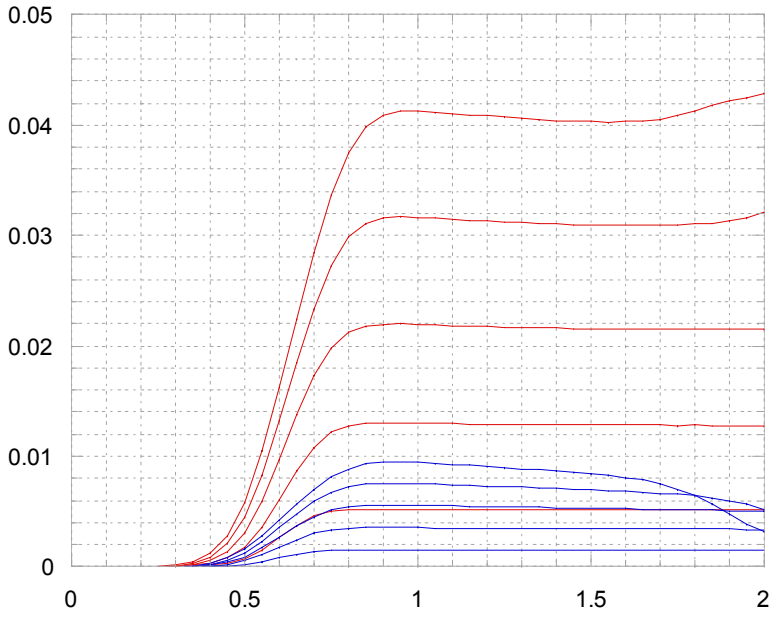
- Long finger: temperature can vary along length of emitter finger
  loss of strong thermal coupling
- Temperature gradients along finger results in nonuniform current distribution
  center of stripe gets hotter → carries more current → gets hotter → …
  Premature Kirk-effect-induced collapse in f_t.

Yun Wei

Measurement of Current hogging in multi-finger DHBT







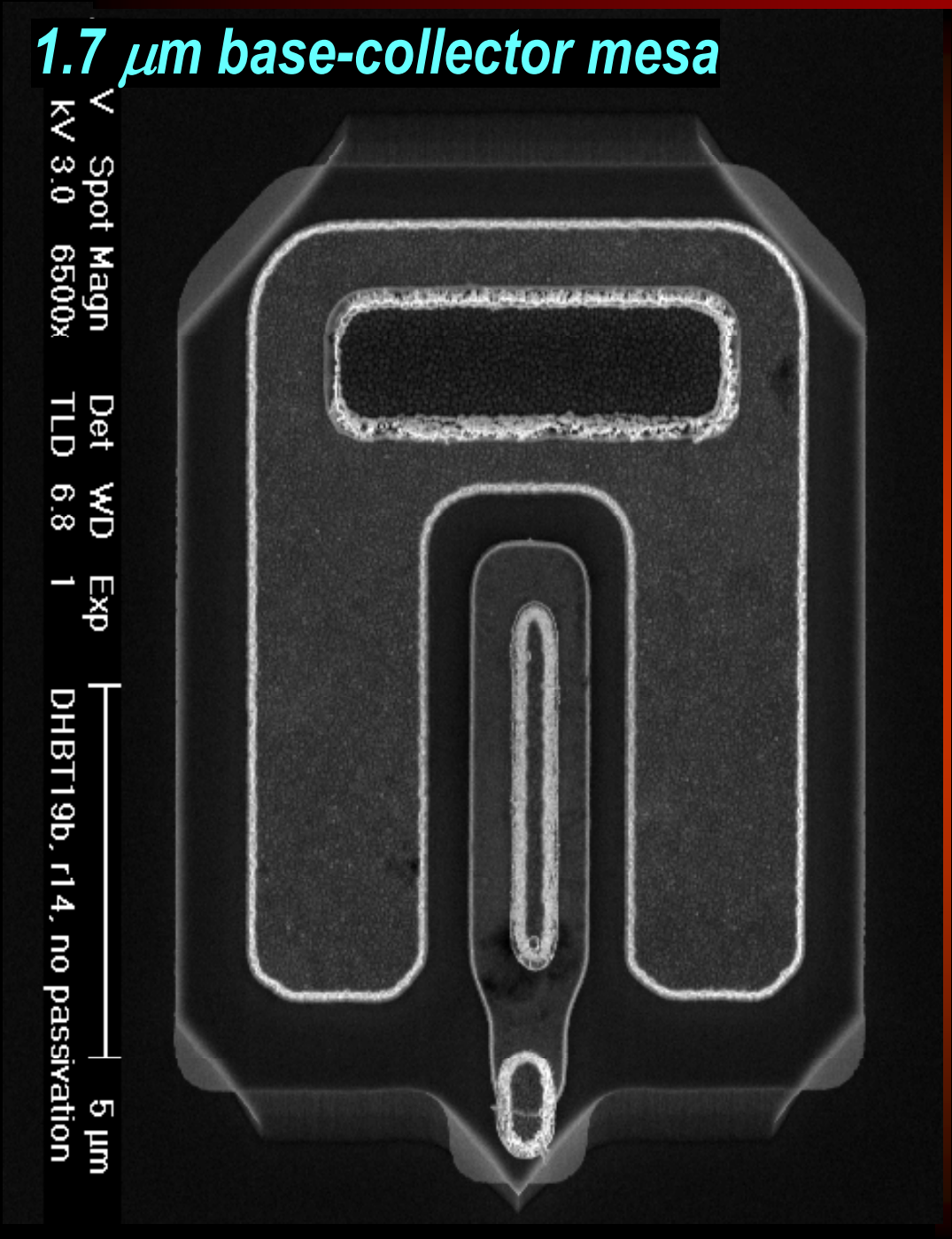
W. Liu, H-F Chau, E. Beam III, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors", IEEE Transactions on Electron Devices, vol.43, (no.3), IEEE, March 1996. p.388-95.

mesa transistor results

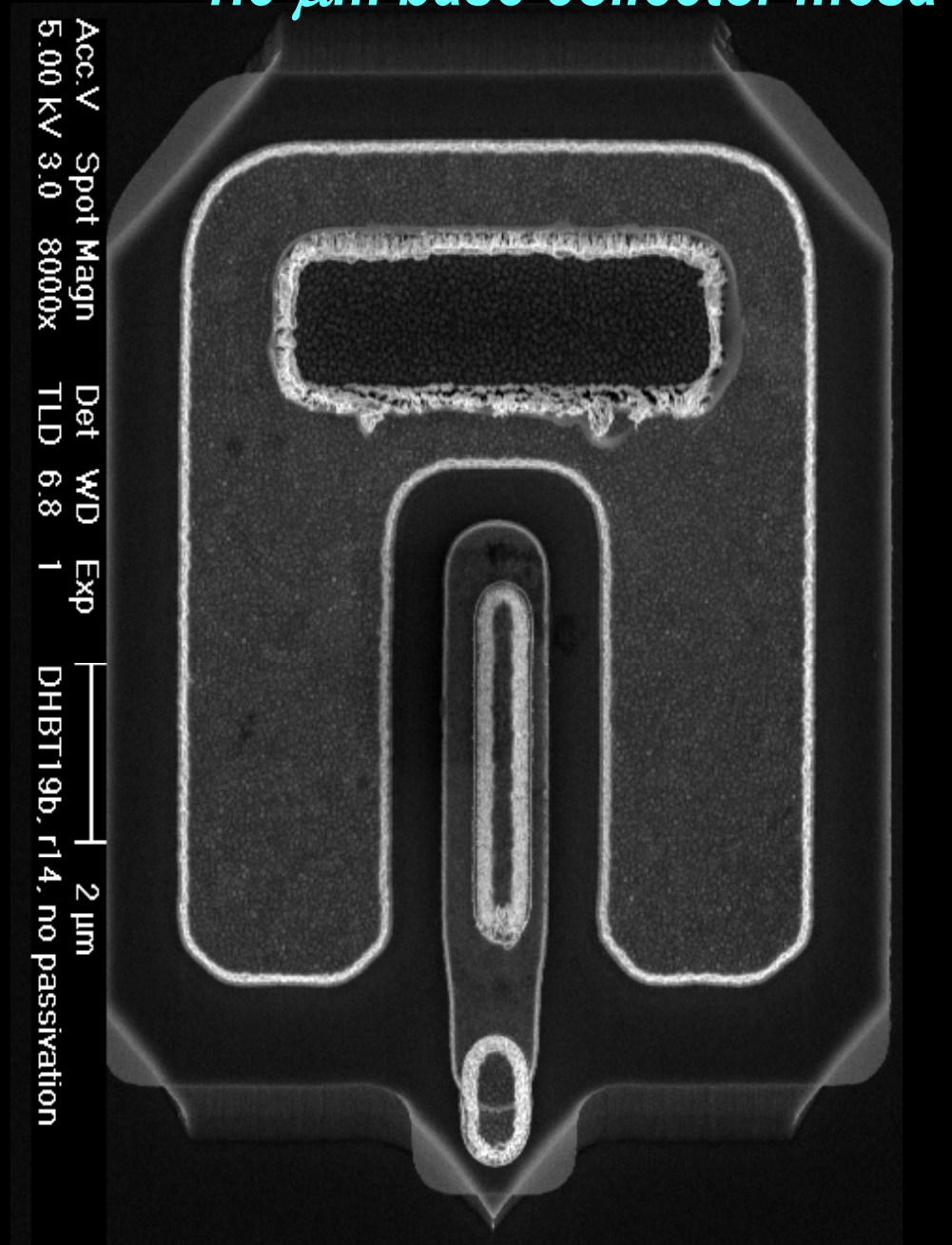
Zach Griffith

InP Mesa DHBTs; 600 nm Emitter Scaling Generation

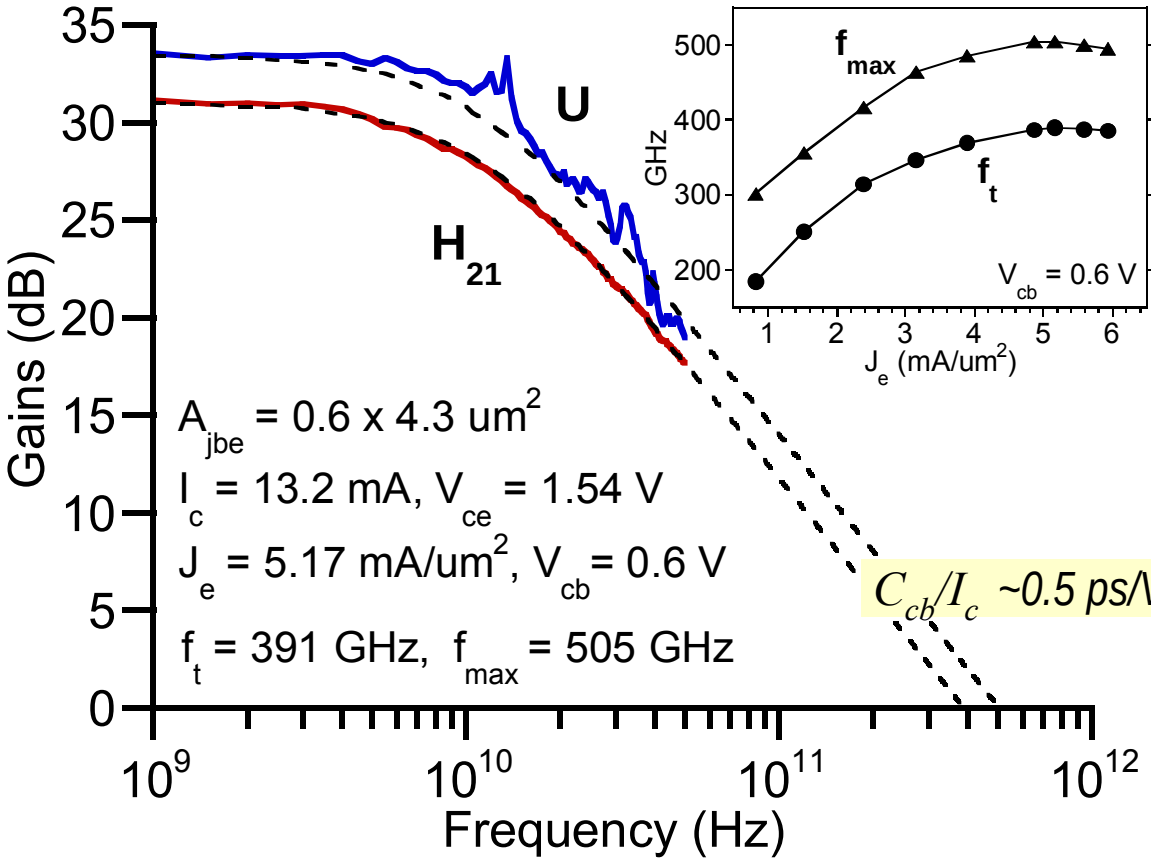
1.7 μm base-collector mesa



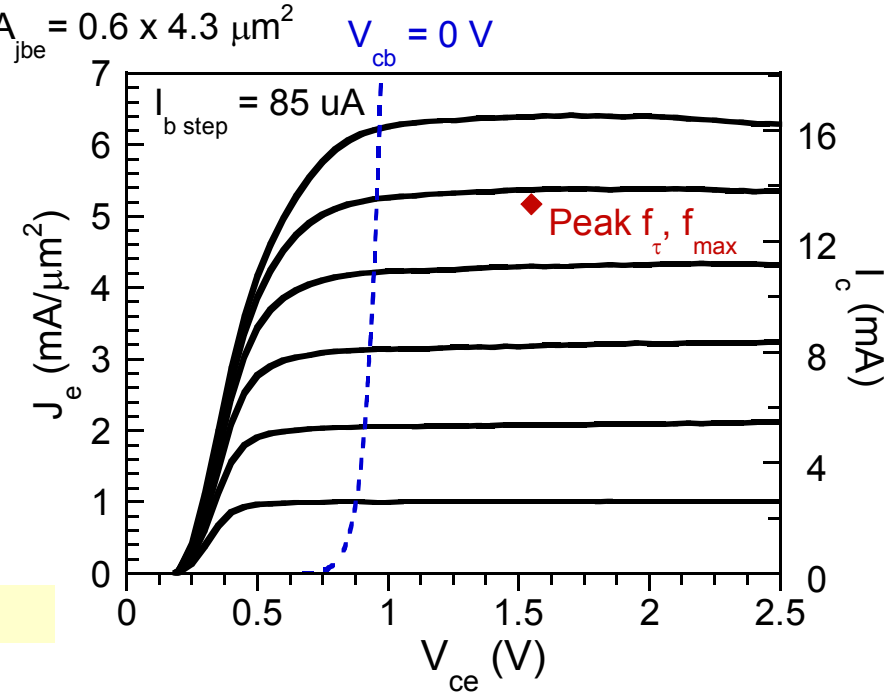
1.3 μm base-collector mesa

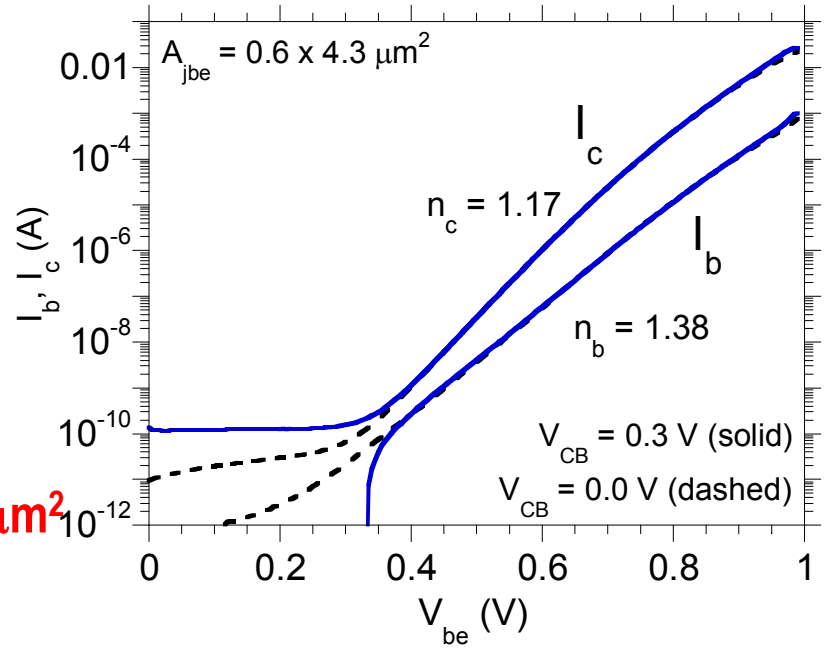


DC, RF performance—150 nm collector, 47 nm transition



C_{cb}/I_c ~0.5 ps/V





Average $\beta \approx 36$, $V_{BR,CEO}$ = 5.1 V (I_c = 50 μA)

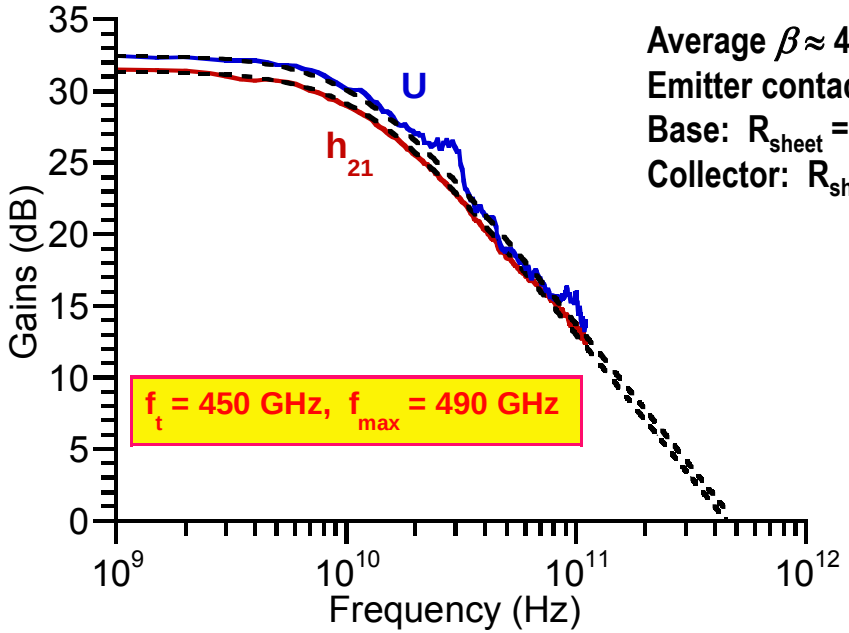
Emitter contact (from RF extraction), R_{cont} = 10.1 Ω·μm²

Base (from TLM) : R_{sheet} = 564 Ω/sq, R_{cont} = 9.6 Ω·μm²

Collector (from TLM) : R_{sheet} = 11.9 Ω/sq, R_{cont} = 5.4 Ω·μm²

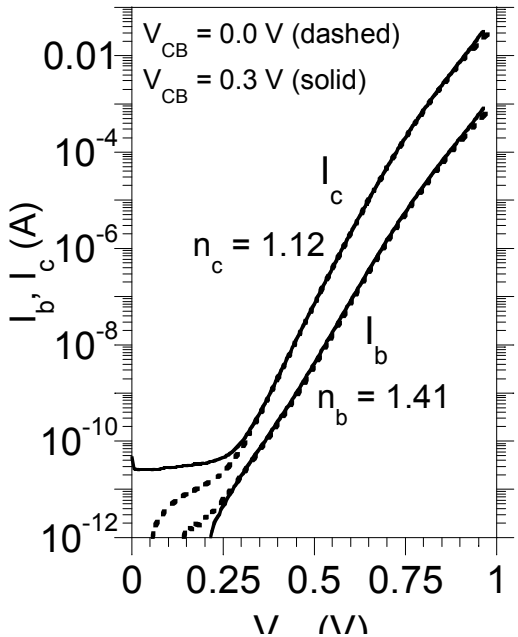
DC, RF performance—120 nm collector, 42 nm transition

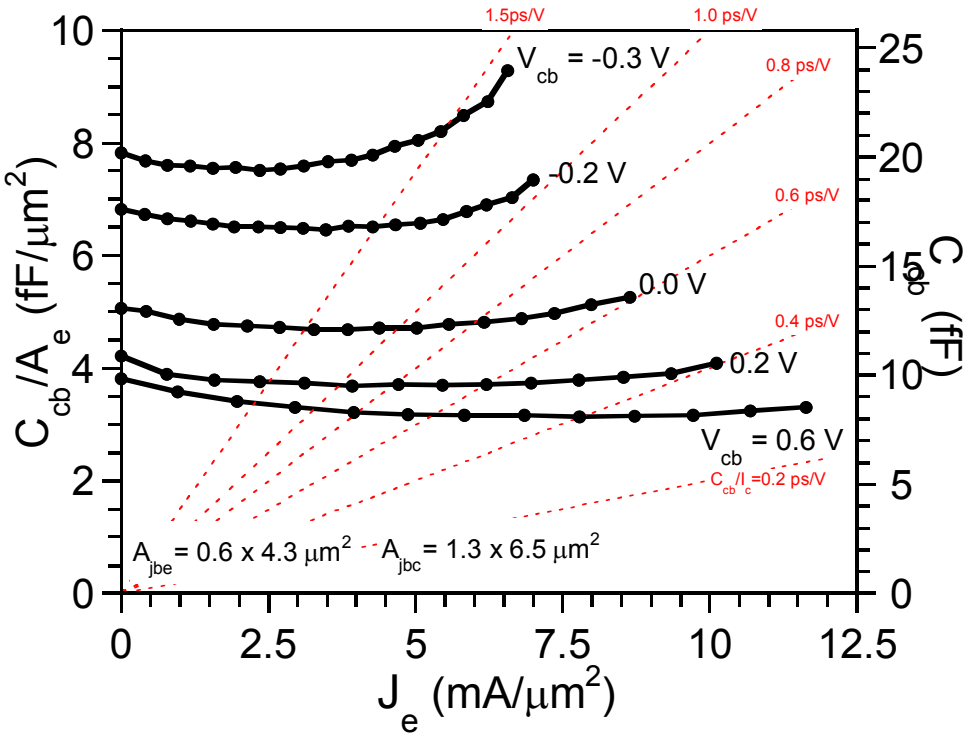
30 nm base

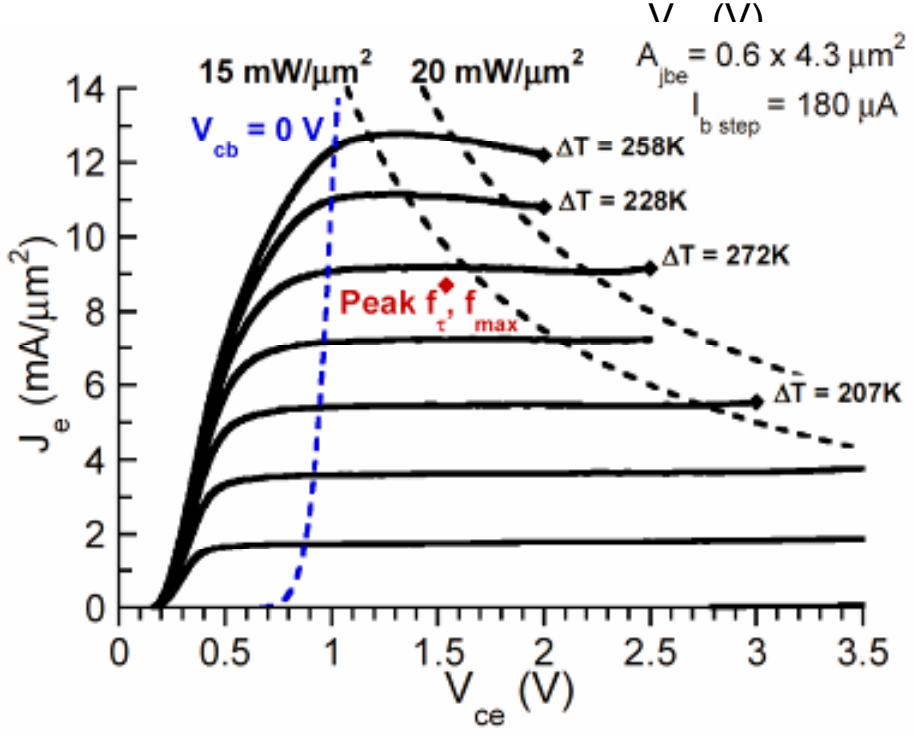


Average $\beta \approx 40$, $V_{BR,CEO}$ = 3.9 V.
Emitter contact $R_{cont} < 10\ \Omega\cdot\mu m^2$
Base: R_{sheet} = 610 Ω/sq, $R_{cont} = 4.6\ \Omega\cdot\mu m^2$
Collector: R_{sheet} = 12.1 Ω/sq, $R_{cont} = 8.4\ \Omega\cdot\mu m^2$

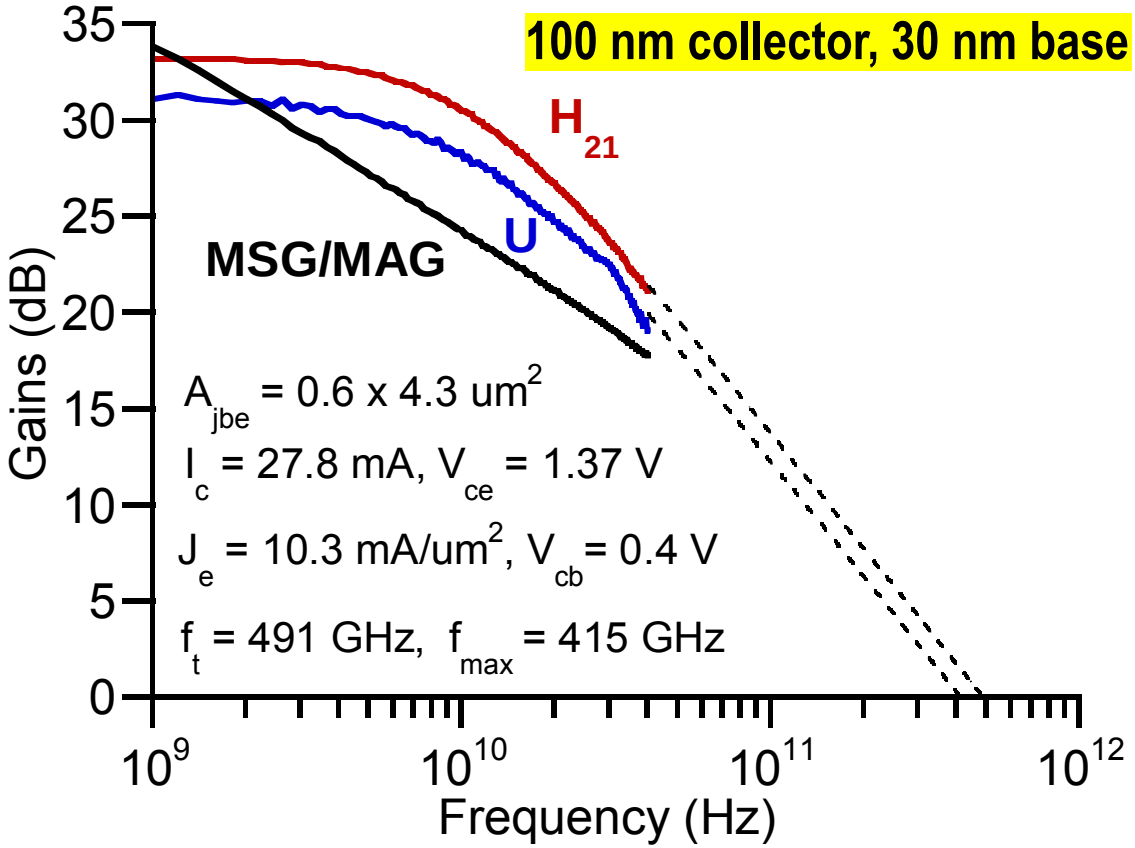
Gummel characteristics

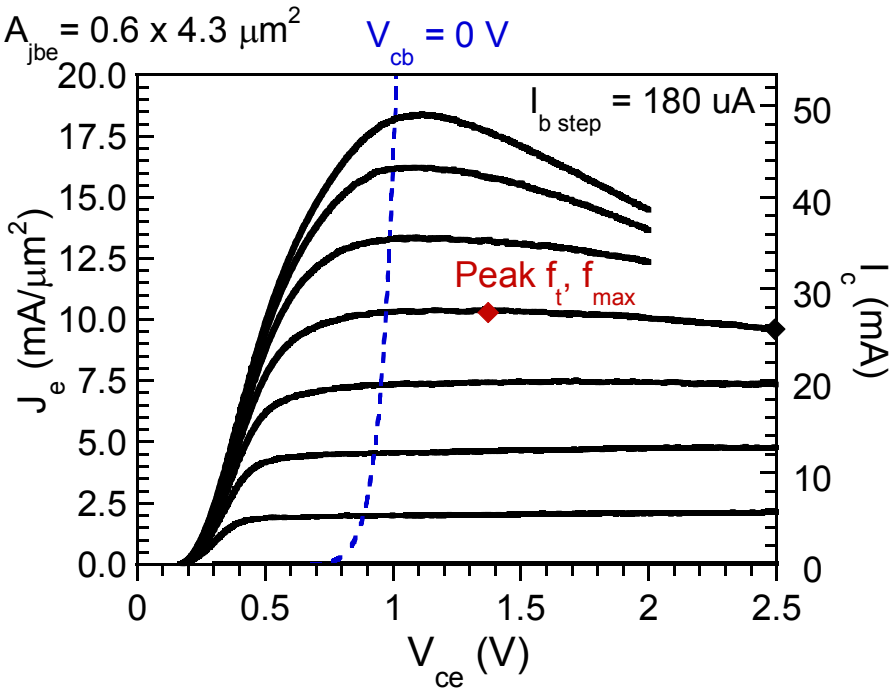


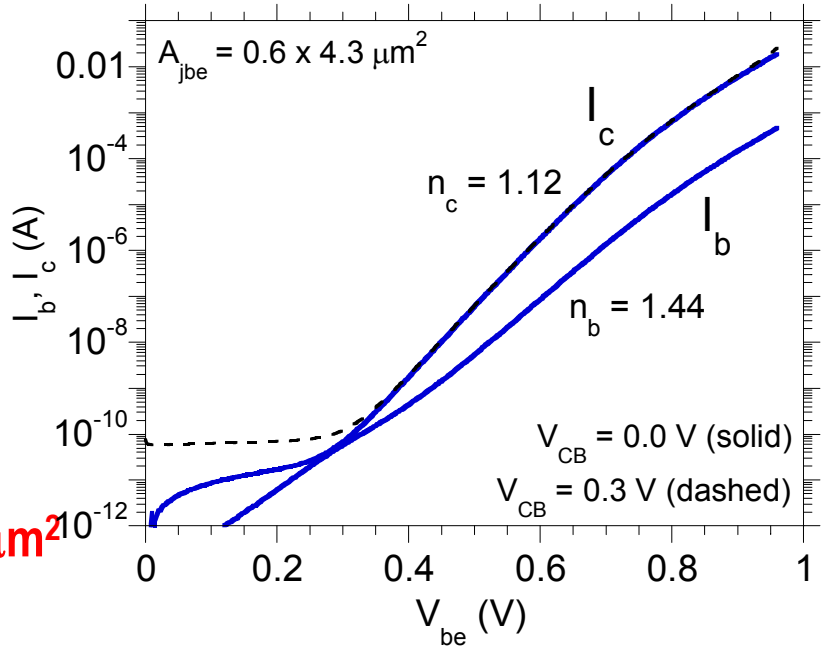




DC, RF performance—100 nm collector, 42 nm transition







Summary of device parameters—

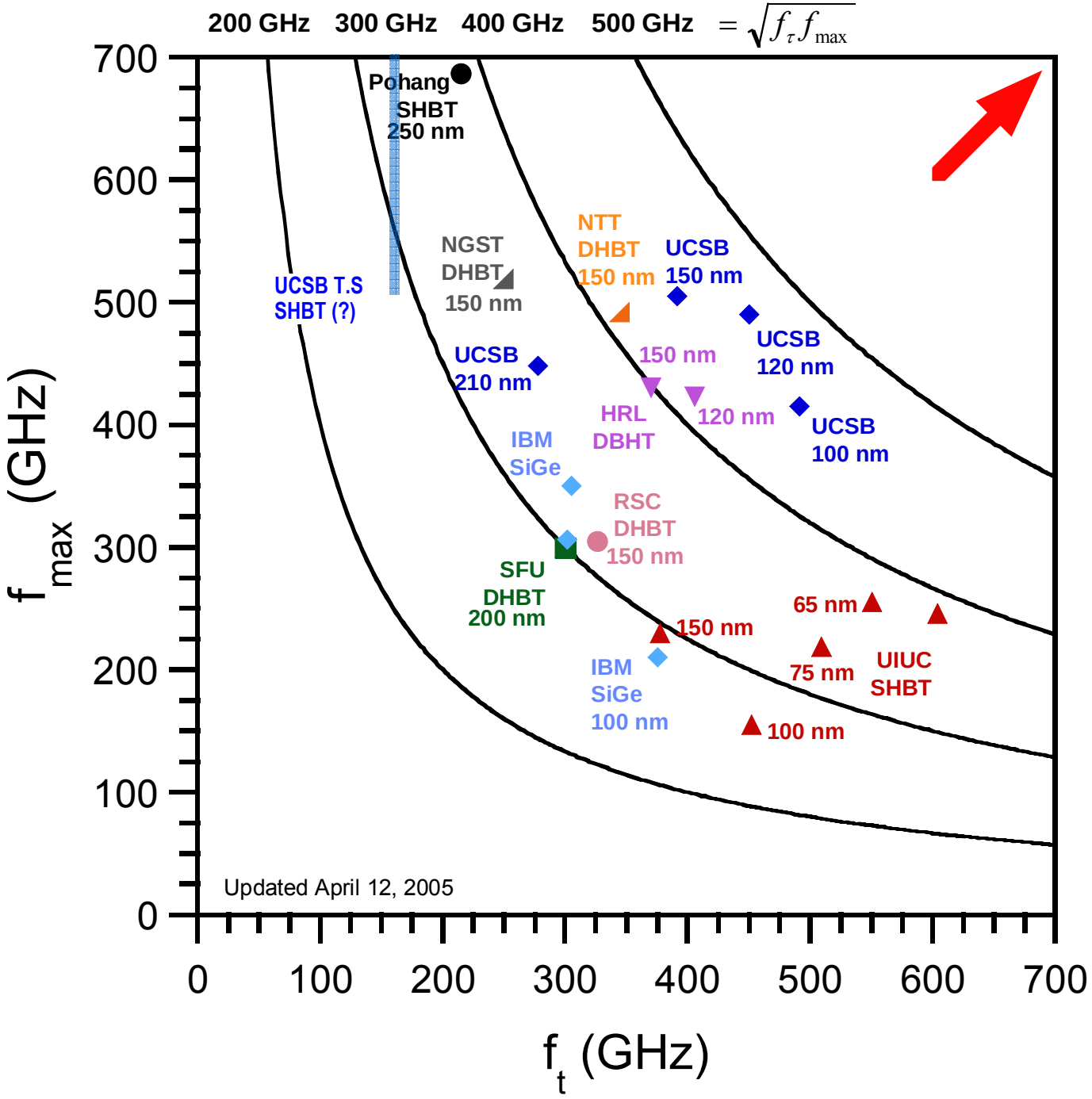
Average $\beta \approx 40$, $V_{BR,\,CEO} = 3.1$ V ($I_c = 50$ μA)

Emitter contact (from RF extraction), $R_{cont} \approx 7.8\ \Omega\cdot\mu m^2$

Base (from TLM) : $R_{sheet} = 629\ \Omega$/sq, $R_{cont} = 6.2\ \Omega\cdot\mu m^2$

Collector (from TLM) : $R_{sheet} = 12.9\ \Omega$/sq, $R_{cont} = 4.0\ \Omega\cdot\mu m^2$

Summary of HBT performance: April 2005



popular metrics :

$(f_\tau + f_{max})/2$

$\sqrt{f_\tau\, f_{max}}$

$(1/f_\tau + 1/f_{max})^{-1}$

better metrics :

power amplifiers :

PAE,

associated gain,

mW/μm

low noise amplifiers :

F_{min},

associated gain,

associated DC power

digital :

f_{clock}, hence

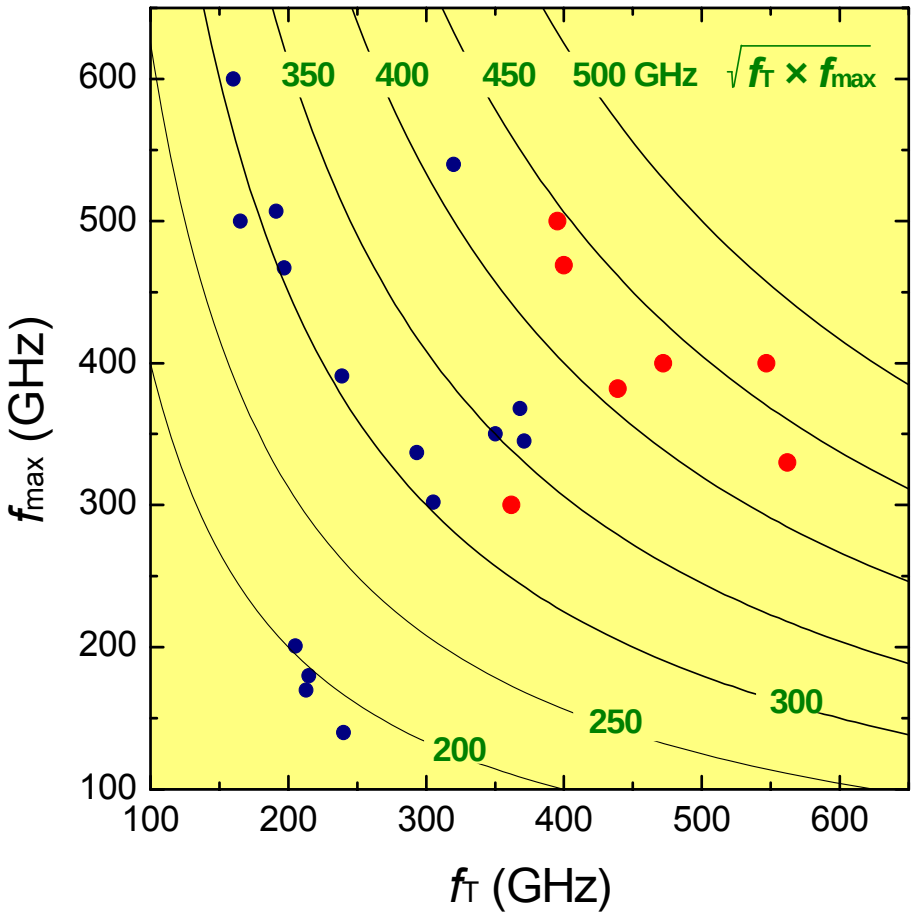
$(C_{cb}\Delta V / I_c)$,

$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

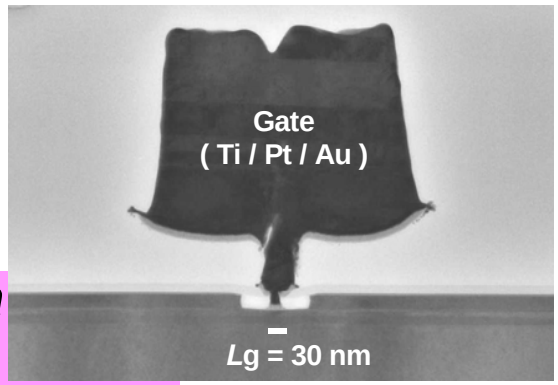
$(\tau_b + \tau_c)$

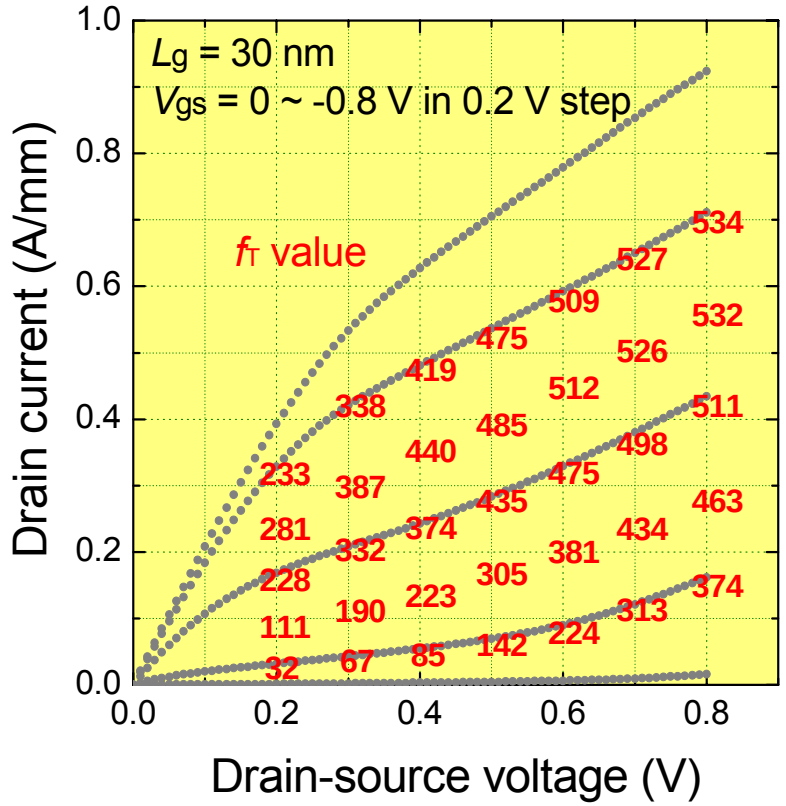
Comparison with InP HEMTs



HBTs have better breakdown than HEMTs
→ use HBTs for power amplifiers

HEMTs have better noise than HBTs
→ use HEMTs for LNAs





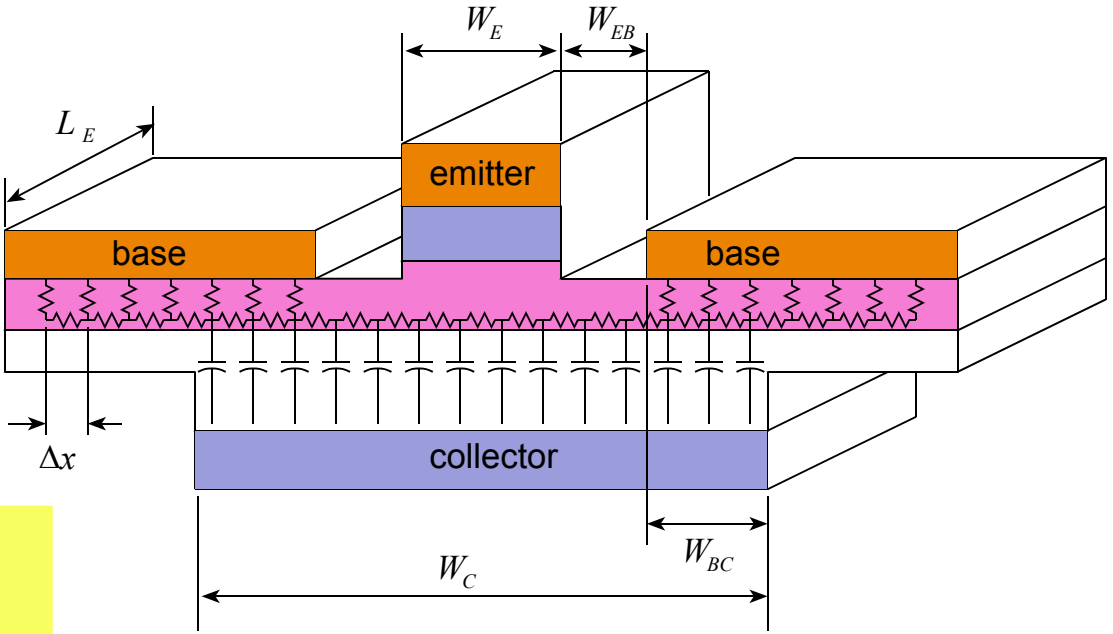
Keisuke Shinohara
CRL Japan

(Now at Rockwell Scientific)

transistor scaling theory

HBT scaling: layer thicknesses

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ 's



reduce T_b by $\sqrt{2}$:1

*$\rightarrow \tau_b$ **improved** 2:1*

reduce T_c by 2:1

*$\rightarrow \tau_c$ **improved** 2:1*

*note that Ccb has been **doubled***
..we had wanted it 2:1 smaller

$$\tau_b \cong T_b^2 / 2D_n$$

$$\tau_b \cong T_c / 2v_{sat}$$

Assume $W_C \sim W_E$

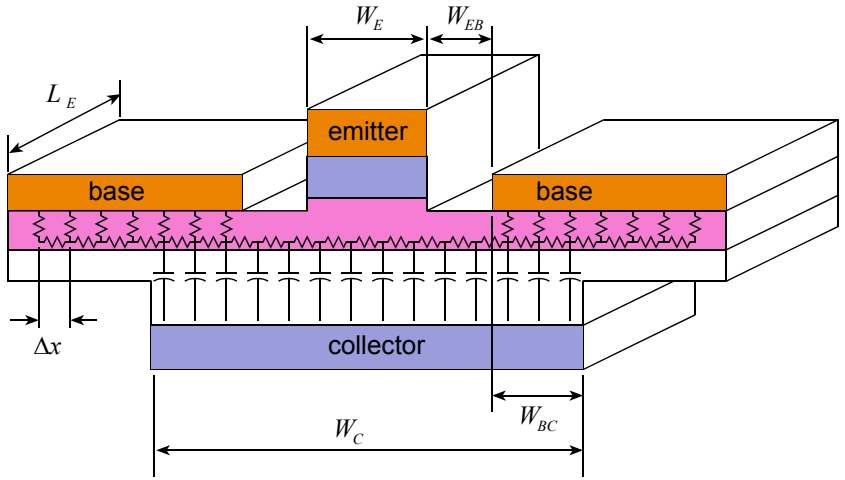
HBT scaling: lithographic dimensions

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ 's

Base Resistance R_{bb} must remain constant
$\rightarrow L_e$ must remain ~ constant

$$R_{bb} = R_{gap} + R_{spread} + R_{contact}$$
$$\cong R_{contact}$$
$$= \sqrt{\rho_{sheet}\rho_{c,vertical}}\Big/ 2L_E$$

*Ccb/Area has been **doubled***
..we had wanted it 2:1 smaller
…must make area=L_eW_e 4:1 smaller
$\rightarrow$ must make W_e & W_c 4:1 smaller



reduce collector width 4:1
reduce emitter width 4:1
keep emitter length constant

Assume $W_C \sim W_E$

HBT scaling: emitter resistivity, current density

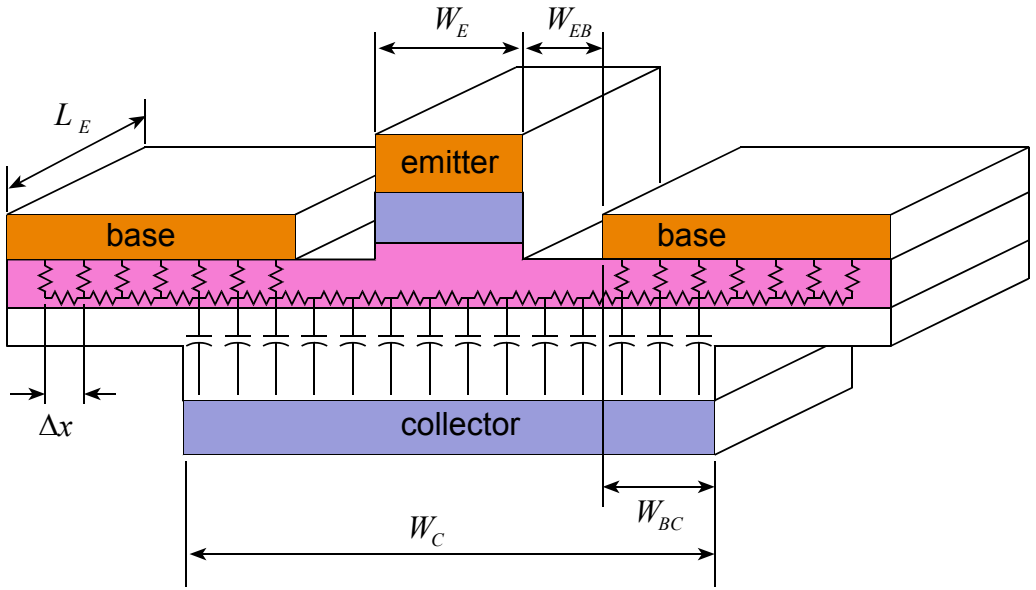
2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ 's

Emitter Resistance R_{ex} must remain constant
but emitter area=L_eW_e is 4:1 smaller
resistance per unit area must be 4:1 smaller

$$\text{Assume } W_C \sim W_E$$

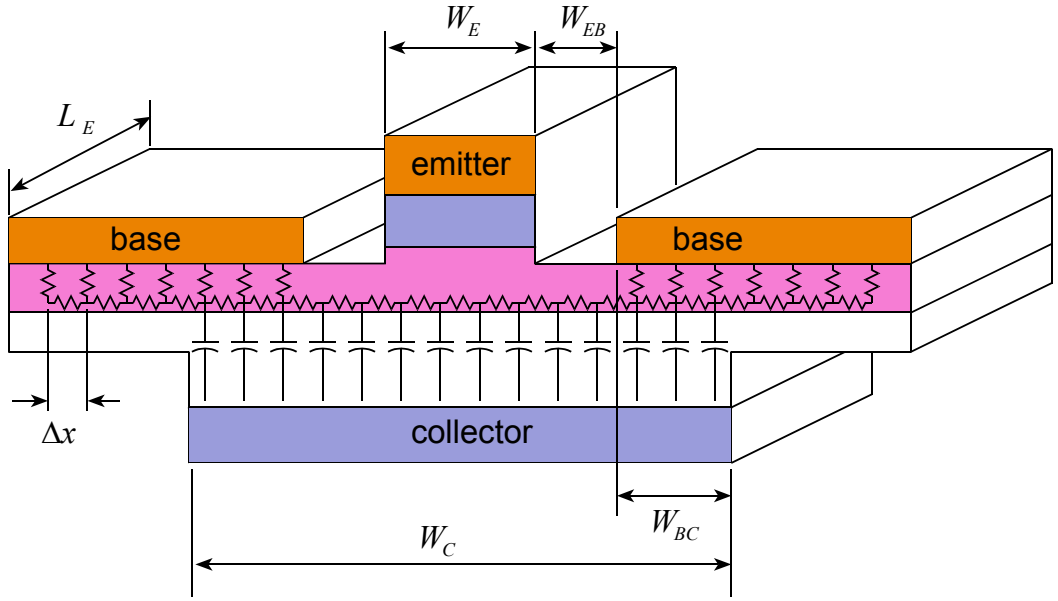
Collector current must remain constant
but emitter area=L_eW_e is 4:1 smaller
and collector area=L_cW_c is 4:1 smaller
current density must be 4:1 larger

increase current density 4:1
reduce emitter resistivity 4:1



Bipolar Transistor Scaling Laws

Scaling Laws:
design changes required
to double transistor bandwidth



key device parameter	required change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter resistance per unit emitter area	decrease 4:1
current density	increase 4:1
base contact resistivity (if contacts lie above collector junction)	decrease ~4:1
base contact resistivity (if contacts do not lie above collector junction)	unchanged

digital / mixed signal IC design and relationship to transistor

We design HBTs for fast logic, not for high f_τ & f_{max}

Gate Delay Determined by :

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C}\right)\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Depletion capacitance charging through the base resistance

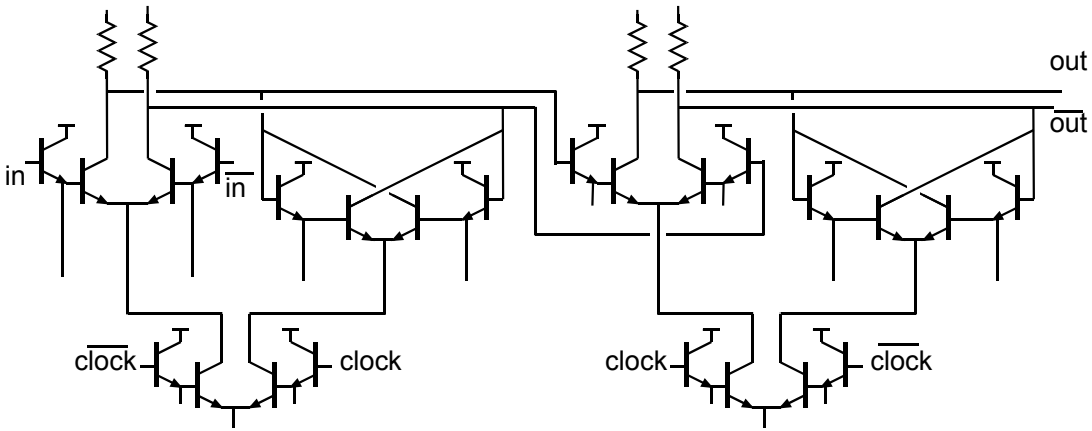
$$R_{\text{bb}}\left(C_{cbi}+C_{be,\text{depletion}}\right)$$

Supplying base + collector stored charge through the base resistance

$$R_{\text{bb}}\left(\tau_b+\tau_c\right)\left(\frac{I_C}{\Delta V_{LOGIC}}\right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 4\cdot\left(\frac{kT}{q}+R_{ex}I_c\right)$$



$(\tau_b+\tau_c)$ typically 10 - 25% of total delay;

Delay not well correlated with f_τ

$\left(\Delta V_{LOGIC}/I_C\right)\left(C_{cb}+C_{be,\text{depl}}\right)$ is 55% - 80% of total.

High $\left(I_C/C_{cb}\right)$ is a key HBT design objective.

$$J_{\max,Kirk}=2\varepsilon\bar{v}_{electron}\left(V_{ce,\text{operating}}+V_{ce,\text{full depletion}}\right)/T_c^2$$

$$\Rightarrow \frac{C_{cb}\Delta V_{LOGIC}}{I_C}=\frac{\Delta V_{LOGIC}}{2V_{CE,\min}}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2\bar{v}_{electron}}\right)$$

R_{ex} must be very low for low ΔV_{logic} at high J

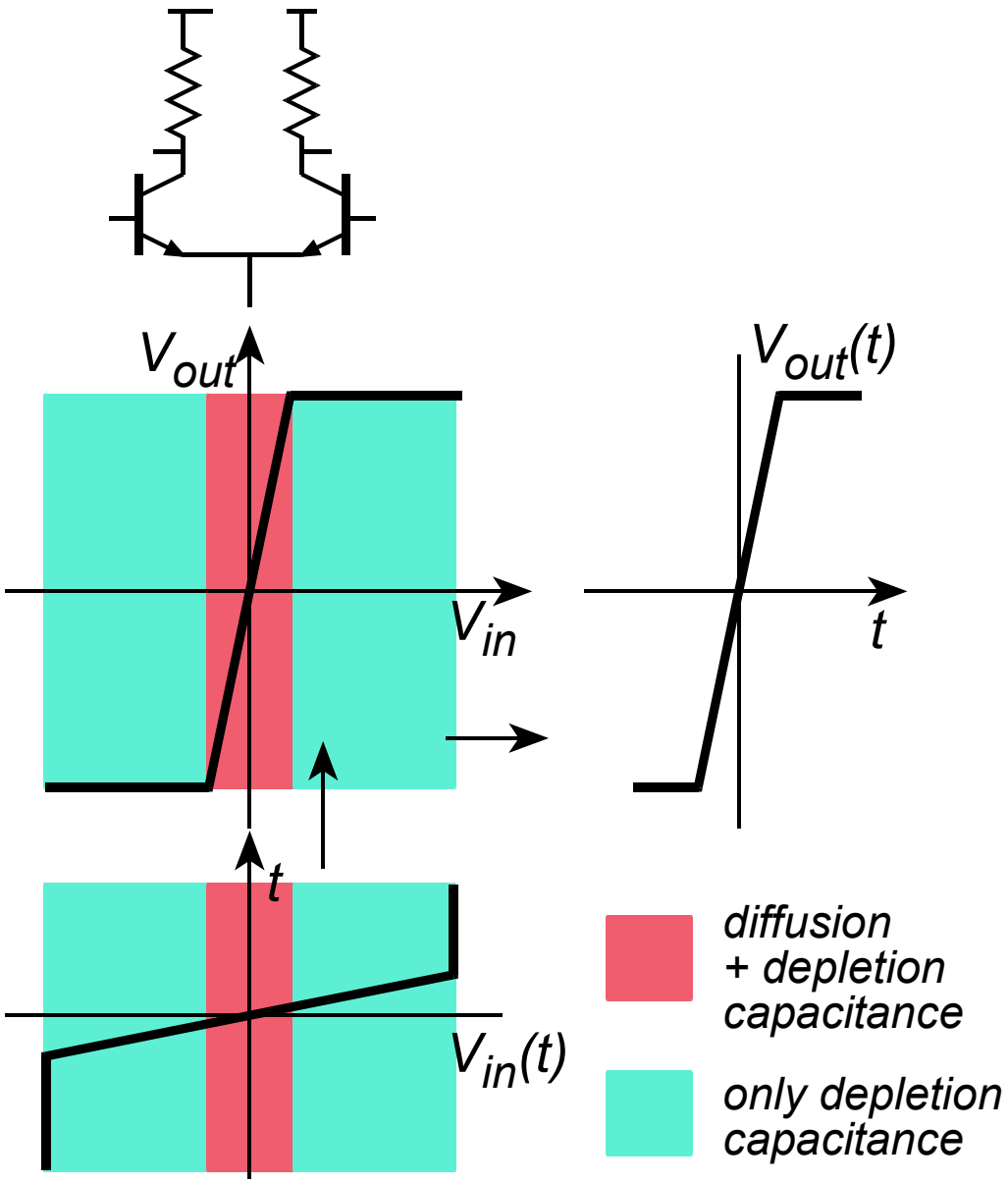
InP HBT Roadmaps: 40 / 80 / 160 Gb/s digital clock rate

Parameter	Gen. 1	Gen. 2	Gen. 3
MS-DFF speed	60 GHz	121 GHz	260 GHz
Emitter Width	1 μm	0.8 μm	0.3 μm
Parasitic Resistivity	50 Ω-μm²	20 Ω-μm²	5 Ω-μm²
Base Thickness	400Å	400Å	300 Å
Doping	5 10^{19}/cm²	7 10^{19}/cm²	7 10^{19}/cm²
Sheet resistance	750 Ω	700 Ω	700 Ω
Contact resistance	150 Ω-μm²	20 Ω-μm²	20 Ω-μm²
Collector Width	3 μm	1.6 μm	0.7 μm
Collector Thickness	3000 Å	2000 Å	1000 Å
Current Density	1 mA/μm²	2.3 mA/μm²	12 mA/μm²
$A_{collector}/A_{emitter}$	4.55	2.6	2.9
f_τ	170 GHz	248 GHz	570 GHz
f_{max}	170 GHz	411 GHz	680 GHz
I_E / L_E	1 mA/μm	1.9 mA/μm	3.7 mA/μm
τ_f	0.67 ps	0.50 ps	0.22 ps
C_{cb} / I_c	1.7 ps/V	0.62 ps/V	0.26 ps/V
$C_{cb}\Delta V_{logic} / I_c$	0.5 ps	0.19 ps	0.09 ps
$R_{bb} / (\Delta V_{logic} / I_c)$	0.8	0.68	0.99
$C_{je}(\Delta V_{logic} / I_C)$	1.7 ps	0.72 ps	0.15 ps
$R_{ex} / (\Delta V_{logic} / I_c)$	0.1	0.15	0.17

Key scaling challenges
emitter & base contact resistivity
current density→ device heating
collector-base junction width scaling
& Yield !

key figures of merit for logic speed

Why isn't base+collector transit time so important for logic?



Diffusion capacitance :

$$\delta Q_{\text{base}} = (\tau_b + \tau_c)\delta I_C$$

$$= (\tau_b + \tau_c)\frac{dI_C}{dV_{be}}\delta V_{be}$$

$$= \frac{(\tau_b + \tau_c)I_C}{kT/q}\delta V_{be}$$

...active only over kT/q voltage swing.

Under Large-Signal Operation :

$$\Delta Q_{\text{base}} = (\tau_b + \tau_c)I_C$$

$$= \frac{(\tau_b + \tau_c)I_{dc}}{\Delta V_{LOGIC}}\Delta V_{LOGIC}$$

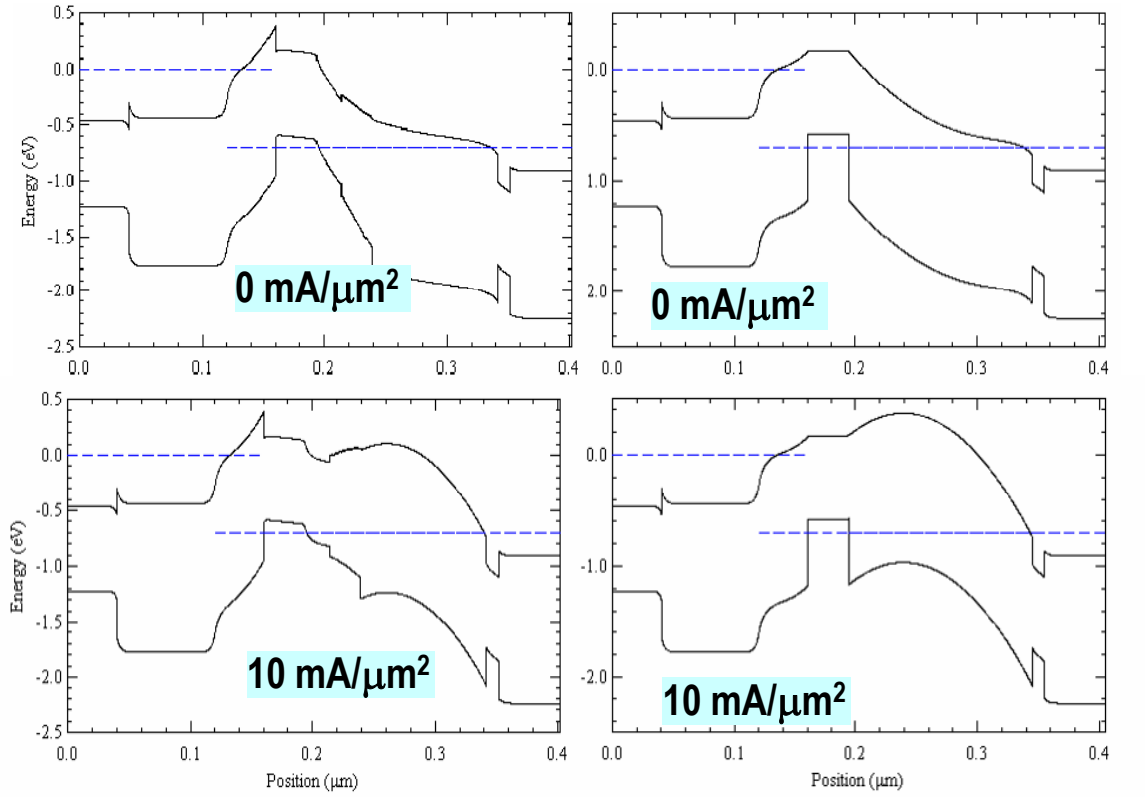
Large-signal diffusion capacitance reduced by ratio of

$$\left(\frac{\Delta V_{LOGIC}}{kT/q}\right),$$ which is $\sim 10:1$

Depletion capacitances present over full voltage swing, no large-signal reduction

Scaling Laws, Collector Current Density, C_{cb} charging time

InGaAs base GaAsSb base



Collector Depletion Layer Collapse

$$V_{cb,\min} + \phi > +(qN_d)(T_c^2 / 2\varepsilon)$$

Collector Field Collapse (Kirk Effect)

$$V_{cb} + \phi > +(J / v_{sat} - qN_d)(T_c^2 / 2\varepsilon)$$

$$\Rightarrow \quad J_{\max} = 2\varepsilon v_{eff}(V_{cb} + V_{cb,\min} + 2\phi) / T_c^2$$

Note that $V_{be} \cong \phi$, hence $(V_{cb} + \phi) \cong V_{ce}$

$$C_{cb}\Delta V_{LOGIC} / I_C = (\varepsilon A_{\text{collector}} / T_c)(\Delta V_{LOGIC} / I_C) = \frac{\Delta V_{LOGIC}}{(V_{CE} + V_{CE,\min})}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2v_{eff}}\right)$$

Collector capacitance charging time scales linearly with collector thickness if $J = J_{max}$

Key HBT Scaling Limit → Emitter Resistance

ECL delay not well correlated with f_τ or f_{max}

Largest delay is charging C_{cb}

$$C_{cb}\frac{\Delta V_{\text{logic}}}{I_C}=\frac{\varepsilon A_{\text{collector}}}{T_C}\frac{\Delta V_{\text{logic}}}{J_e A_{\text{emitter}}}\quad;\ \text{where } J_{e,\max}\propto 1/T_c^2.$$

→ $J_e \cong 10$ mA/μm² *needed for 200 GHz clock rate*

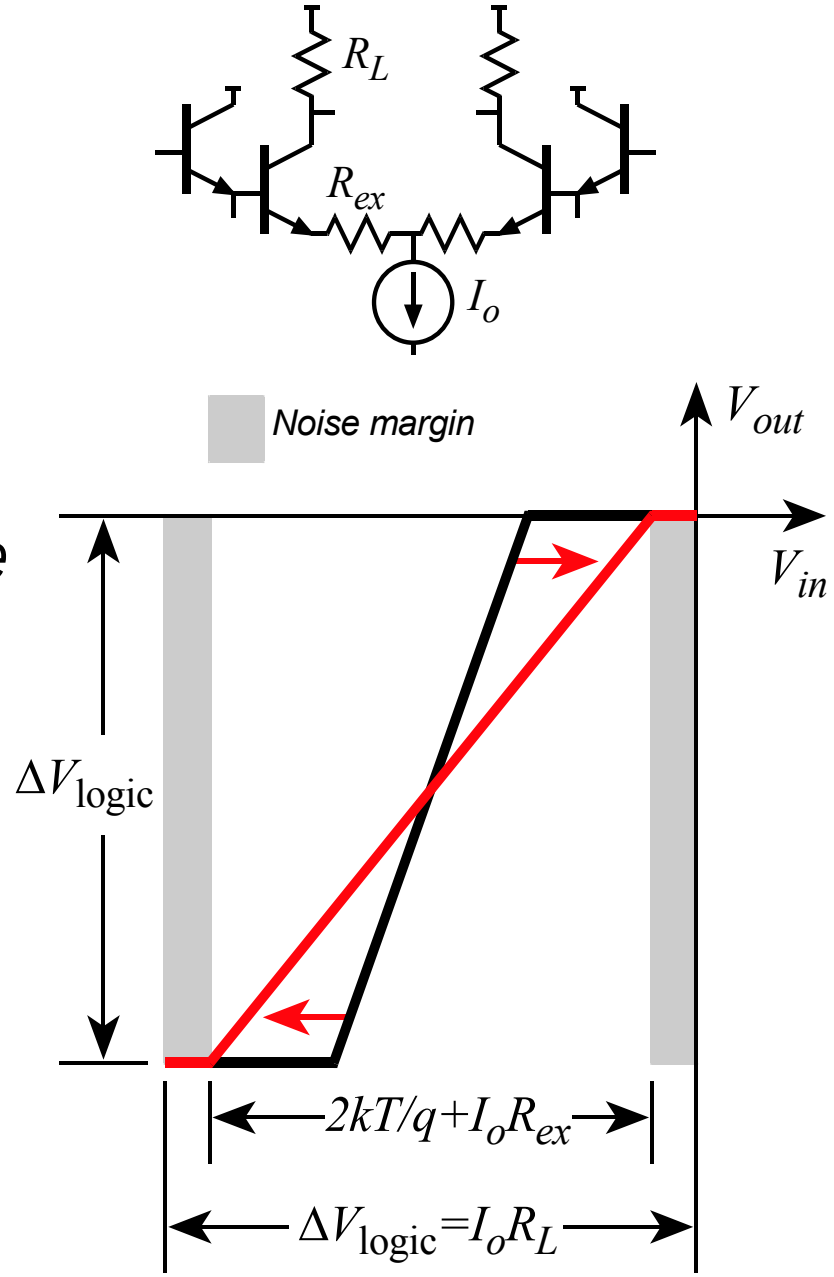
Voltage drop of emitter resistance becomes excessive

$R_{ex}I_c = \rho_{ex}J_e = (15\ \Omega\cdot\mu m^2)\cdot(10\ mA/\mu m^2) =$ ***150 mV***

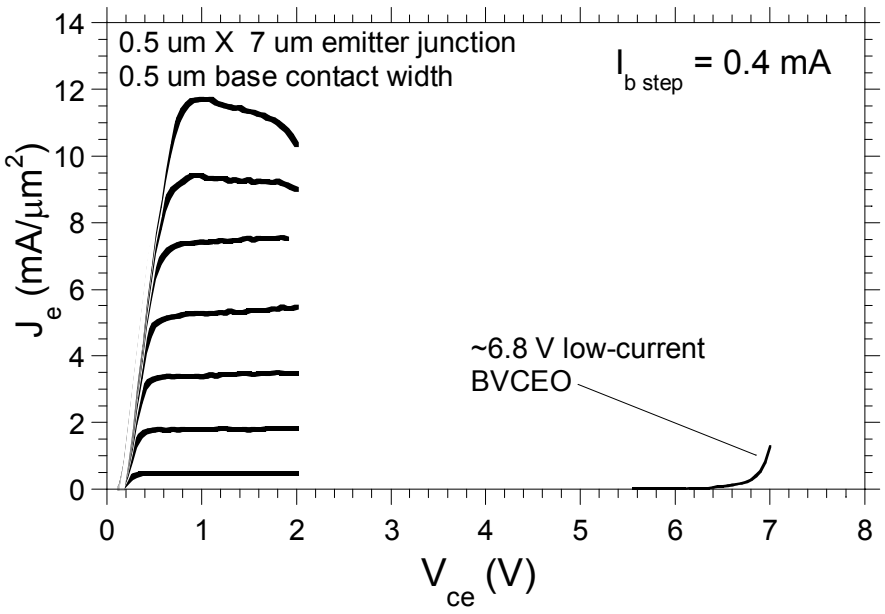
→ *considerable fraction of* $\Delta V_{logic} \cong 300$ *mV*

Degrades logic noise margin

→ $\rho_{ex} \le 7\ \Omega\cdot\mu m^2$ *needed for 200 GHz clock rate*



Breakdown: Thermal failure is more significant than BVCEO

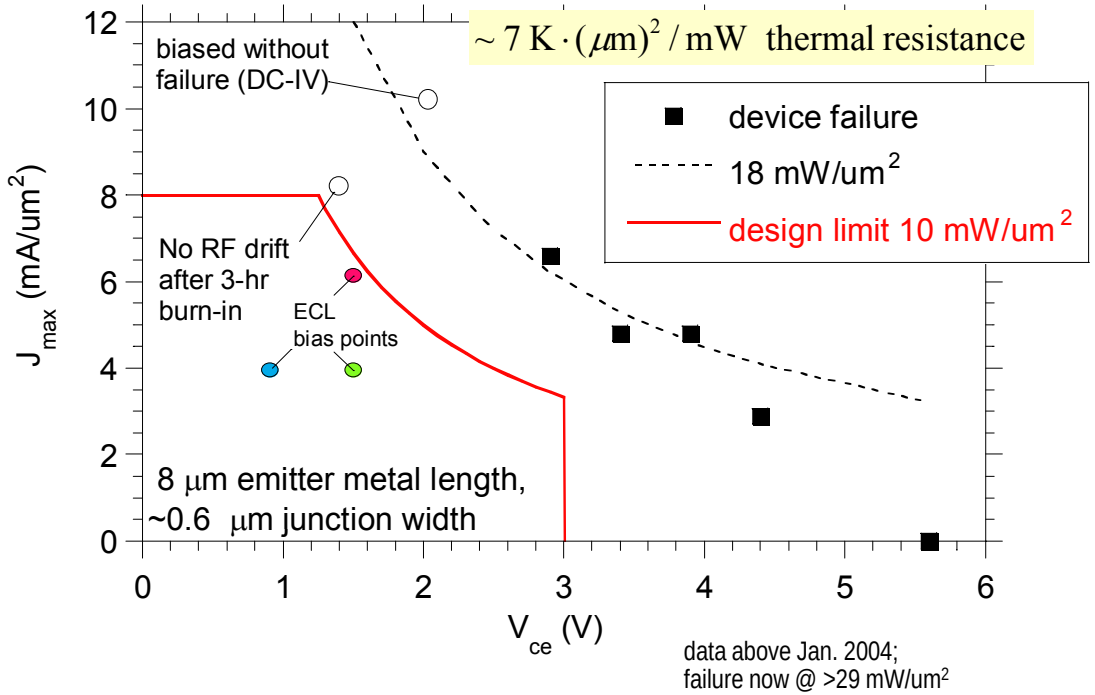


Breakdown - $V_{br,ceo}$ or $V_{br,cbo}$ - is measured at low J_e

High f_τ and $f_{\max}$ requires high J_e

$\Rightarrow$ low - current breakdown often not relevant

$V_{br,ceo} = E_{\max} T_{\text{collector}}$ decreases more slowly than f_{clock}^{-1} because $E_{\max}$ increases with thin collectors



Dissipation limits power density

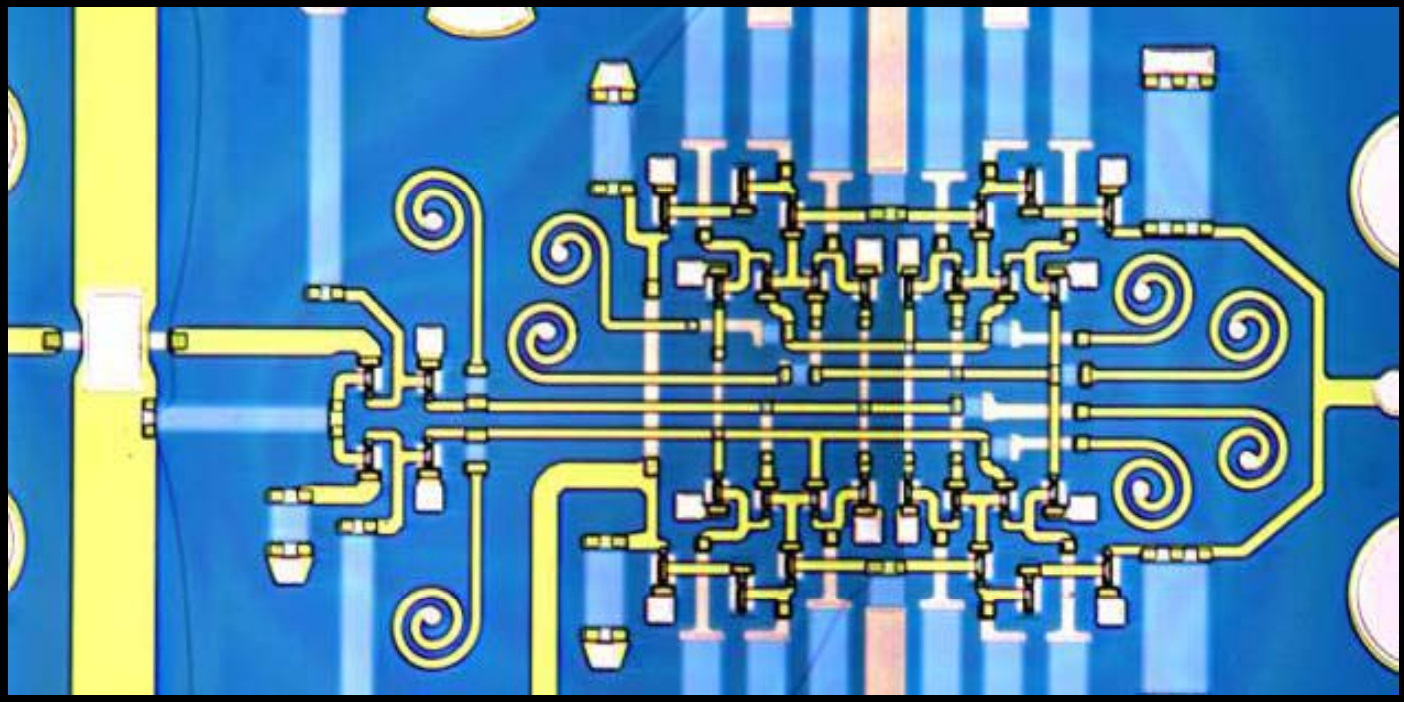
$P/A_E = J_E V_{ce} \propto f_{clock}^2 V_{CE}$

$\Rightarrow V_{\max} \propto 1/\theta_{ja} f_{clock}^2$

Low thermal resistance is critical. DHBTs are superior to SHBTs.

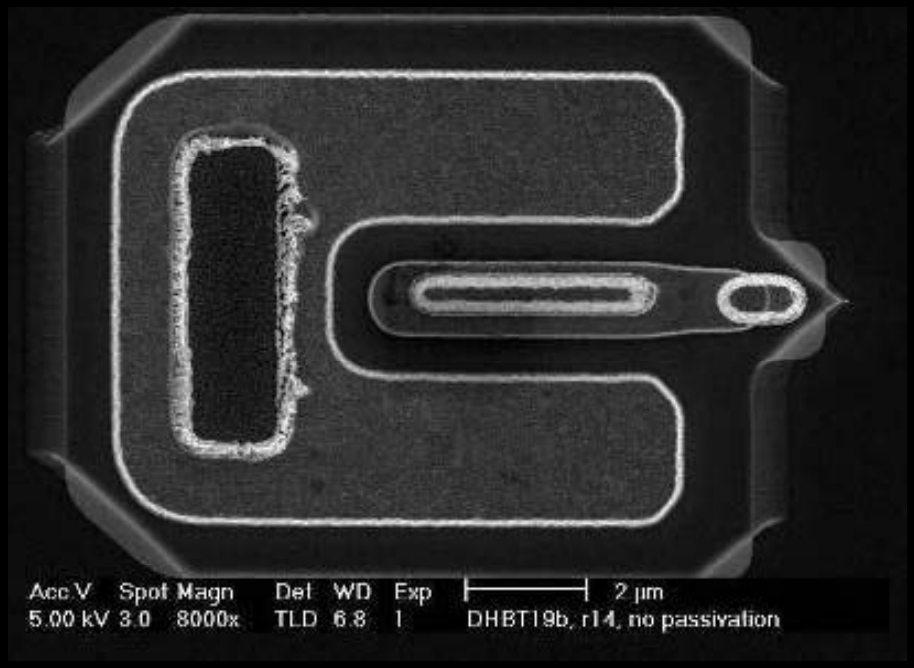
digital IC results

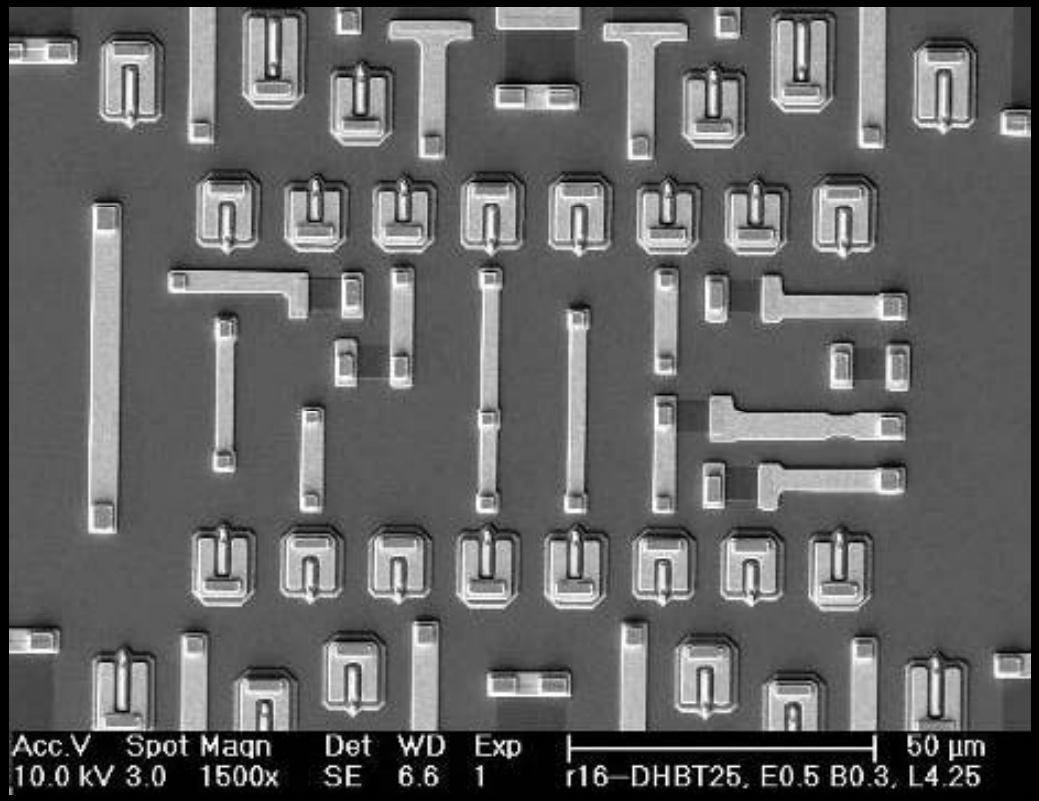
Digital circuits: towards 200 GHz clock rate



142 GHz latch from NNIN @ UCSB, 150 GHz ICs from UCSB/GSC/RSC
200 GHz is the next goal

underlying technology:
400-500 GHz InP transistors





Z Griffith

Static Frequency Divider: Standard Digital Benchmark

ECL Master-Slave Latch with Inverting Feedback

Forms 2:1 Frequency Divider.

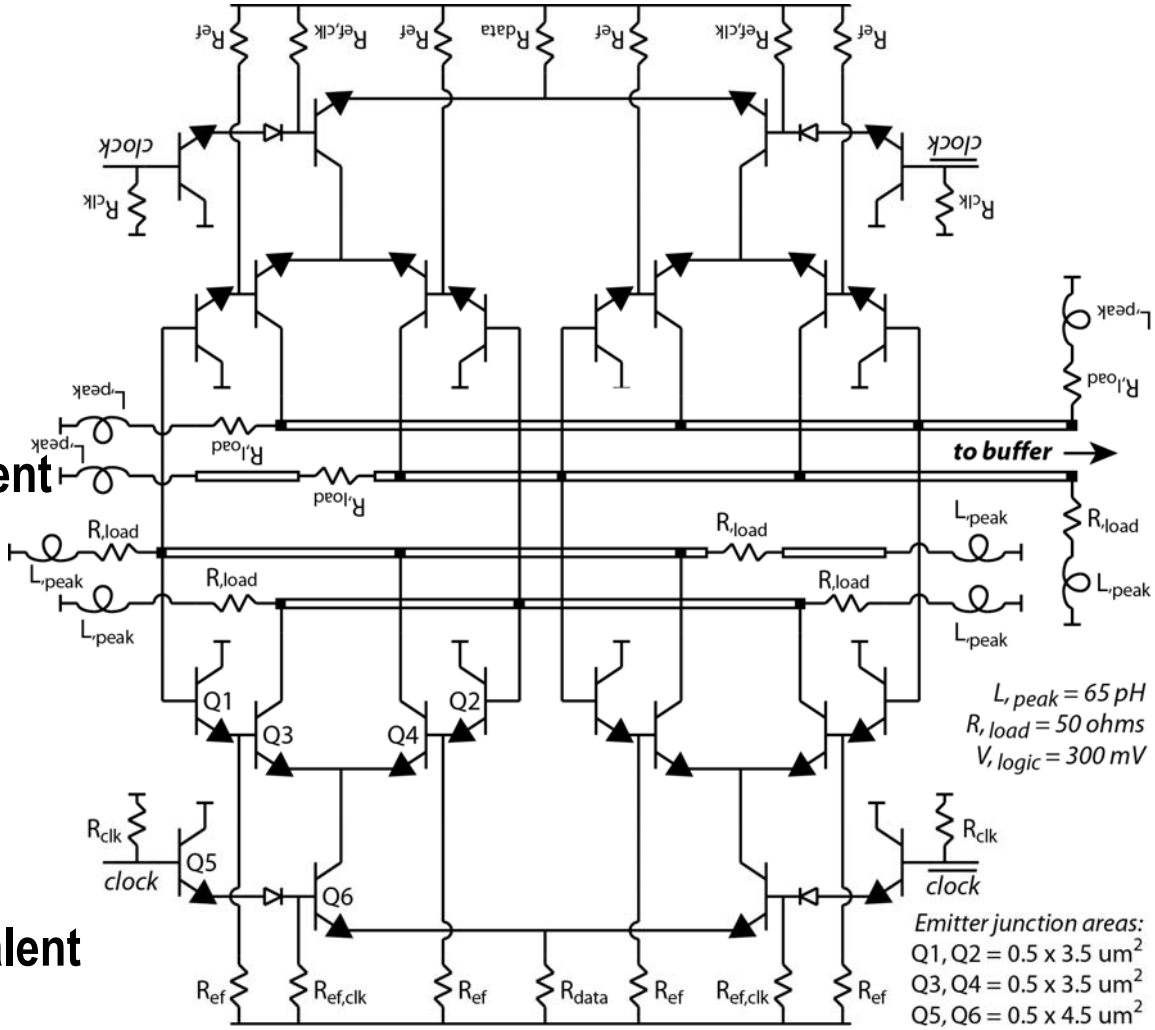
Maximum clock frequency is measure of technology speed.

Standard circuit configuration for consistent benchmarking - no tricks.

Small inductive peaking (L/R~1.3 ps).

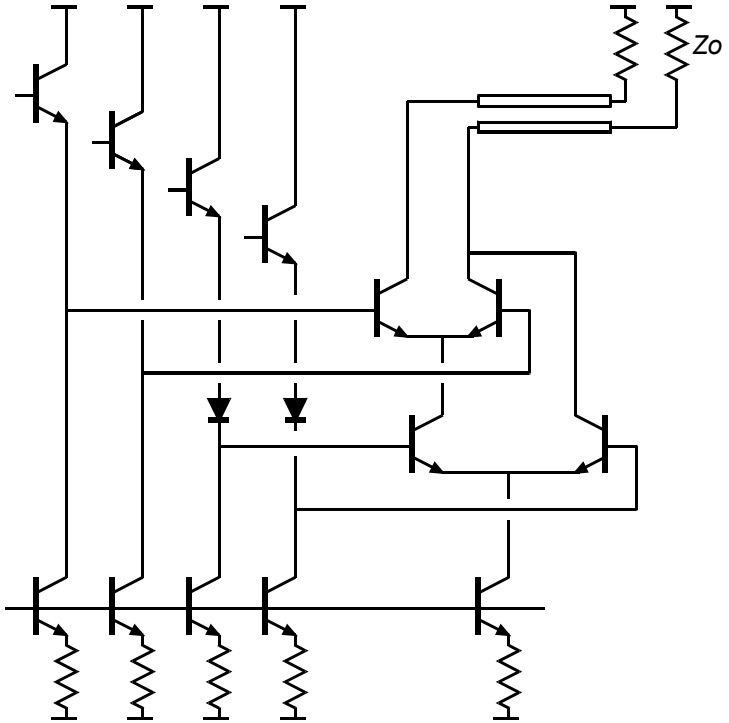
One clock period has 2 latch delay.
Each latch is a 2-input gate with an equivalent fanout of 2 or 3

→ much more strenuous test than 2:1 mux or ring oscillator

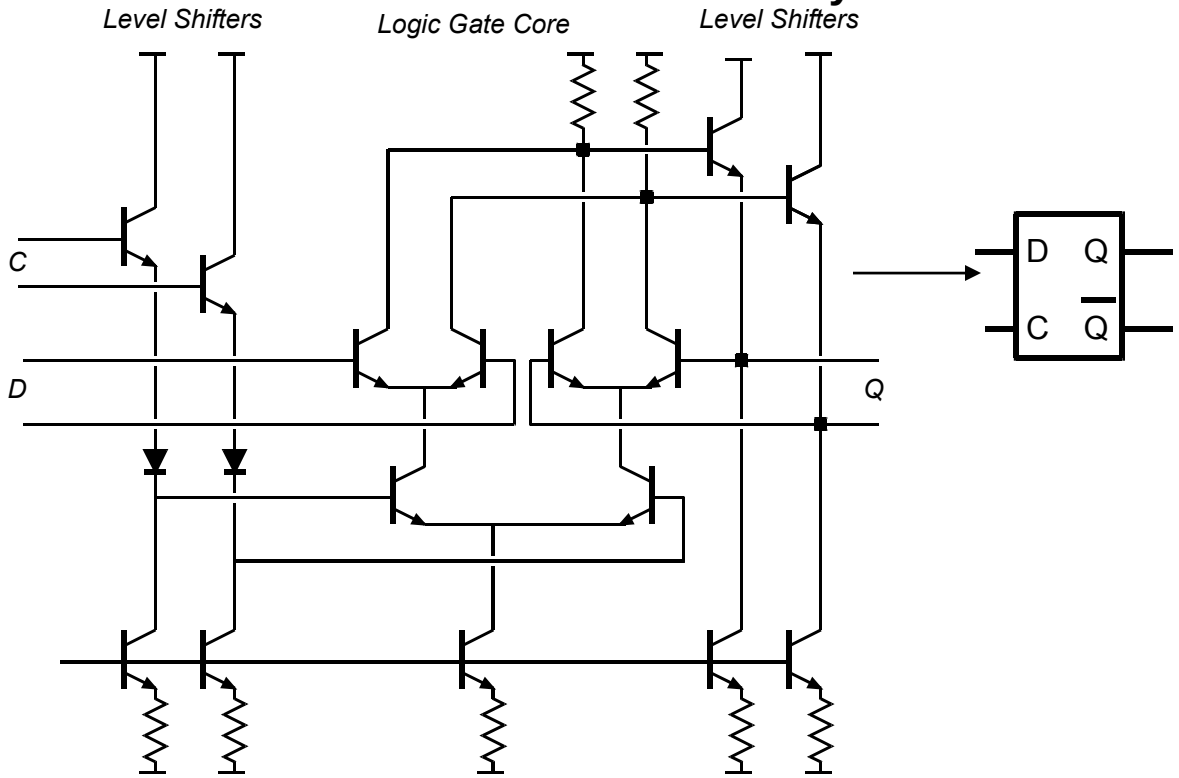


Hierarchy of ECL Static Frequency Divider

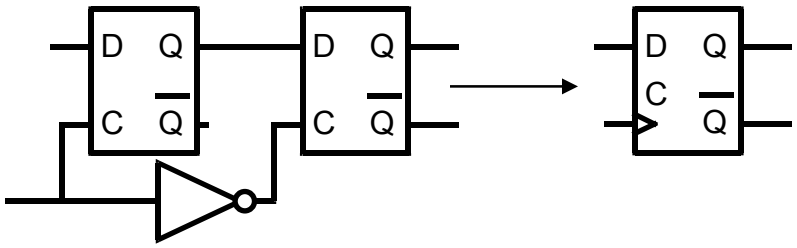
ECL NAND/NOR Gate



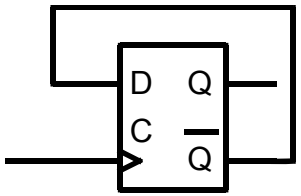
ECL Latch: level-clocked memory element



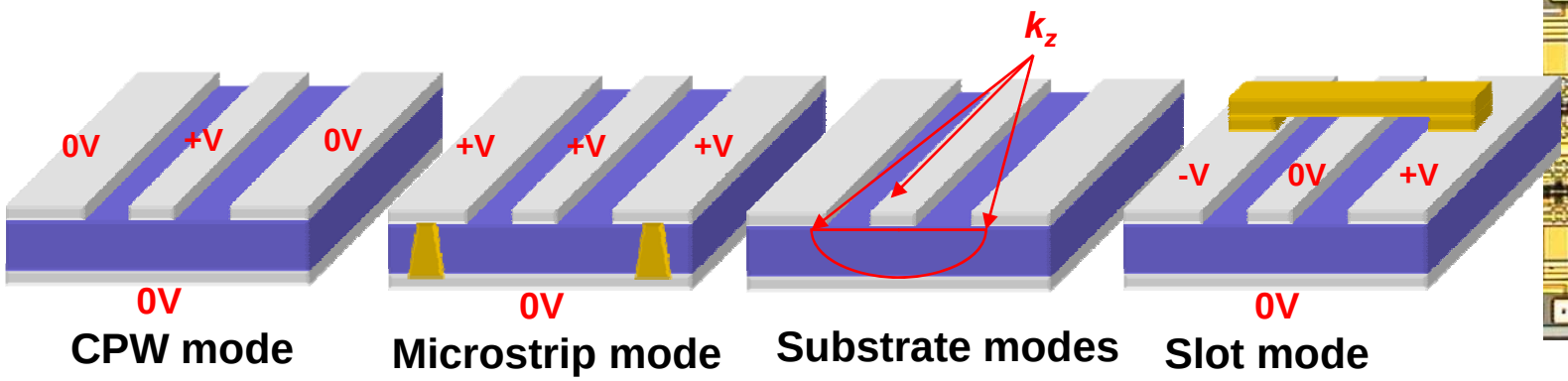
Master-Slave Latch:
transition-clocked memory element

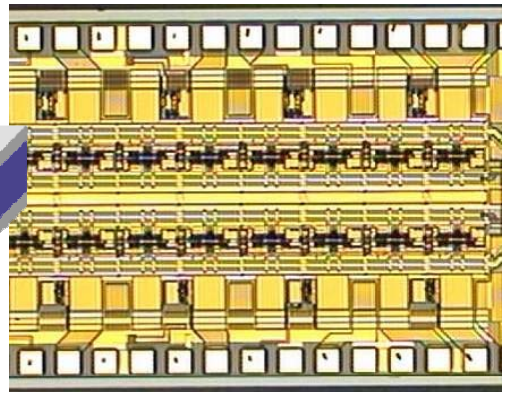


2:1 Static Frequency Divider



CPW has parasitic modes, coupling from poor ground plane integrity

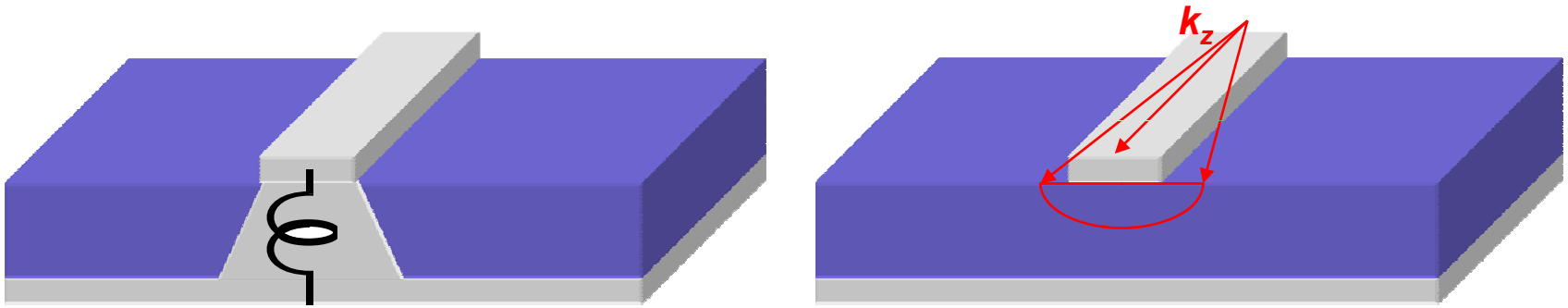




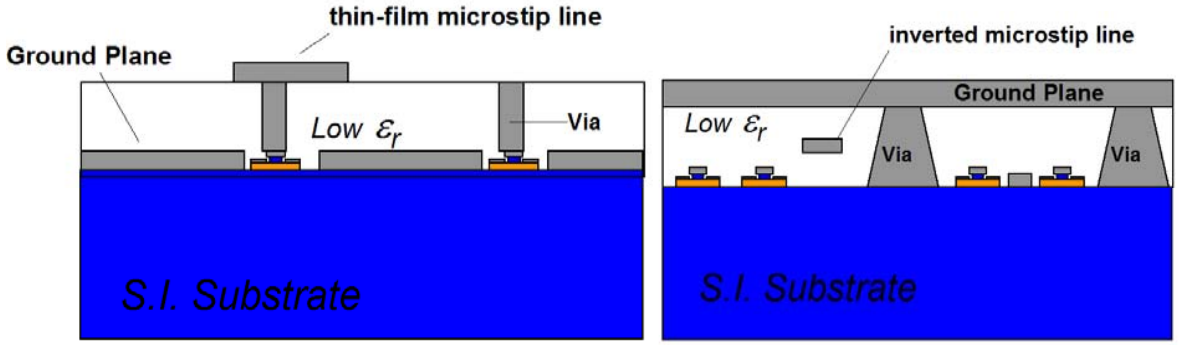
ground straps suppress slot mode, but multiple ground breaks in complex ICs produce ground return inductance
ground vias suppress microstrip mode, wafer thinning suppresses substrate modes

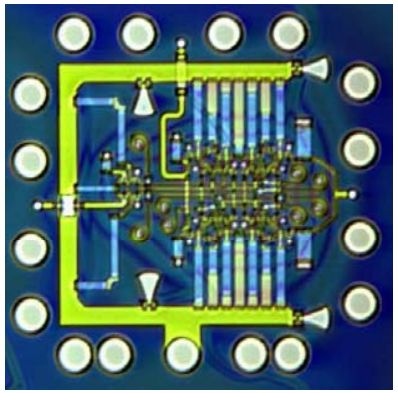
---

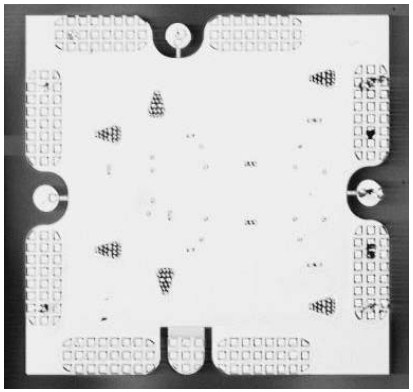
Microstrip has high via inductance, has mode coupling unless substrate is thin.



We prefer (credit to NTT) thin-film microstrip wiring, inverted is best for complex ICs



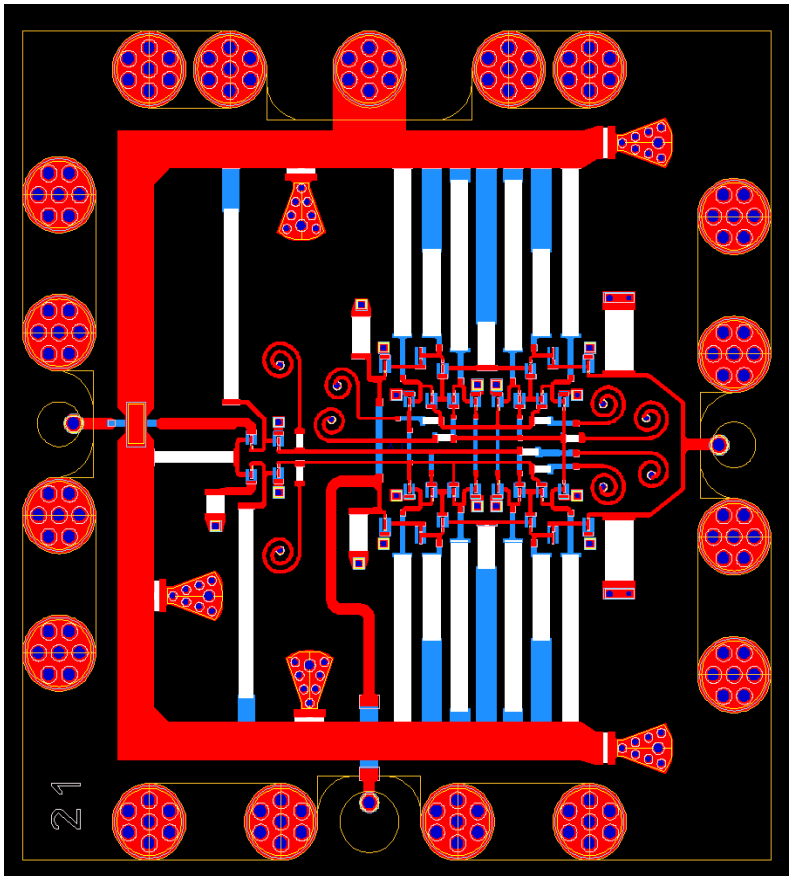




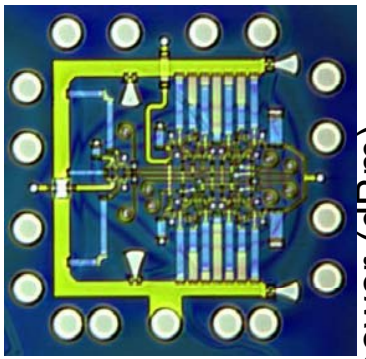
M. Urteaga, Z. Griffith, S. Krishnan

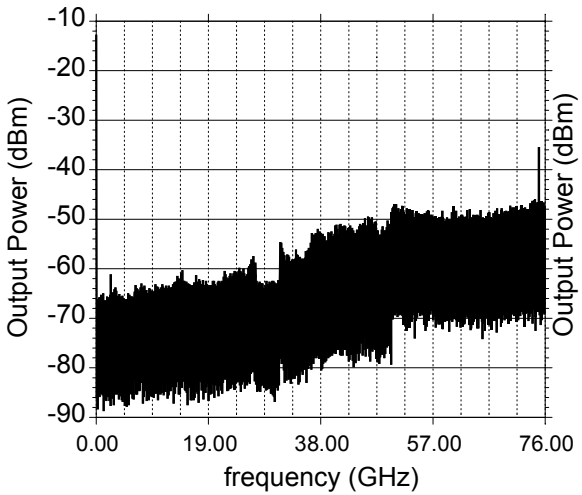
UCSB / RSC / GCS 150 GHz Static Frequency Dividers

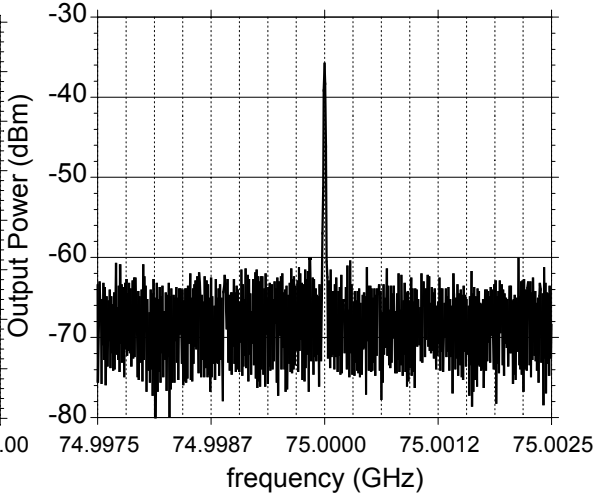
IC design: Z. Griffith, UCSB
HBT design: RSC / UCSB / GCS
IC Process / Fabrication: GCS
Test: UCSB / RSC / Mayo

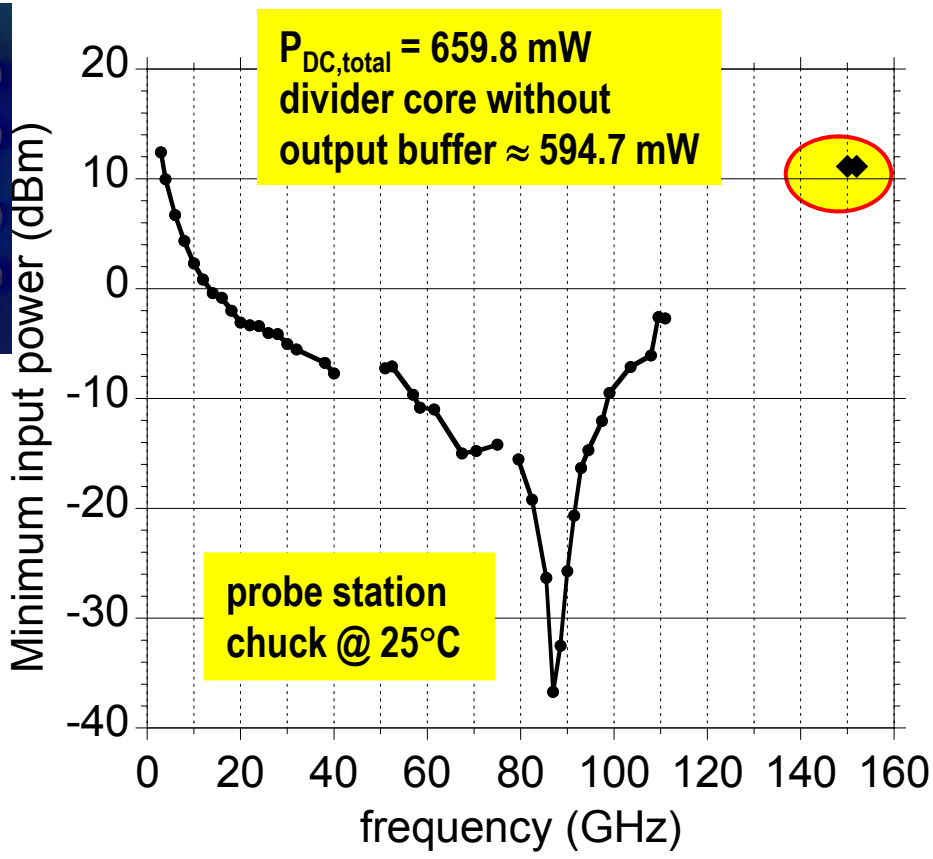


	units	data current steering	data emitter followers	clock current steering	clock emitter followers
size	μm^2	0.5 x 3.5	0.5 x 4.5	0.5 x 4.5	0.5 x 5.5
current density	$mA/\mu m^2$	6.9	4.4	4.4	4.4
C_{cb}/I_c	psec / V	0.59	0.99	0.74	0.86
V_{cb}	V	0.6	0	0.6	1.7
f_τ	GHz	301	260	301	280
f_{max}	GHz	358	268	358	280









Z. Griffith, M. Dahlström

UCSB 142 GHz Master-Slave Latches (Static Frequency Dividers)

Static 2:1 divider:
Standard digital benchmark.
Master-slave latch with inverting feedback.
Performance comparison between digital technologies

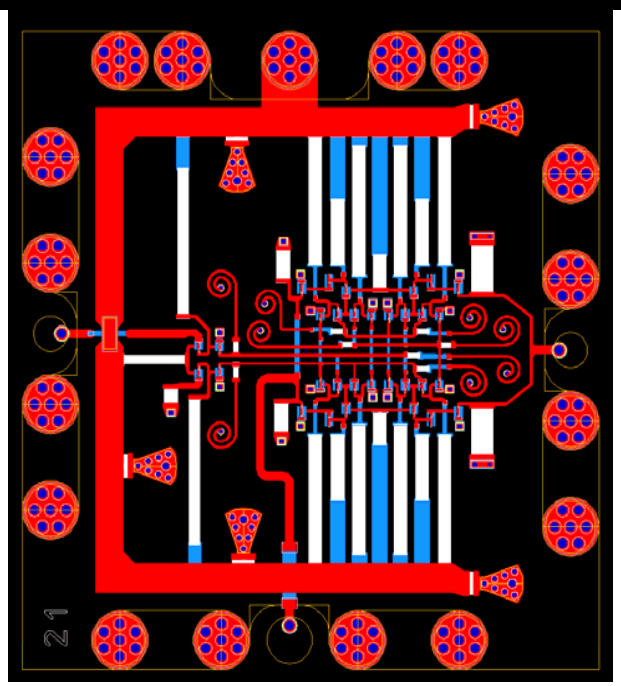
UCSB technology 2004:
InP mesa HBT technology
12-mask process
600 nm emitter width
142 GHz maximum clock.

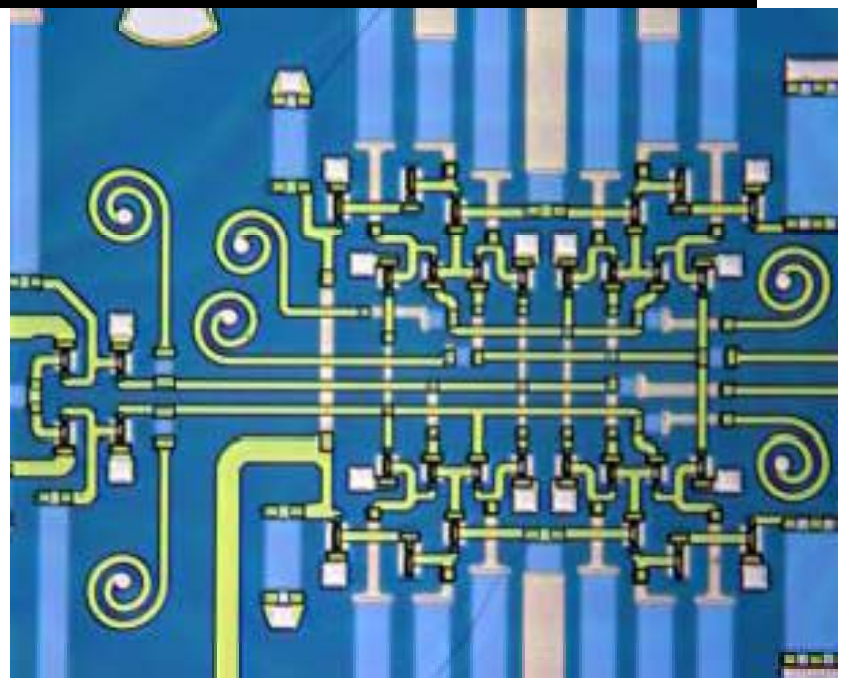
Implications:

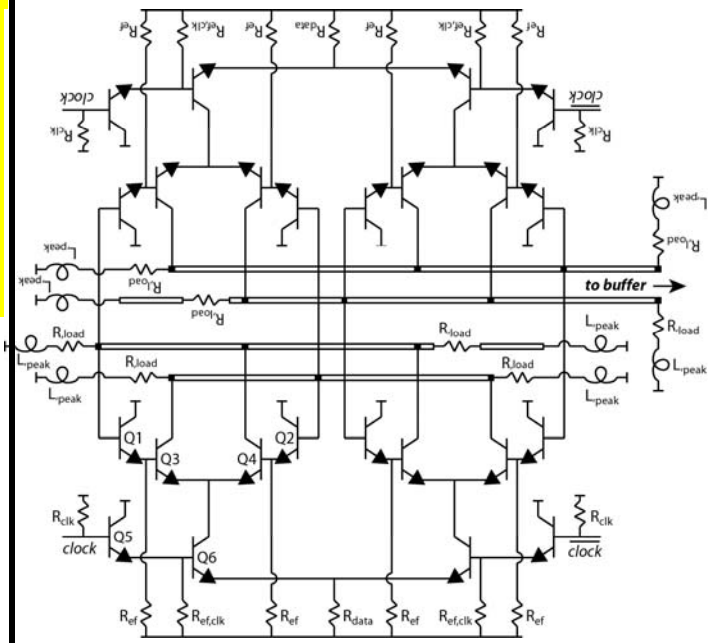
160 Gb/s fiber ICs

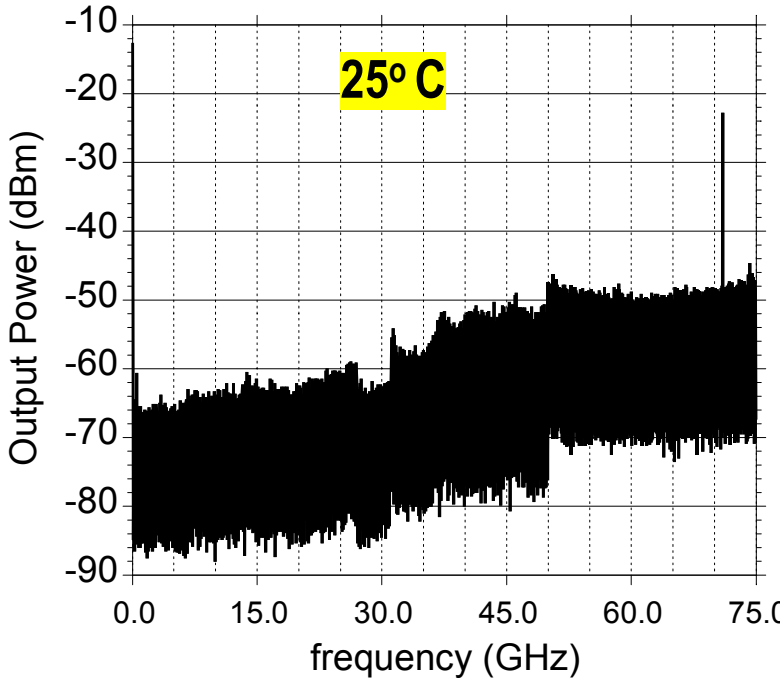
100 + Gb/s serial links

Target is 260 GHz clock rate at 300 nm scaling generation

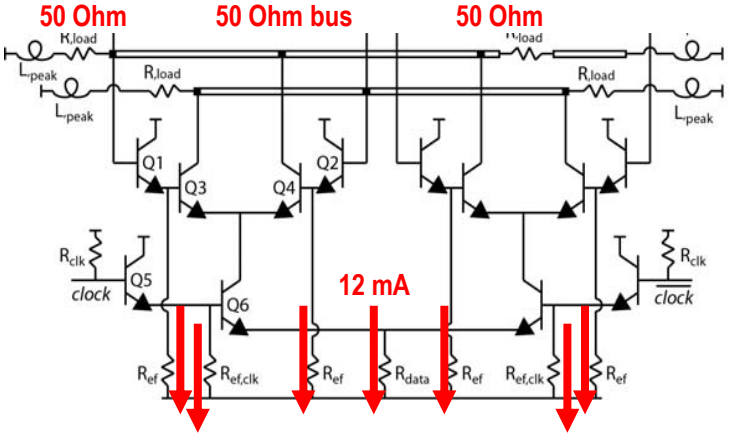




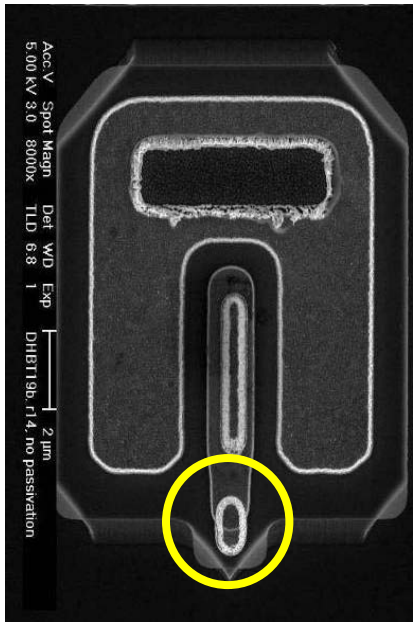


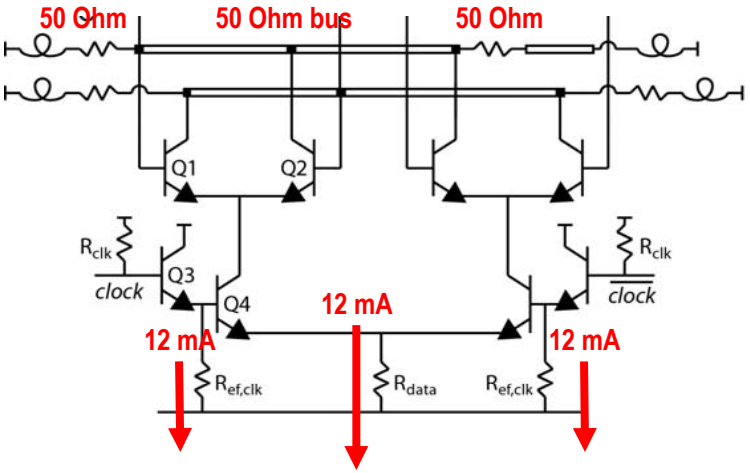


Reducing Divide-by-2 Dissipation

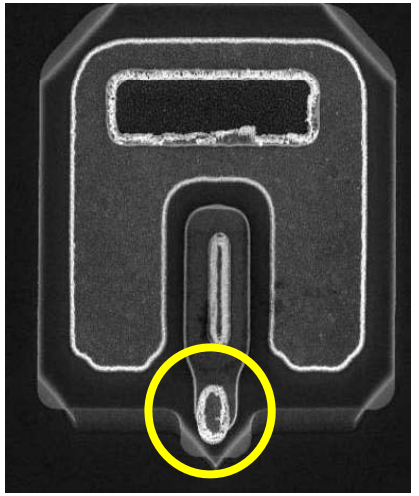


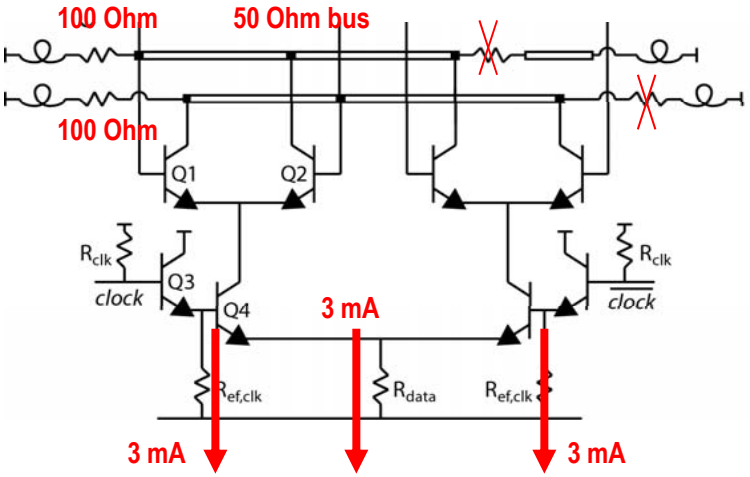
ECL with impedance-matched 50 Ohm bus:
25 Ohm load→ switch 12 mA
12 mA x 7 x 4 V = 336 mW/latch





CML with impedance-matched 50 Ohm bus:
25 Ohm load→ switch 12 mA
12 mA x 3 x 3 V = 108 mW/latch





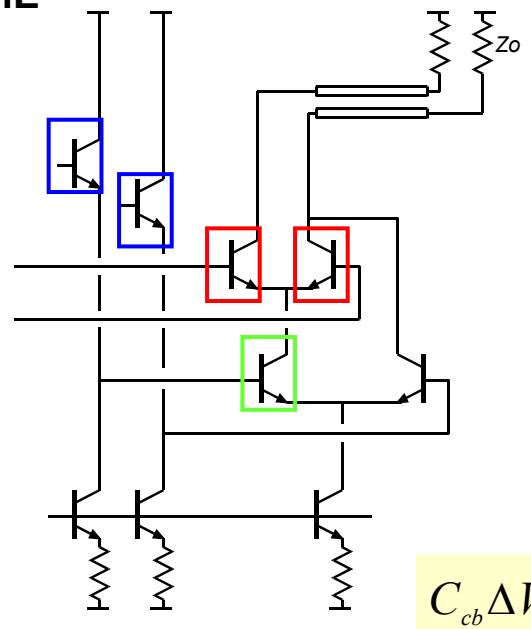
Low-Power CML
100 Ohm loaded → switch 3 mA
3 mA x 3 x 3 V = 27 mW/latch

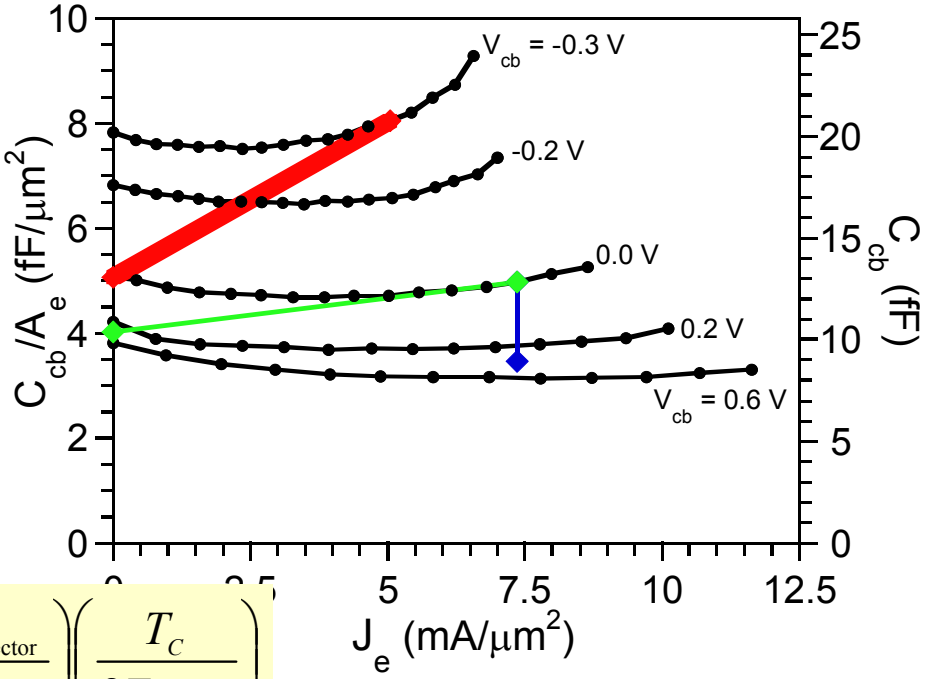
$$\text{High speed} @ \text{low power} = \text{low } C_{wiring}, \text{low } C_{cb,pad}$$

Significant dissipation in the emitter-follower level-shifters

C_{cb}/I_c Charging Rate: ECL is much better than CML

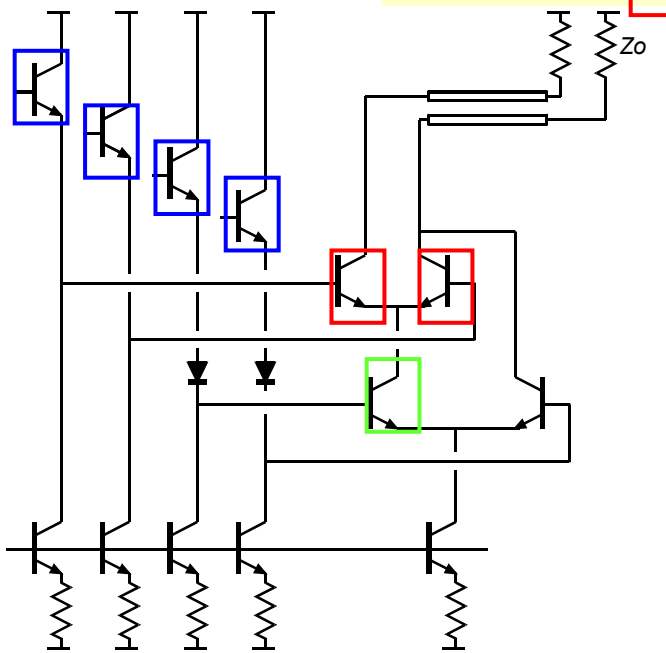
CML

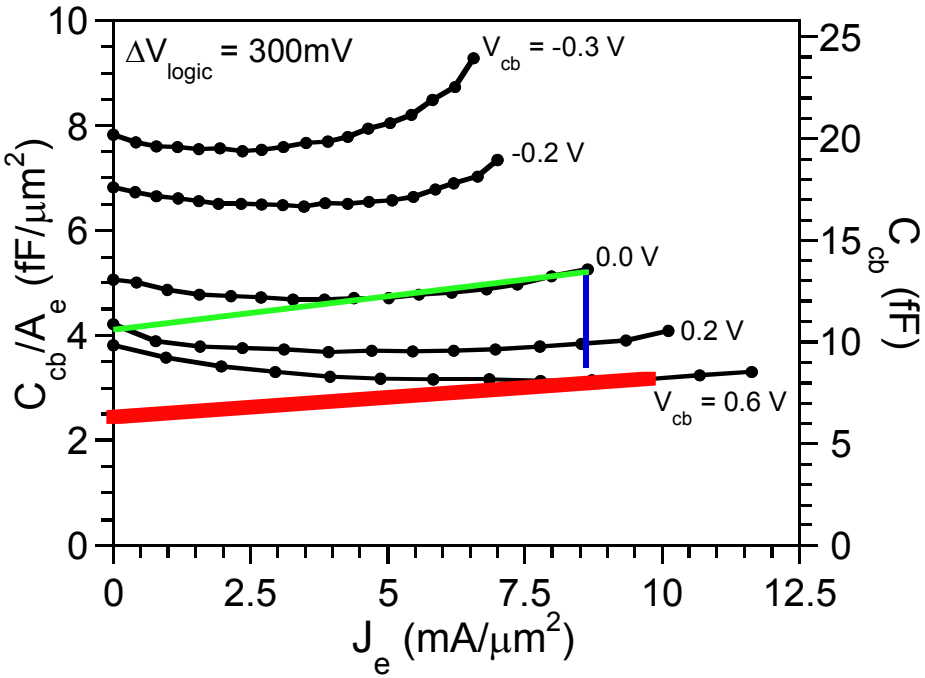




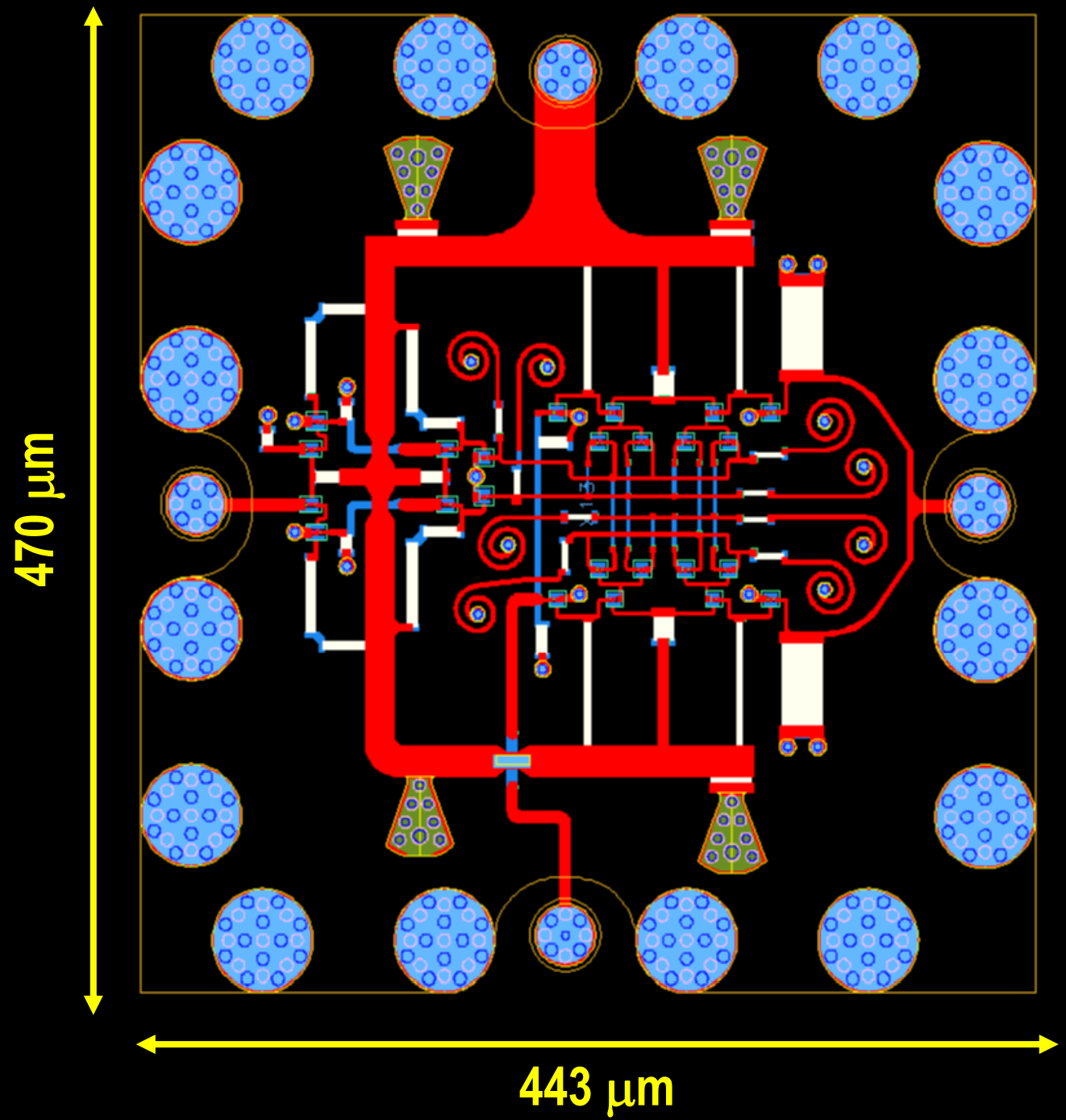
$$\frac{C_{cb}\Delta V_{LOGIC}}{I_C} = \frac{\Delta V_{LOGIC}}{V_{CE} + V_{CE,\min}}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2\bar{v}_{electron}}\right)$$

ECL





Phase II divide by 2—Ultra low power CML divider



Simulated divider speed…

With Collector Pedestal

A_{jbe} = 1.0 μm², f_{max} = 100 GHz

$P_{divider\ core,} \approx 31$ mW

mm-wave amplifiers

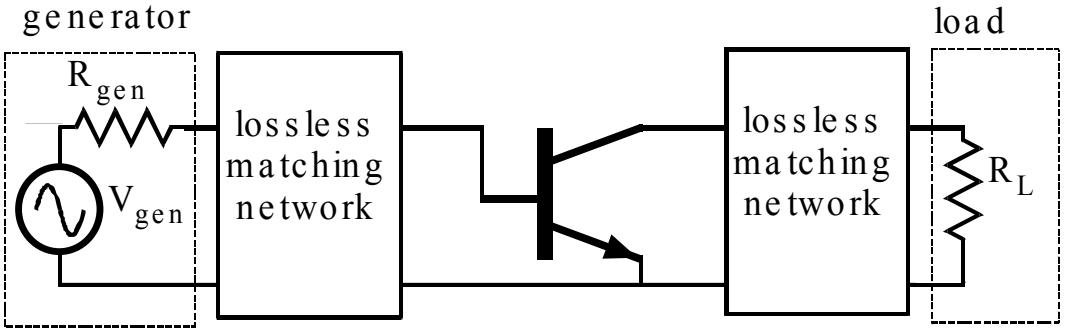
Tuned Amplifier Design for Maximum Gain

If Device is Unconditionally Stable

Simultaneously match input and output of device

$$\mathbf{MAG} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right)$$

K = Rollet stability factor

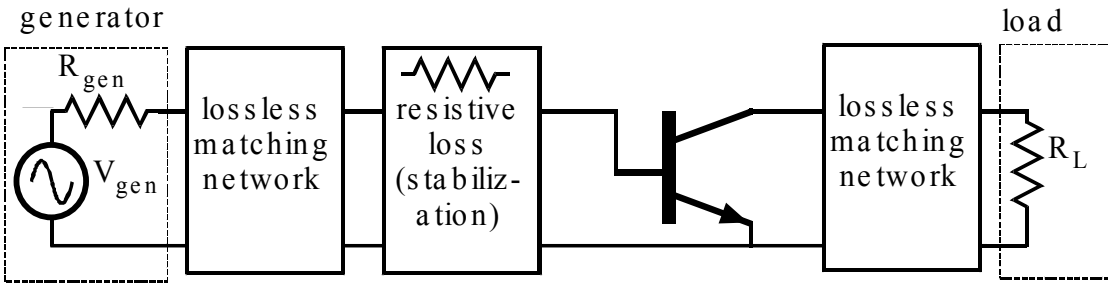


If transistor is unconditionally stable, circuit gain is transistor MAG

If Device is Potentially Unstable

Stabilize transistor and simultaneously match input and output of device

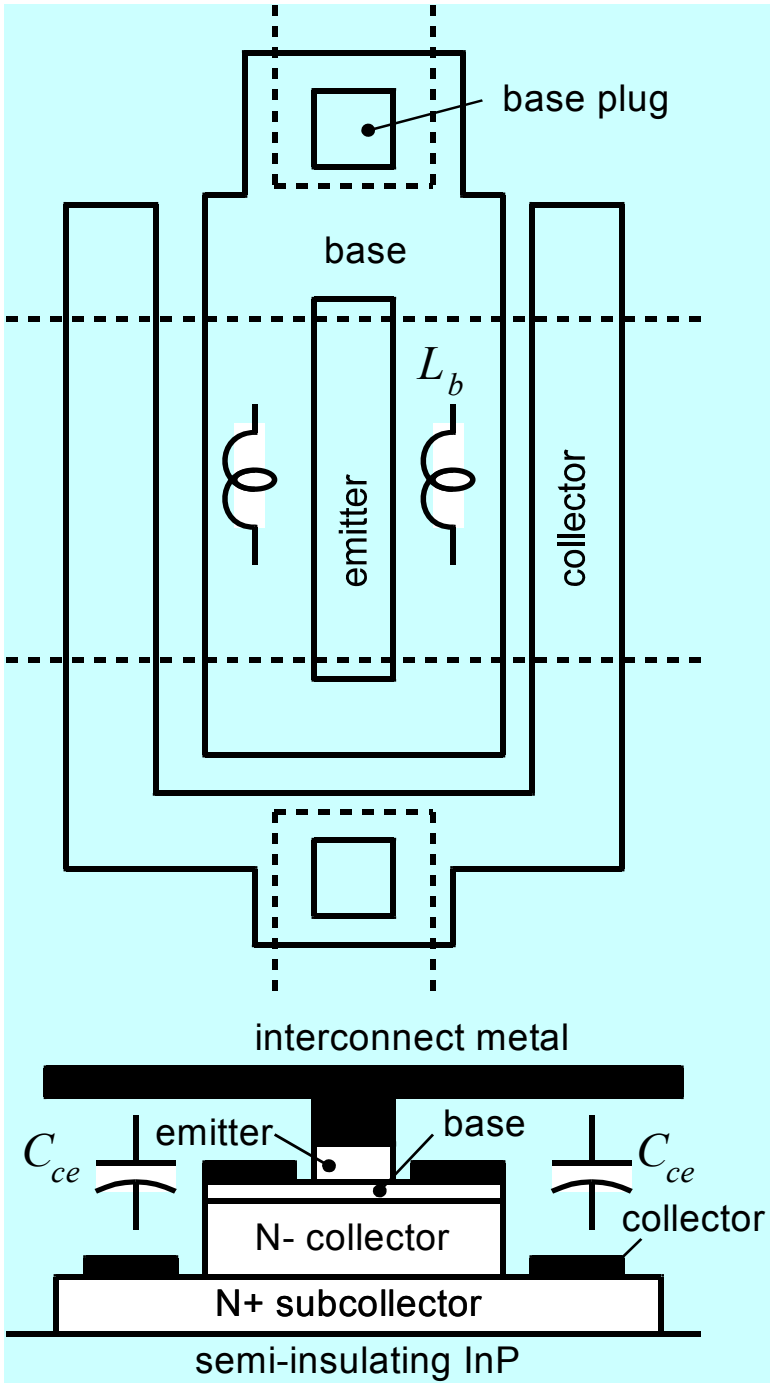
$$\mathbf{MSG} = \frac{|S_{21}|}{|S_{12}|} = \frac{|Y_{21}|}{|Y_{12}|}$$

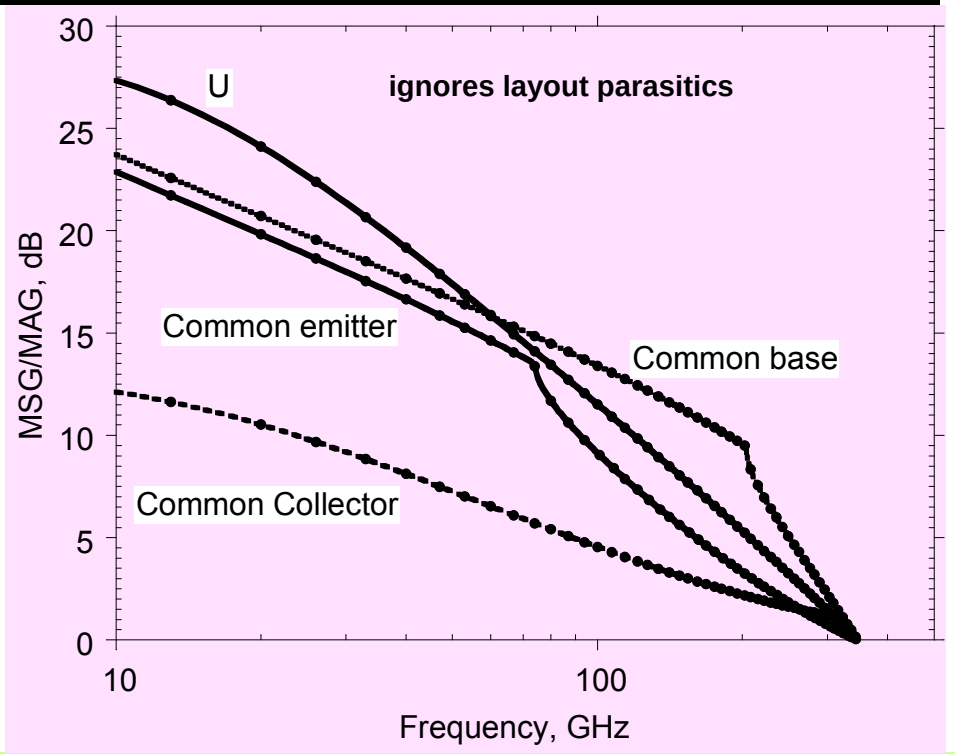


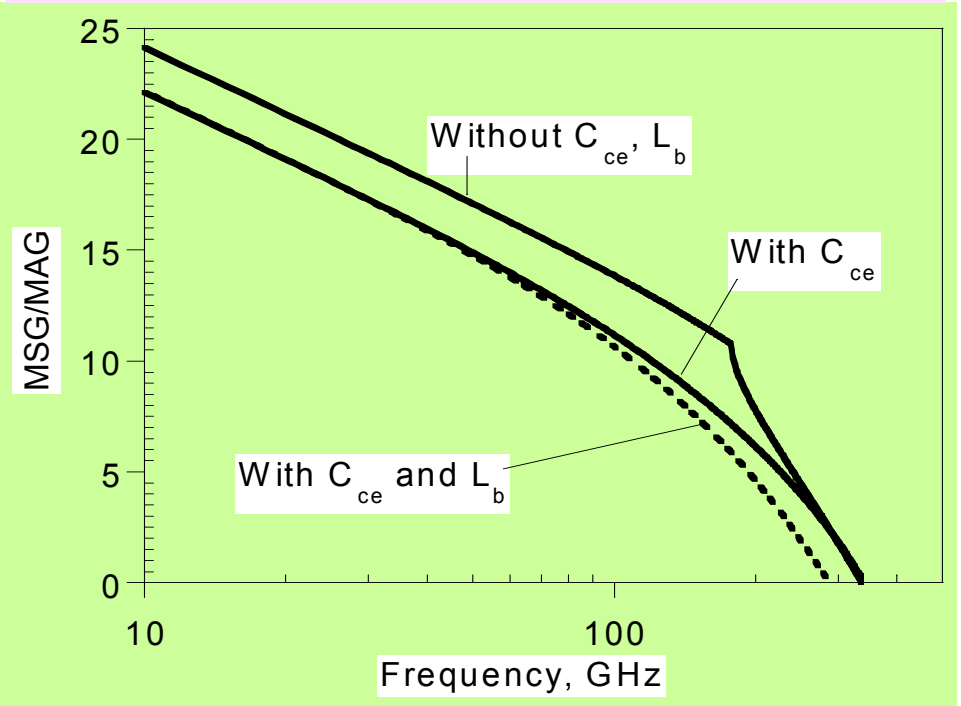
If transistor is potentially unstable, circuit gain is transistor MSG

Design for maximum gain is rare;
usually one designs for maximum saturated power or for minimum noise.
Gain is then less, discussion is beyond our scope

Common-Base Has Highest Gain, but Layout Parasitics Matter

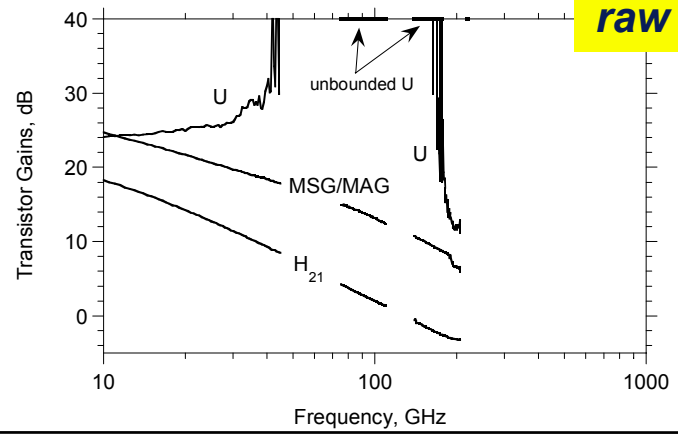




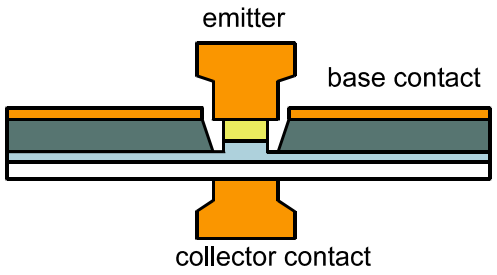


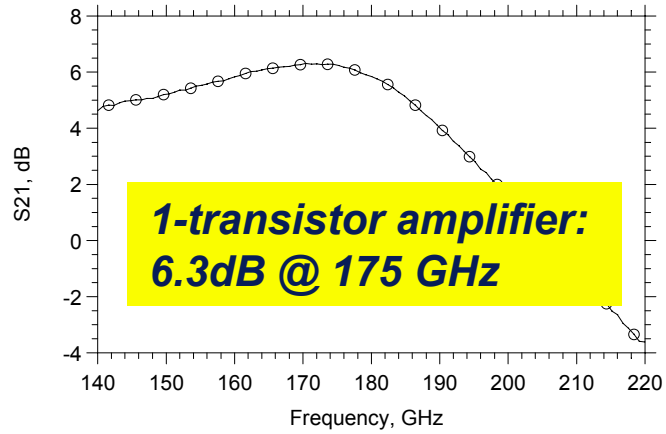
mm-wave IC results

Deep Submicron Bipolar Transistors for 140-220 GHz Amplification

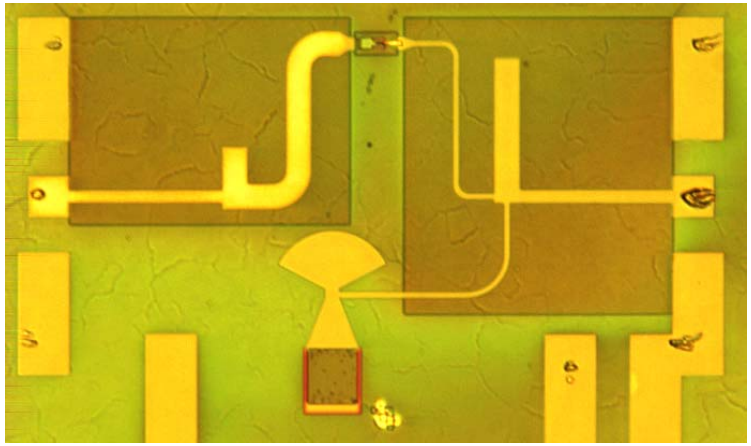


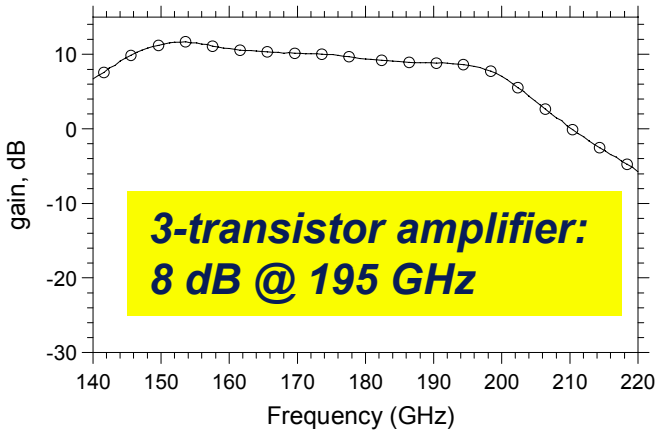
raw 0.3 μm transistor: high power gain @ 200 GHz



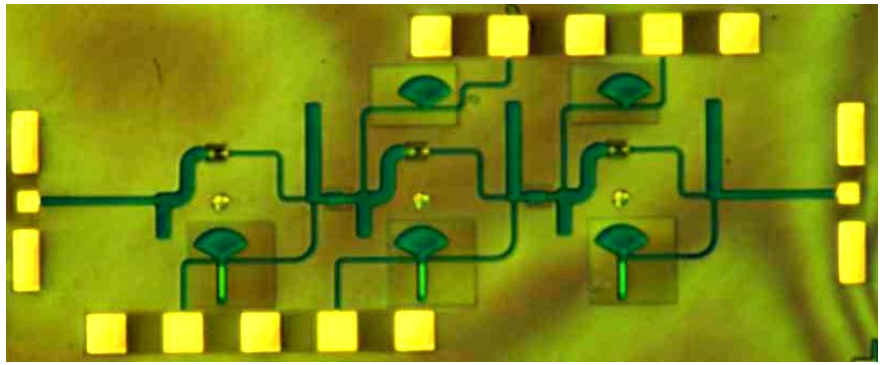


1-transistor amplifier: 6.3dB @ 175 GHz



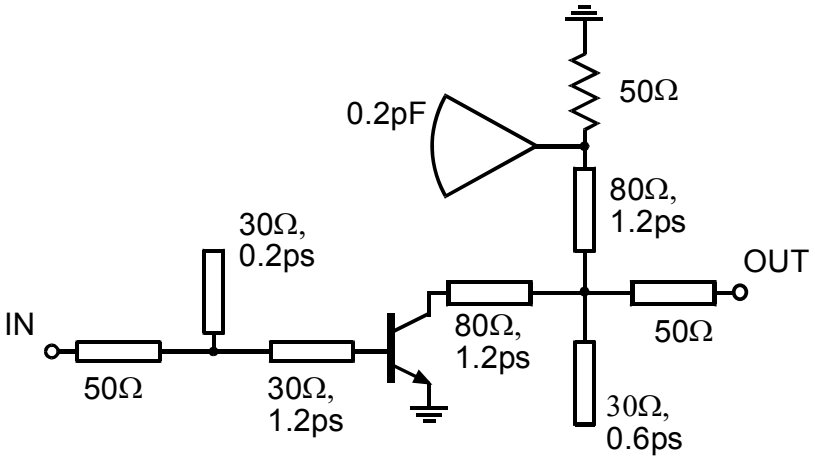


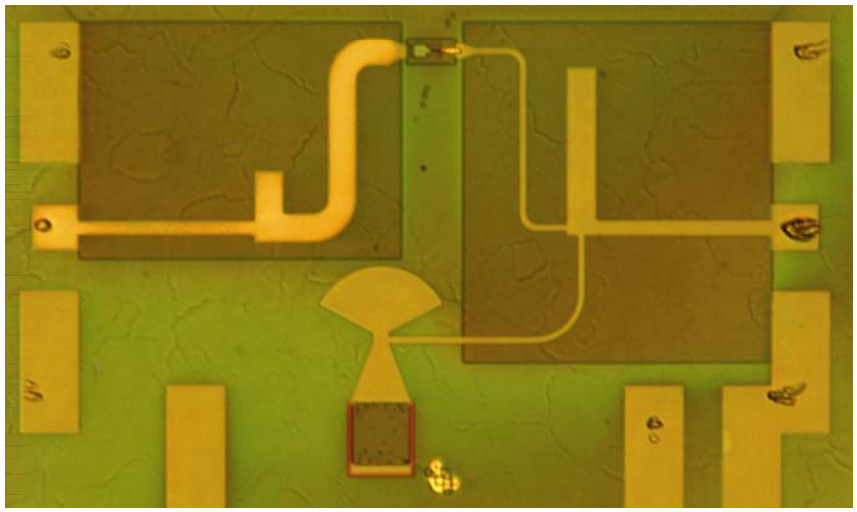
3-transistor amplifier: 8 dB @ 195 GHz

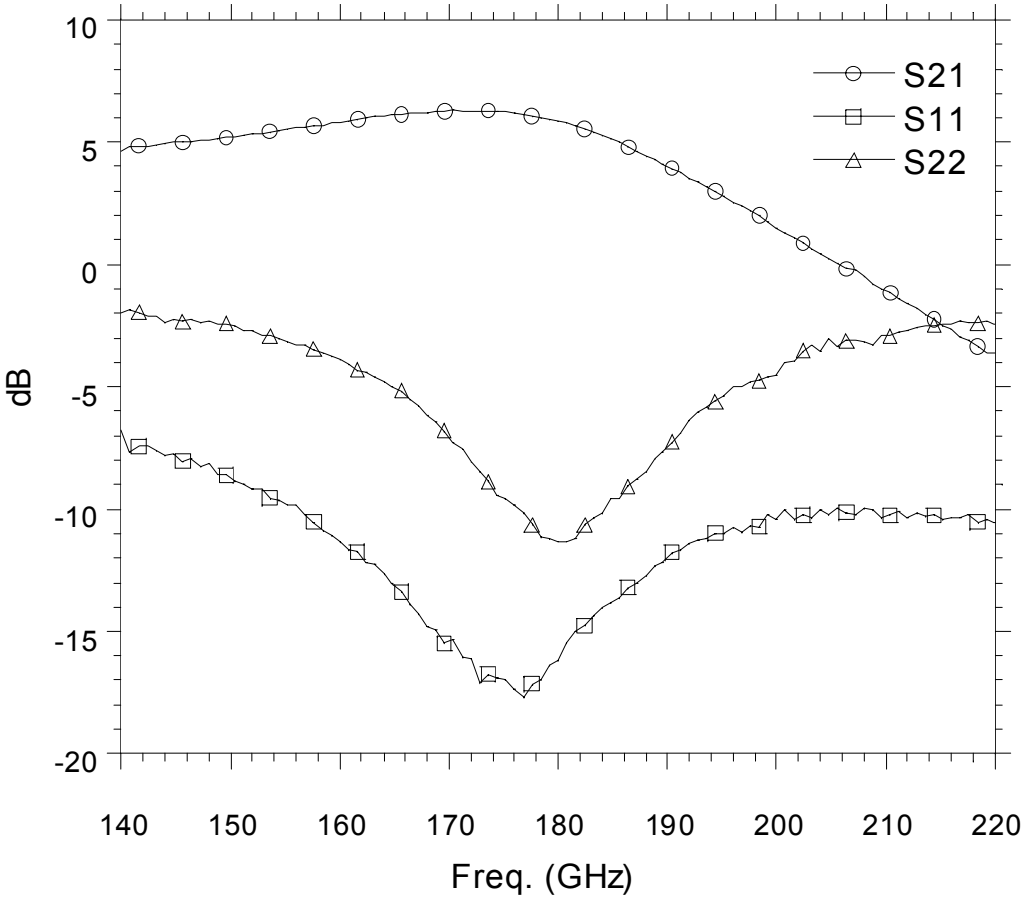


Miguel Urteaga

175 GHz Single-Stage Amplifier



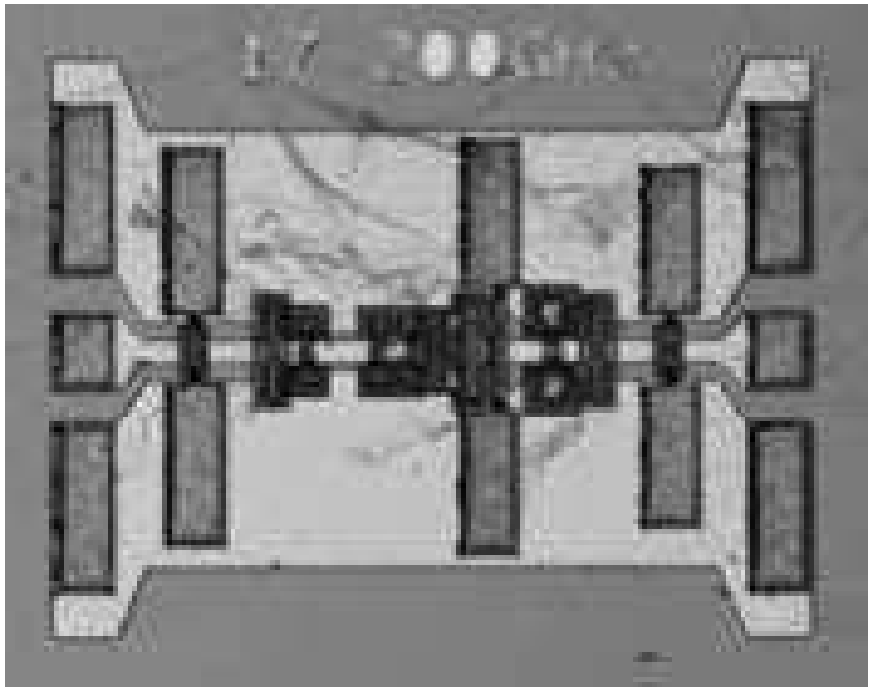


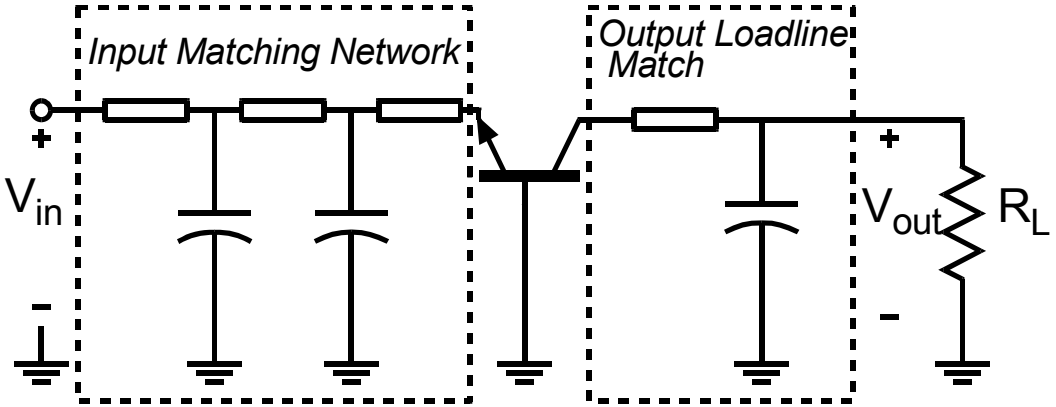


6.3 dB gain at 175 GHz

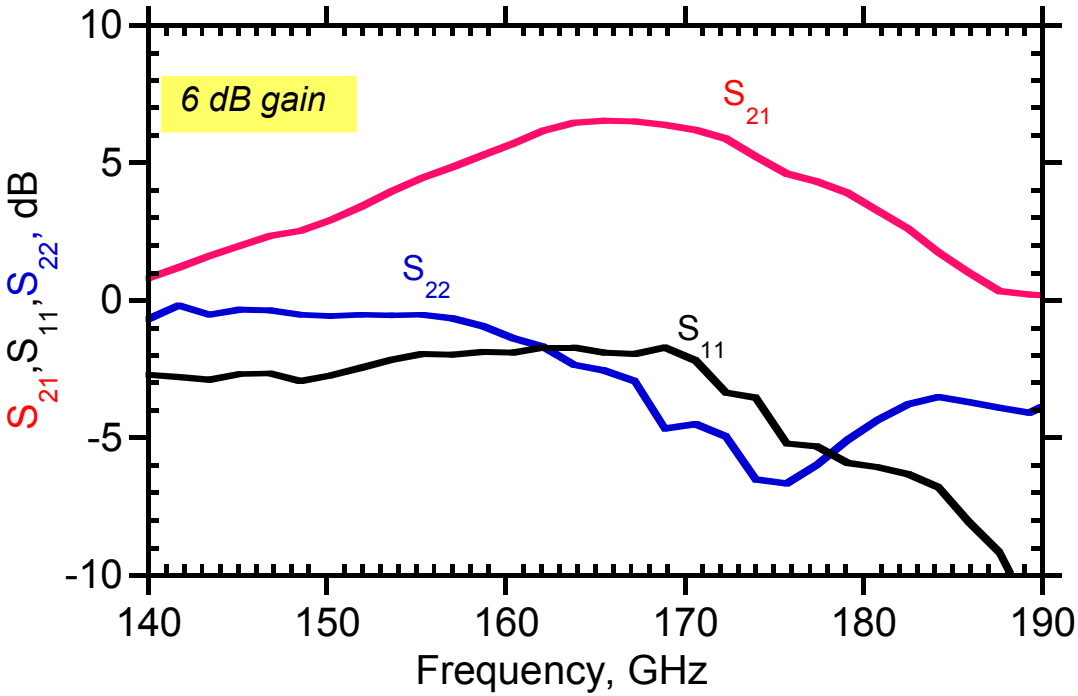
V. Paidi, Z. Griffith, M. Dahlström

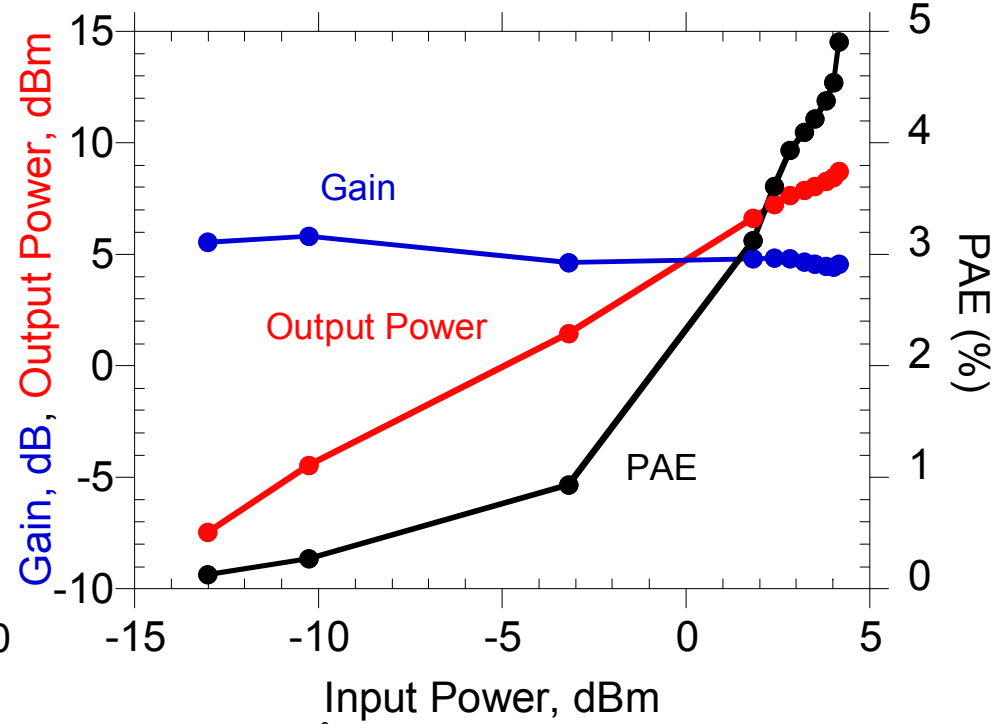
172 GHz Common-Base Power Amplifier





8.3 dBm saturated output power
4.5-dB associated power gain at 172 GHz
DC bias: Ic=47 mA, Vcb=2.1V.
transistor fmax was 300 GHz

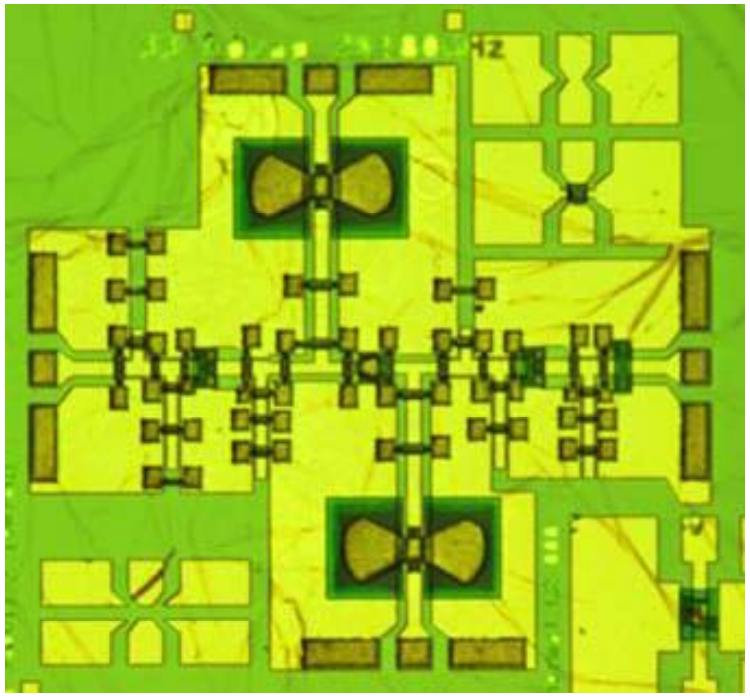




2 fingers x 0.8 um x 12 um, ~250 GHz f_τ, 300 GHz f_{max} , V_{br} ~ 7V, ~ 3 mA/um^2 current density

176 GHz Two-Stage Amplifier

V. Paidi, Z. Griffith, M. Dahlström

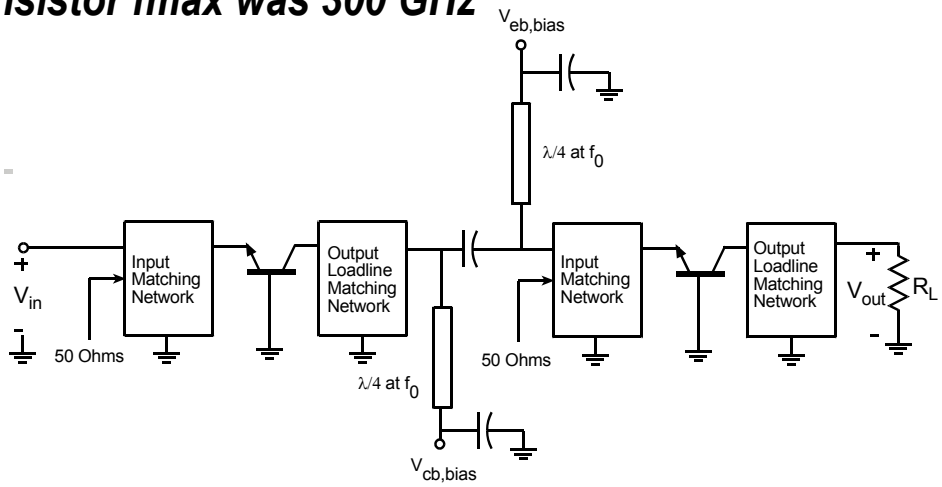


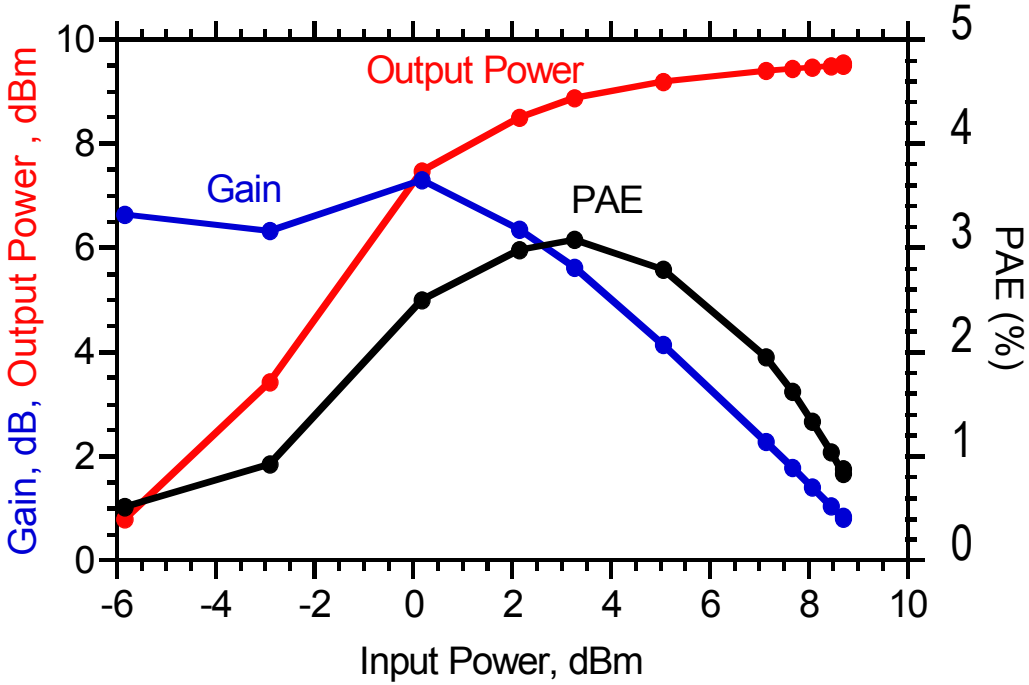
7-dB gain at 176 GHz

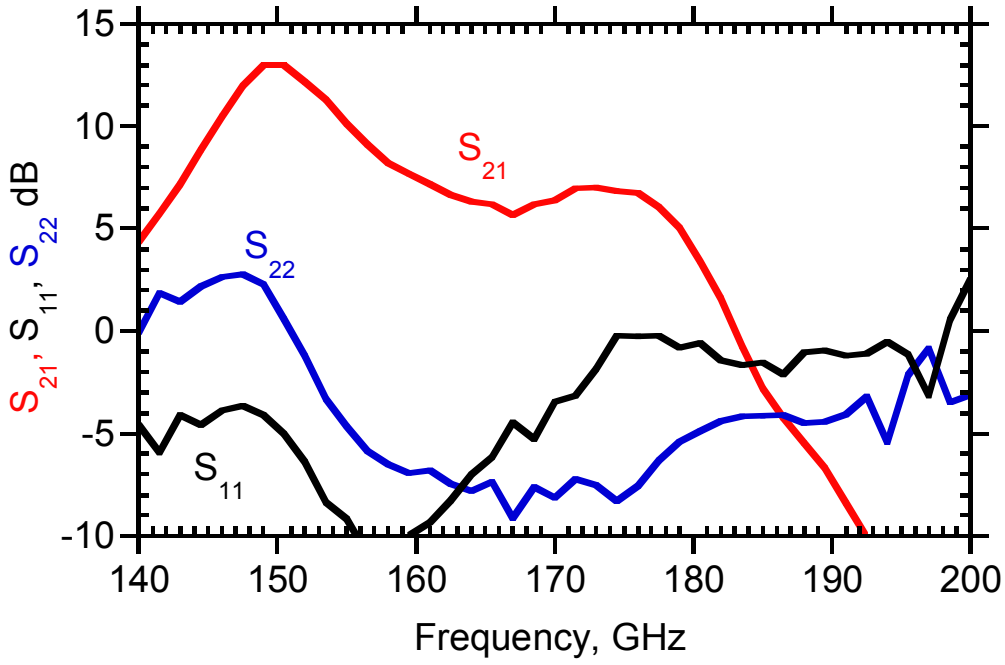
8.1 dBm output power, 6.3 dB power gain at 176 GHz

9.1 dBm saturated output power at 176 GHz

transistor fmax was 300 GHz







measurement issues

140-220 & 220-330 GHz On-Wafer Network Analysis

• HP8510C VNA,
Oleson Microwave Lab mm-wave Extenders

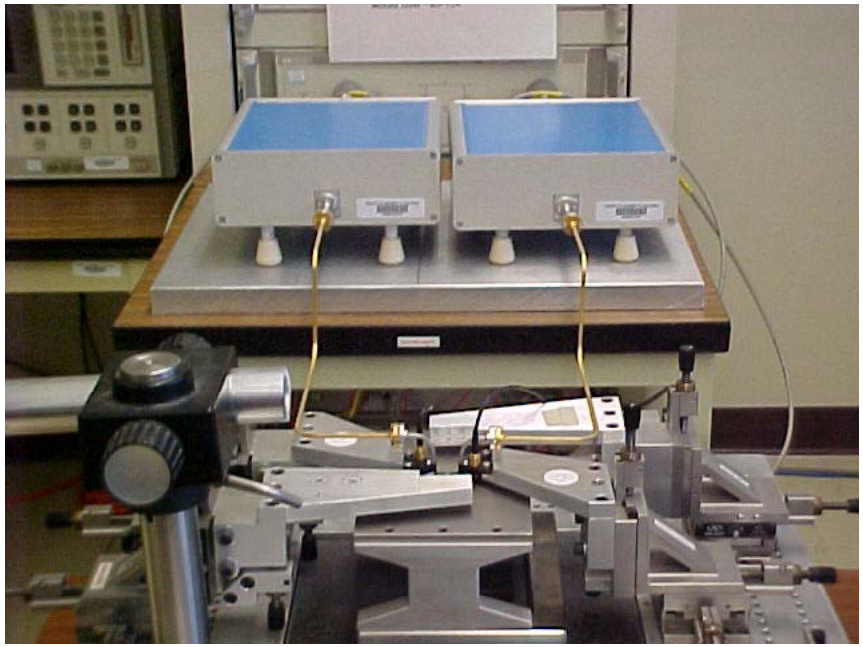
• coplanar wafer probes made by: GGB Industries, Cascade Microtech

•connection via short length of waveguide

• Internal bias Tee's in probes for biasing active devices

• 75-110 GHz set-up is similar

• DC-50 GHz set is standard coax-based system: SNR ok only to ~30 GHz

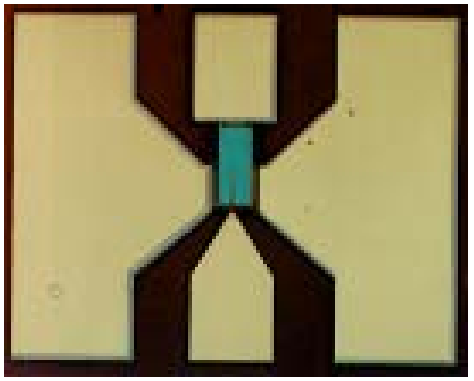


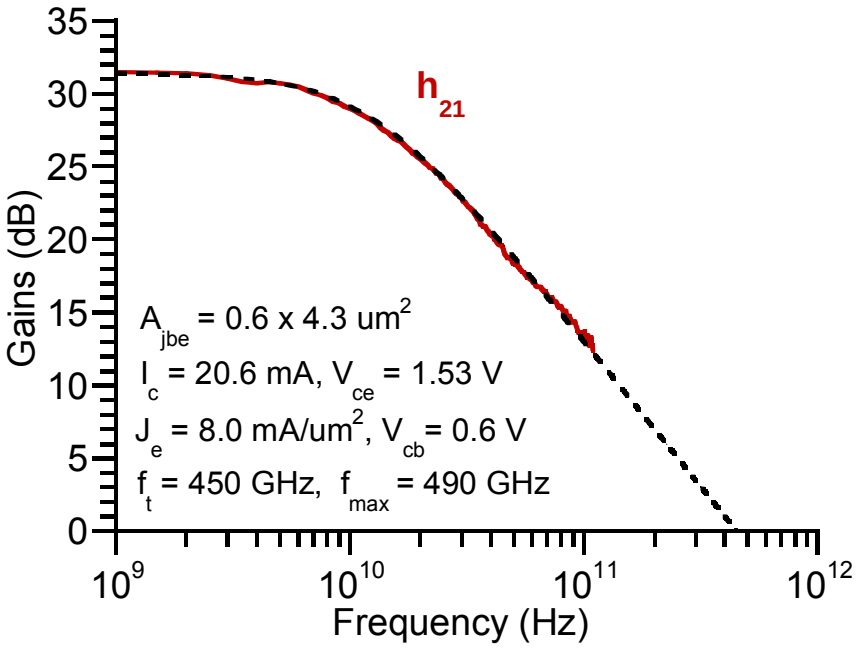
GGB Wafer Probes
330 GHz available with bias Tees

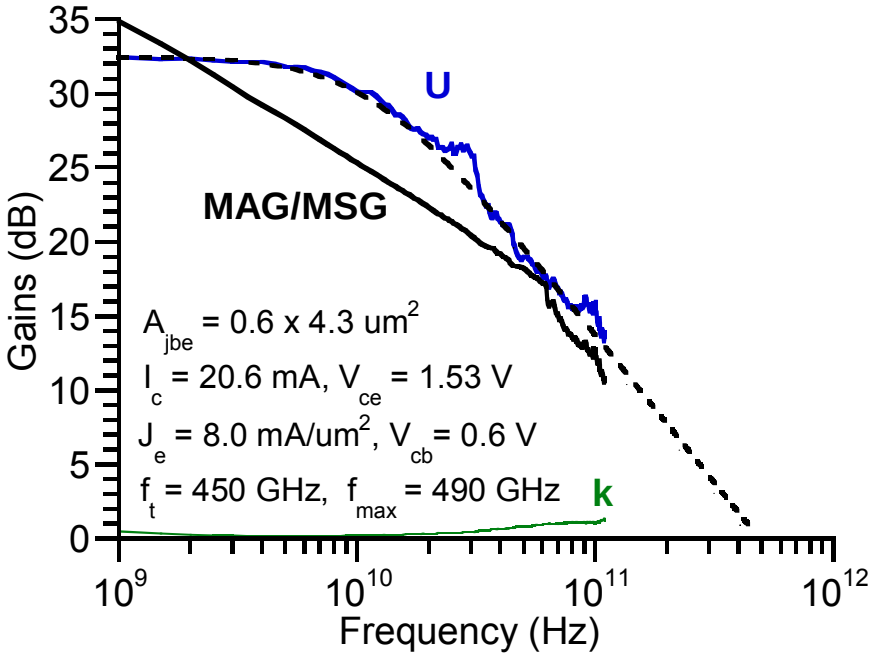
High Frequency HBT Gain Measurements : Standard Pads

Measuring wideband transistors is very hard ! Much harder than measuring amplifiers. Determining fmax in particular is extremely difficult once it exceeds 400 GHz

Standard "short pads"
must strip pad capacitance
must strip pad inductance--or ft will be too high !
cal bad above ~25 GHz due to substrate coupling
make pads small, or lift them off the InP !
cal bad above ~25 GHz due to probe coupling
use small probe pitch, use shielded (infinity) probes



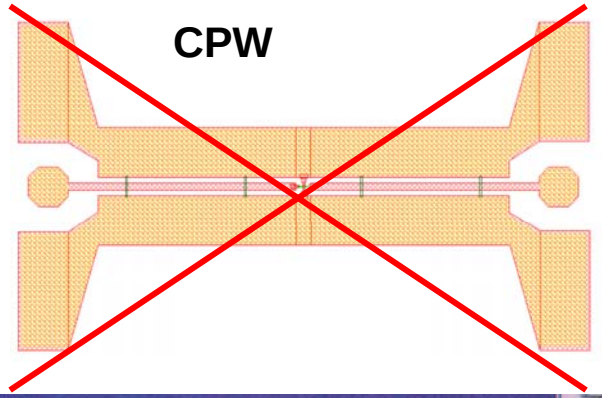


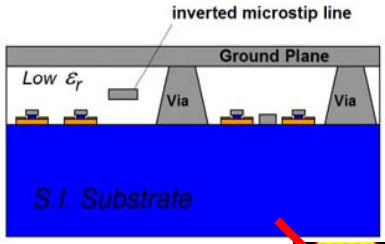


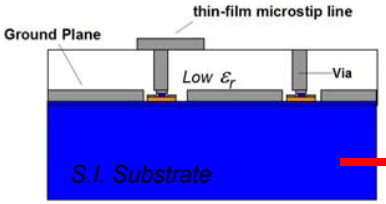
High Frequency HBT Measurements : On-Wafer LRL

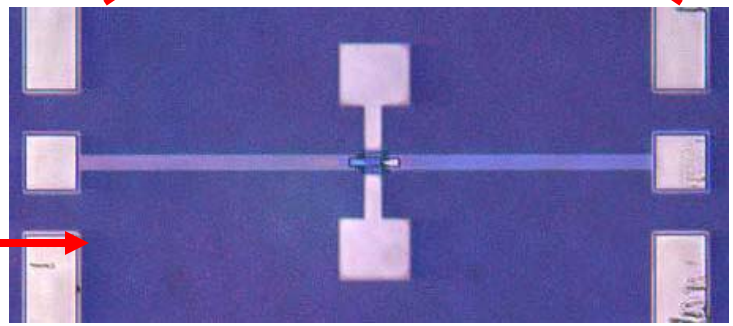
Extended Reference planes
transistors placed at center of long on-wafer line
LRL standards placed on wafer
large probe separation → probe coupling reduced
still should use the best-shielded probes available

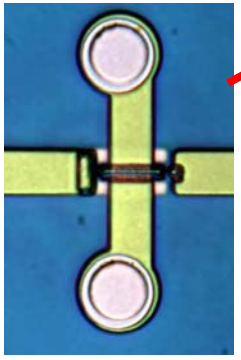
Problem: substrate mode coupling
method will FAIL if lines couple to substrate modes
→ method works very poorly with CPW lines
need on wafer thin-film microstrip lines

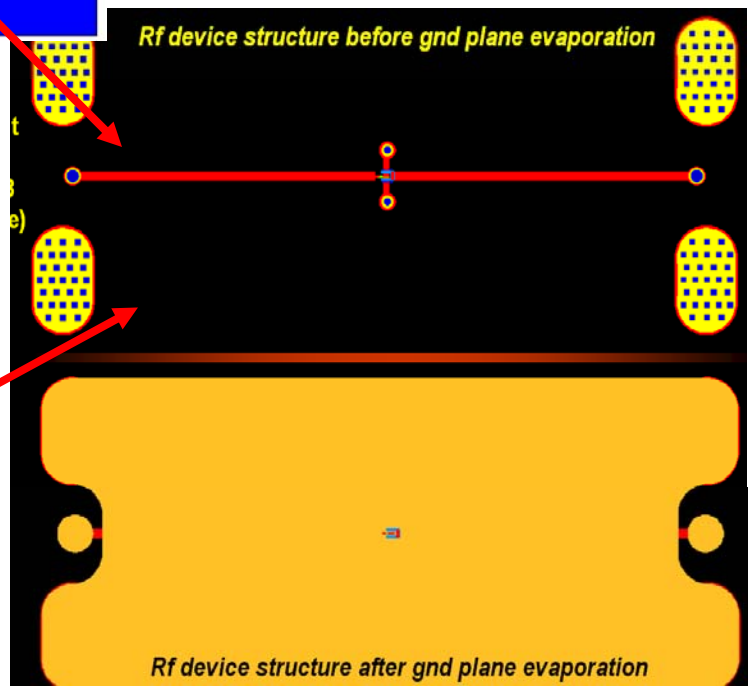


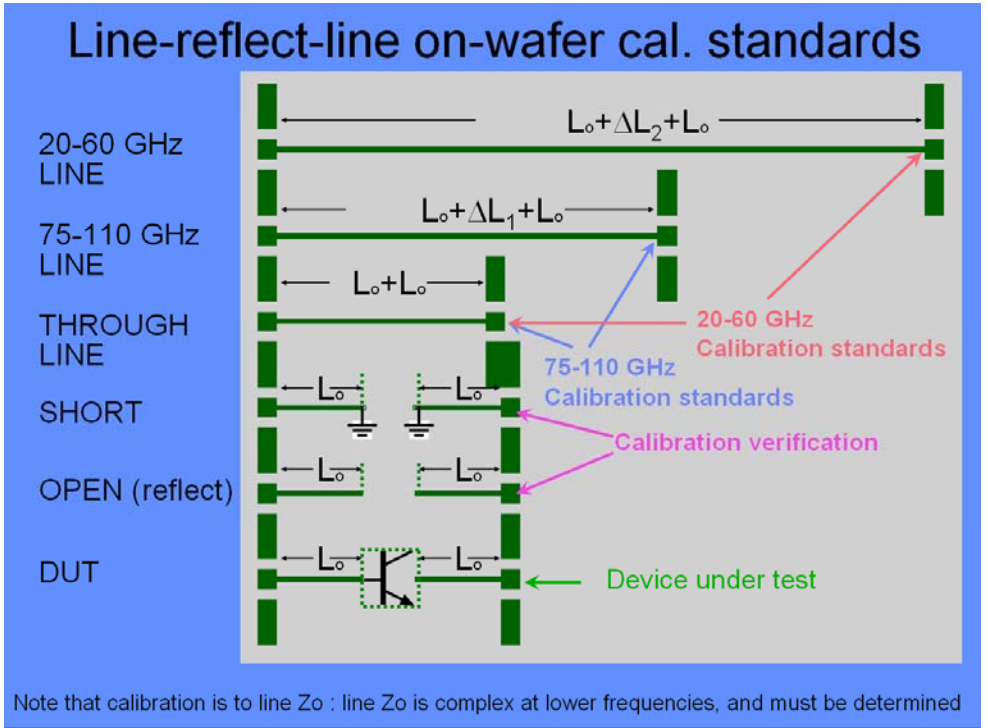




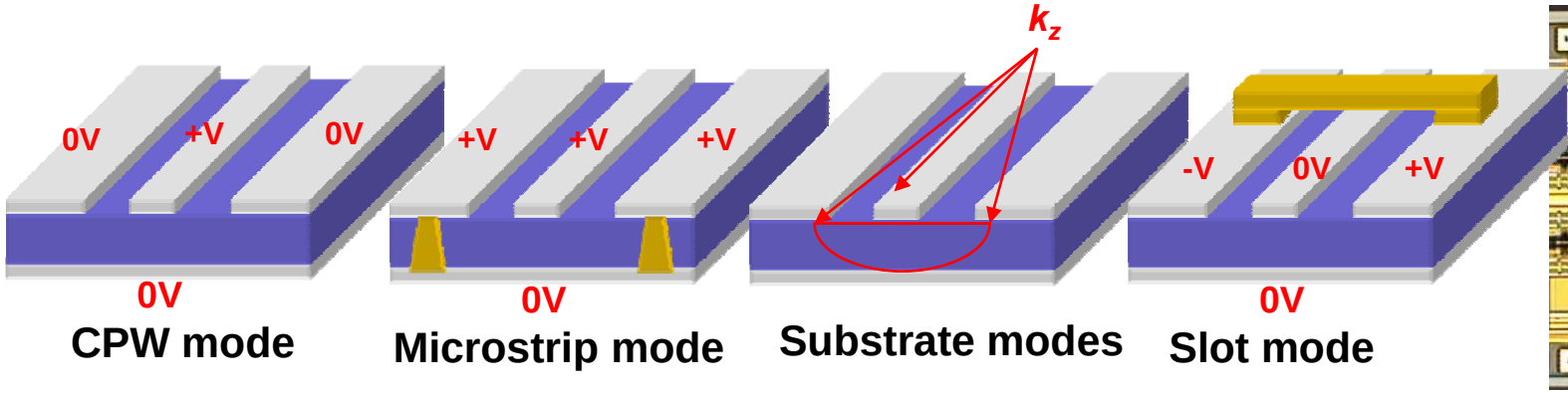


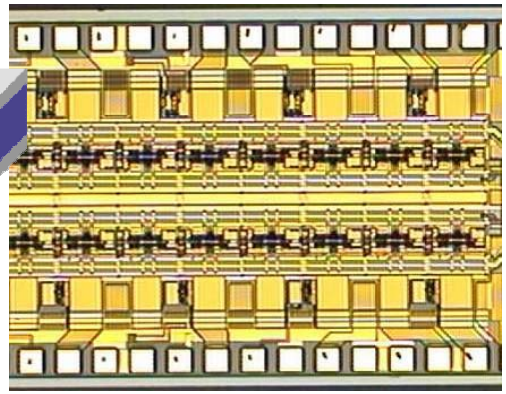






CPW has parasitic modes, coupling from poor ground plane integrity





ground straps suppress slot mode, but multiple ground breaks in complex ICs produce ground return inductance
ground vias suppress microstrip mode, wafer thinning suppresses substrate modes

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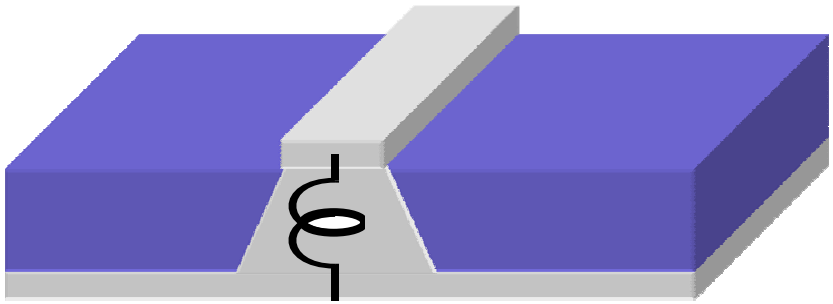
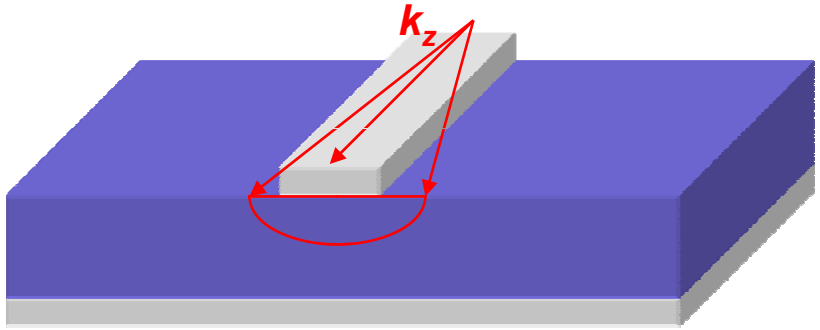
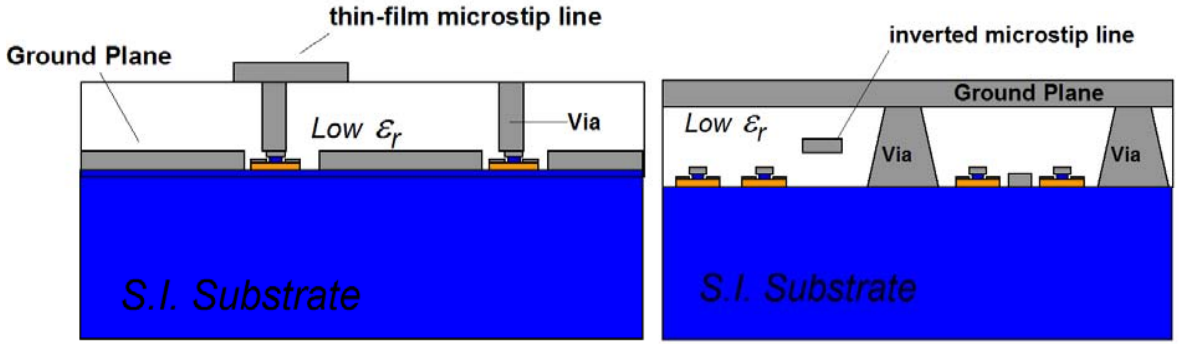
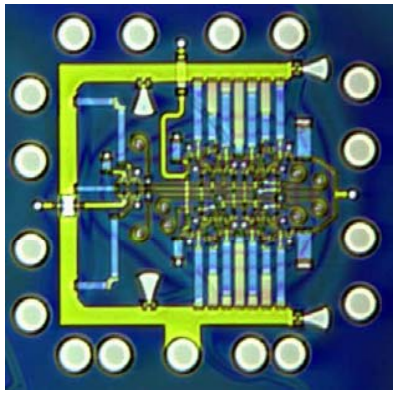
Microstrip has high via inductance, has mode coupling unless substrate is thin.

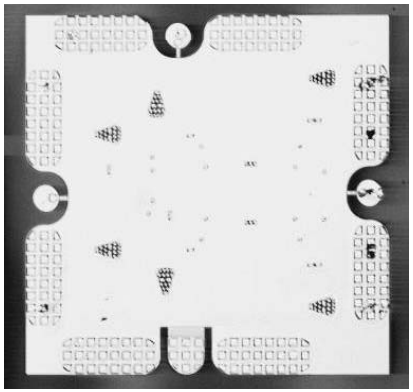




We prefer (credit to NTT) thin-film microstrip wiring, inverted is best for complex ICs







M. Urteaga, Z. Griffith, S. Krishnan

advanced fabrication processes

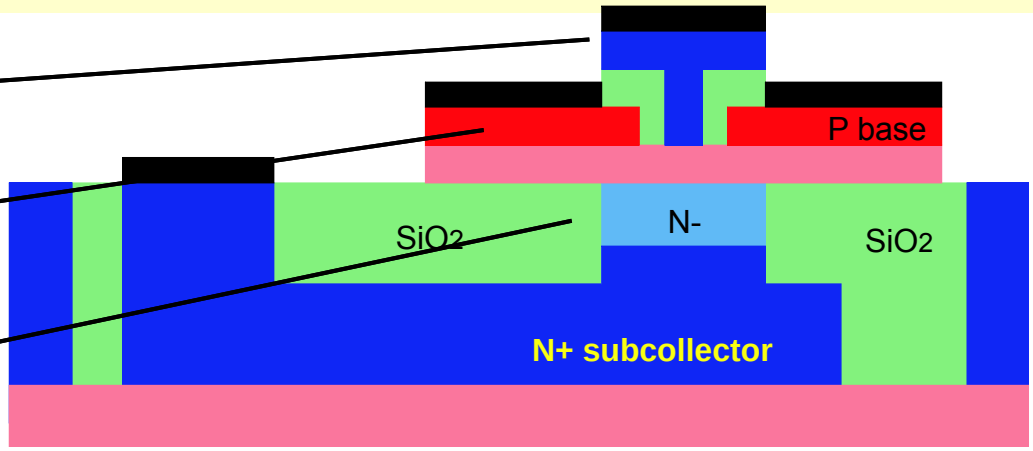
Parasitic Reduction for Improved InP HBT Bandwidth

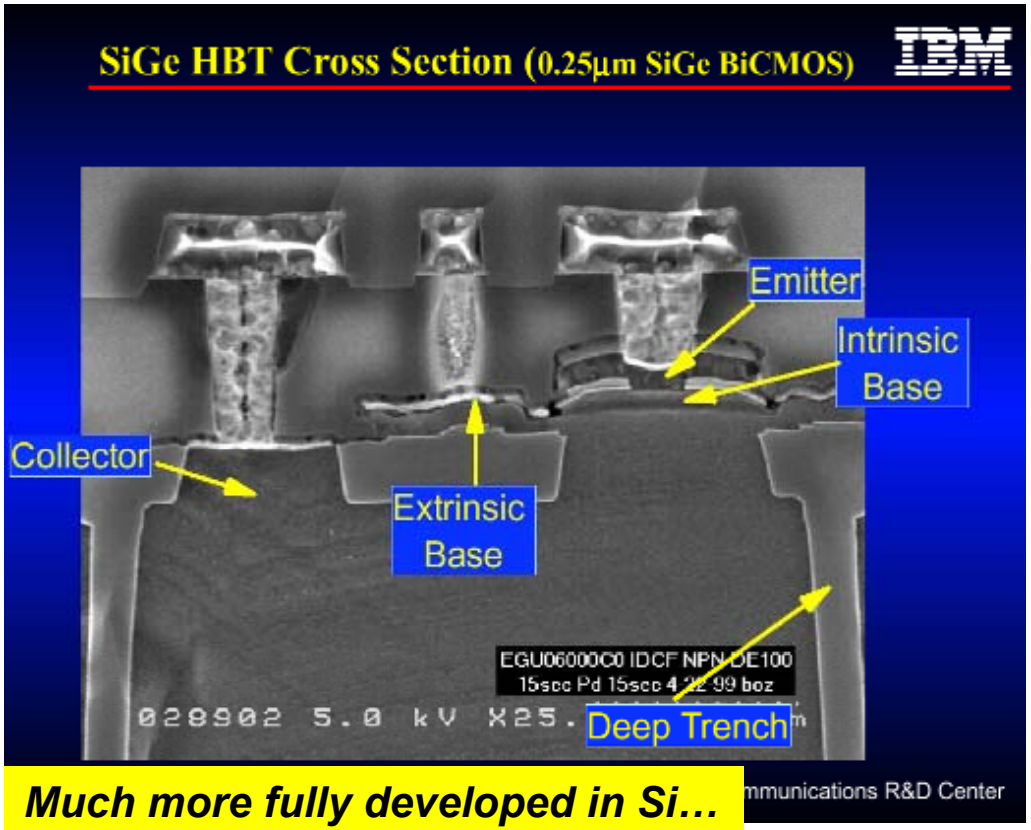
At a given scaling generation, intelligent choice of device geometry reduces extrinsic parasitics

wide emitter contact: low resistance
narrow emitter junction: scaling (low R_{bb}/A_e)

thick extrinsic base : low resistance
thin intrinsic base: low transit time

wide base contacts: low resistance
narrow collector junction: low capacitance





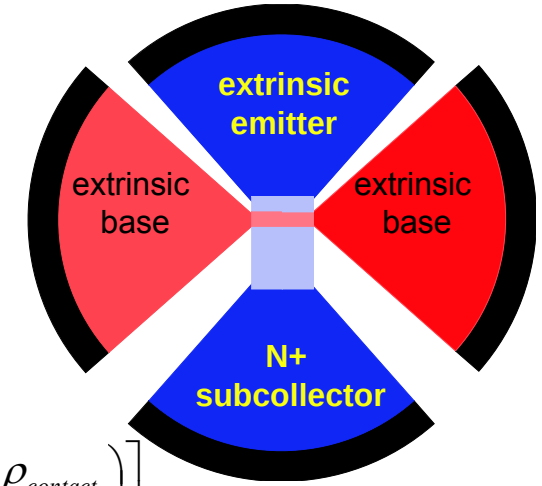
Much more fully developed in Si…

These are planar approximations to radial contacts:

$$R_{bulk} = \frac{2\rho_{bulk}}{\pi L}\ln\left(\frac{\sqrt{2}\cdot r}{W}\right)$$

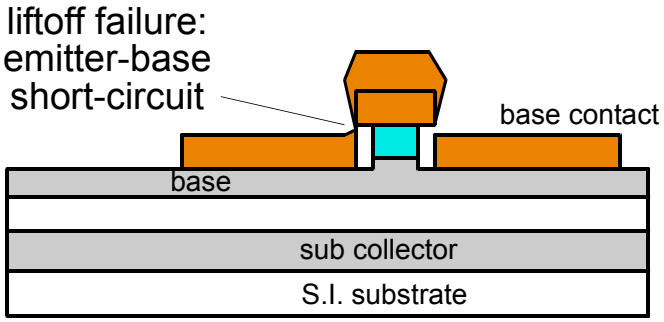
$$R_{contact} = \frac{2\rho_c}{\pi L r}$$

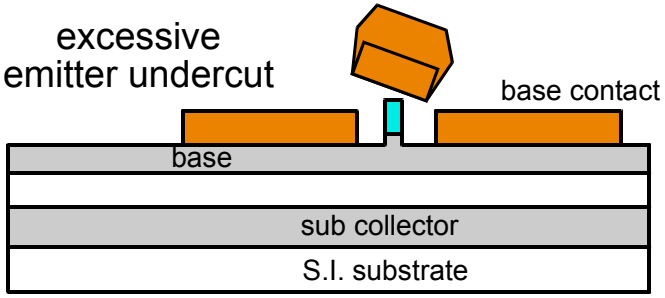
$$R_{\text{total,min}} = \frac{2\rho_{bulk}}{\pi L}\left[1.34 + \ln\left(\frac{\rho_{contact}}{W\rho_{bulk}}\right)\right]$$

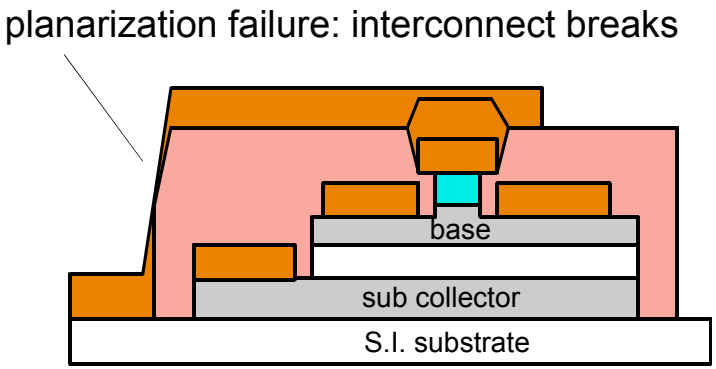


→ ***greatly reduced access resistance***

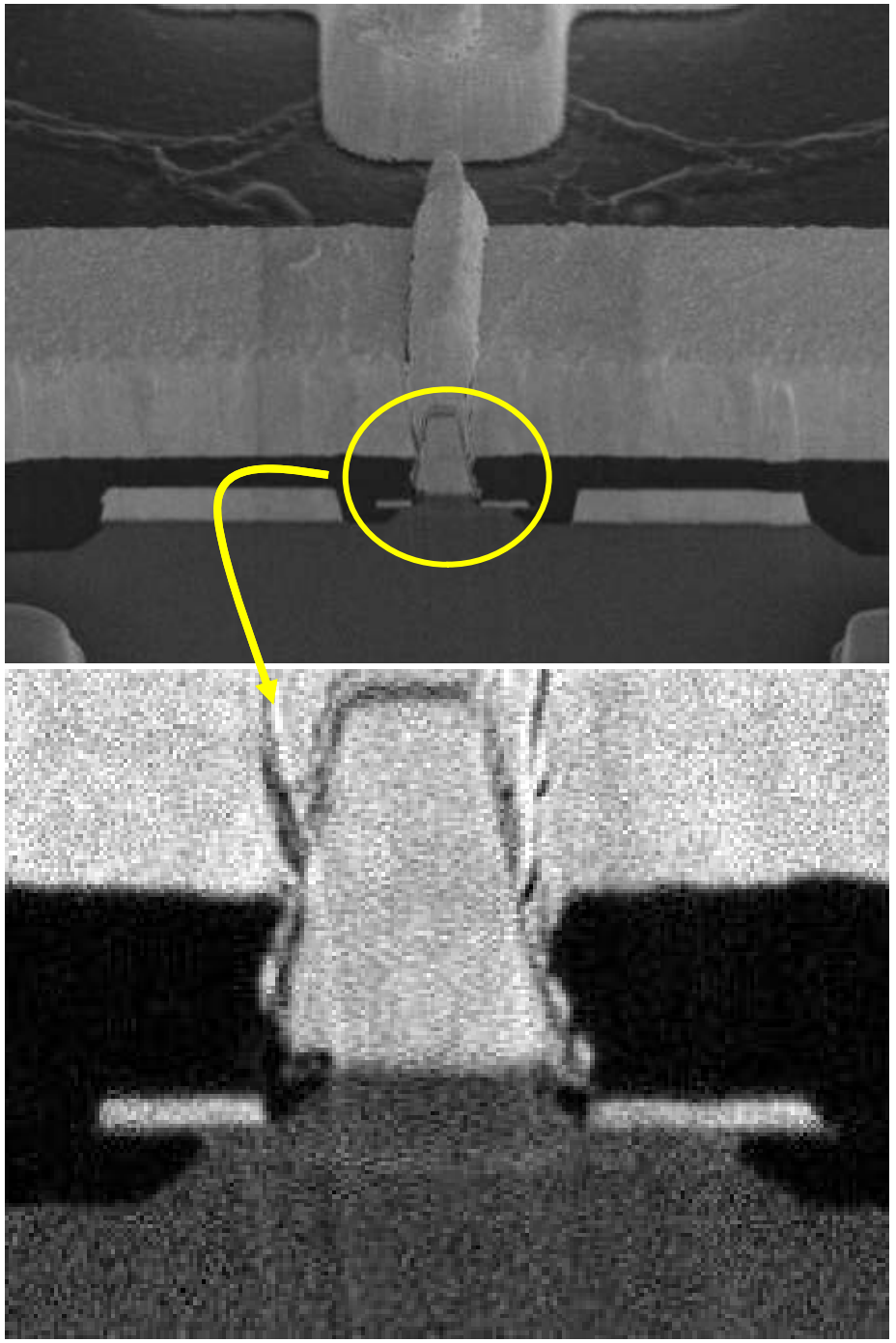
Yield & Scaling Problems: Liftoff, Undercut, Planarity



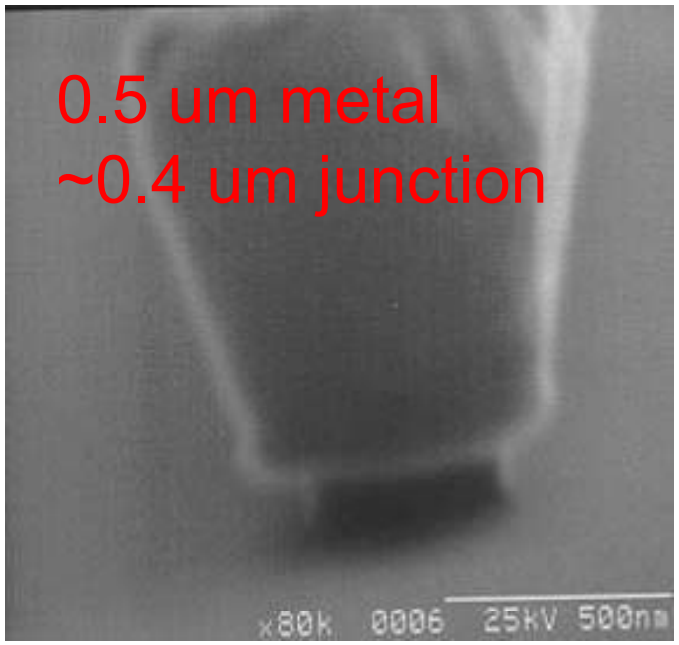


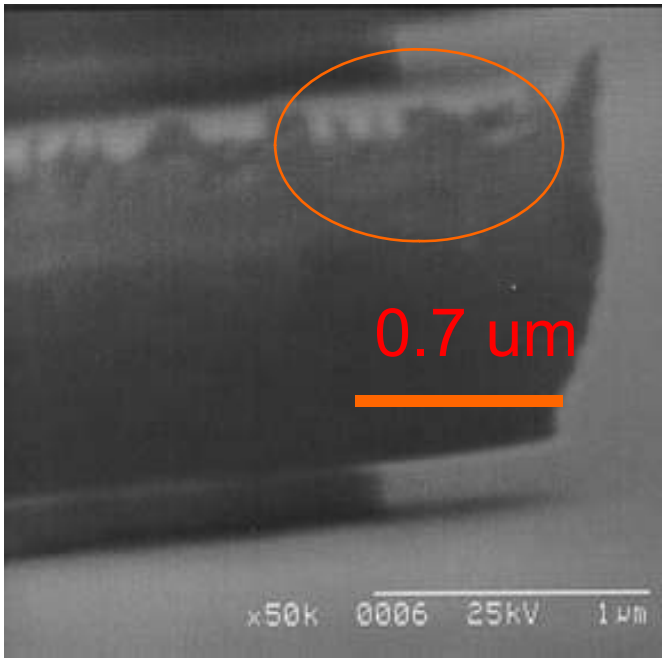


Yield quickly degrades as emitters are scaled to submicron dimensions



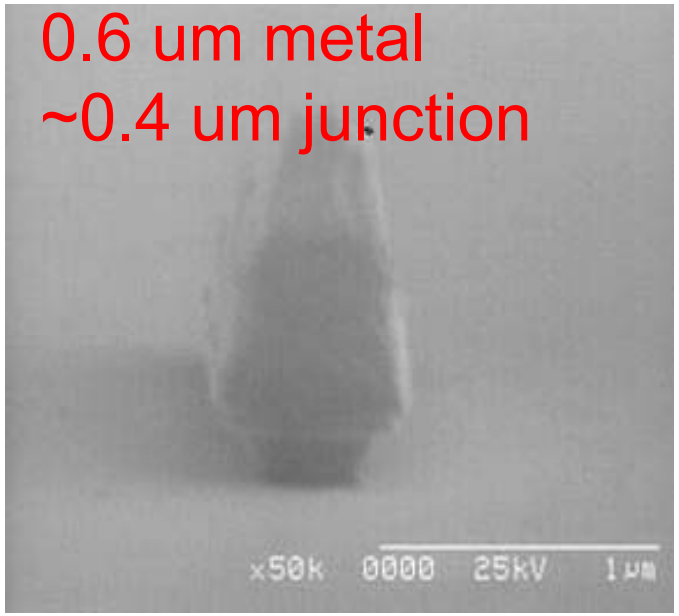
Controlling Emitter Undercut: Wet-Etch Mesa Process

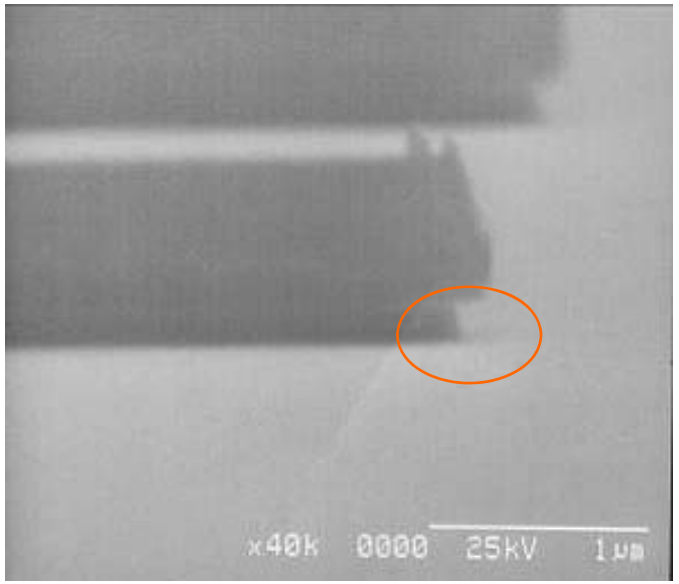




InP

Front and side views





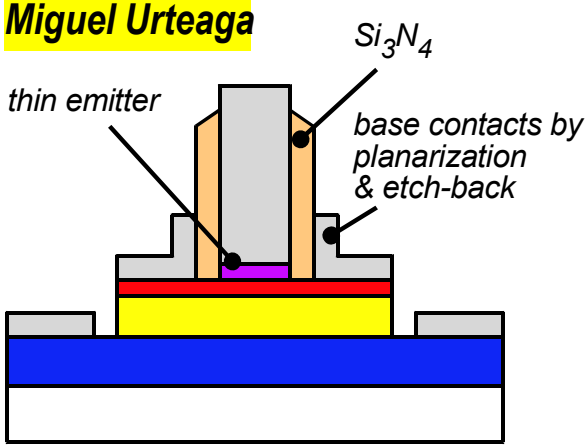
InAlAs

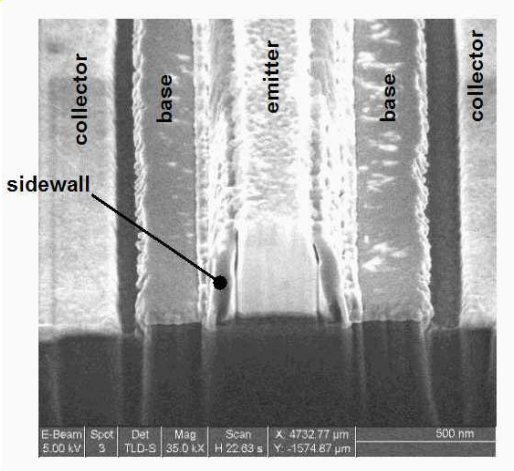
Front and side views

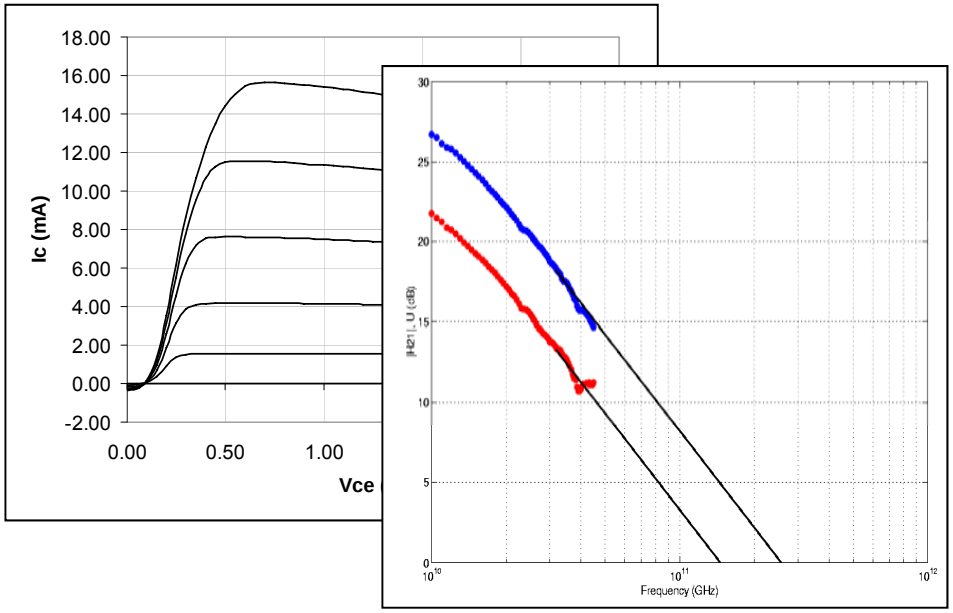
Smaller emitters → lower yield. Need better fabrication process

Manufacturable Emitter Dielectric Sidewall Processes

First-Generation: UCSB and Rockwell Scientific
Miguel Urteaga



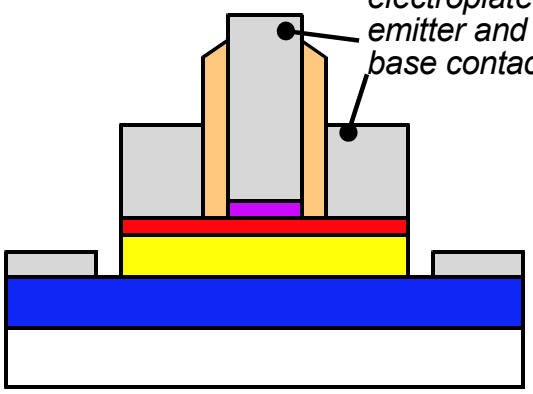


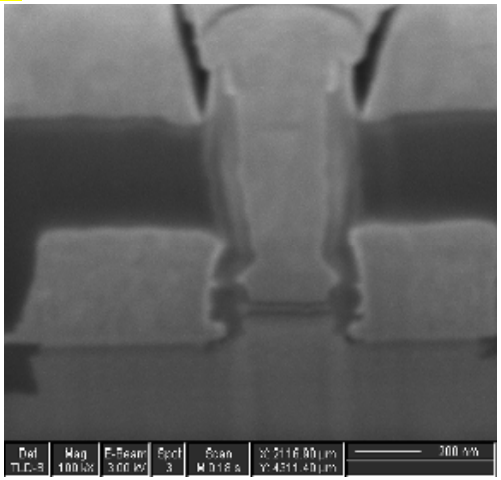


Urteaga, Rodwell , Pierson, Rowell , Brar, Nguyen, Nguyen: UCSB, RSC, GCS

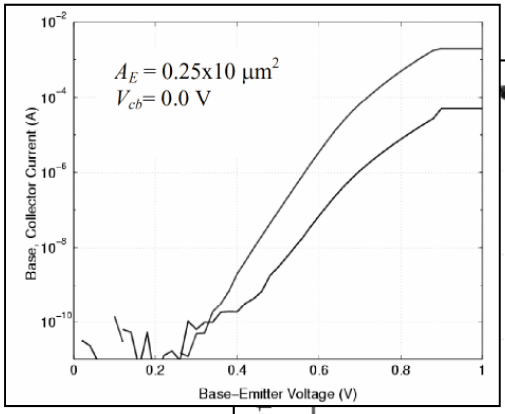
266 GHz f_t, 133 GHz f_{max}, , C_{cb}/I_c=0.4 ps/V

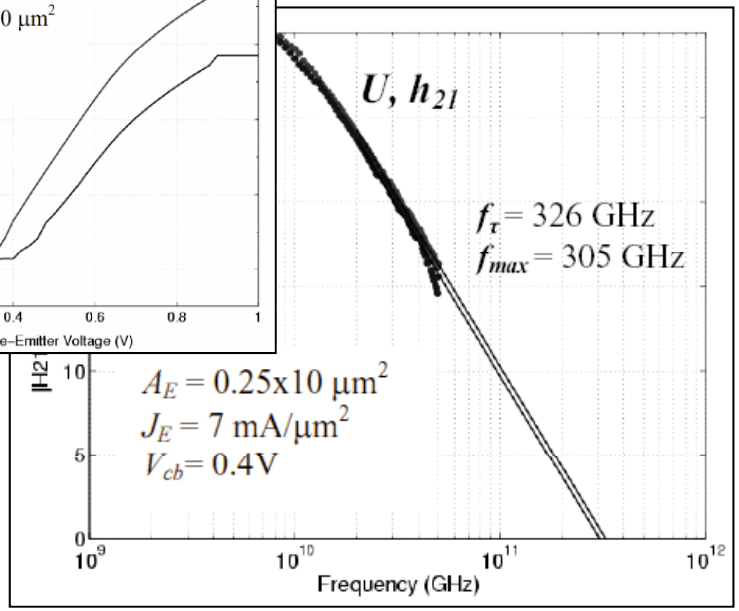
2nd-Generation: Rockwell Scientific
Miguel Urteaga, Petra Rowell





250 nm emitter

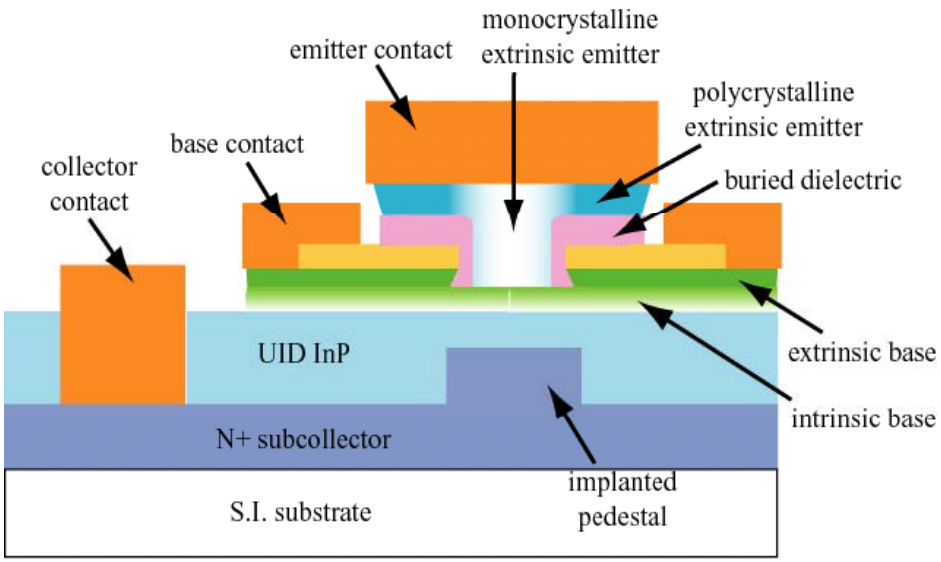


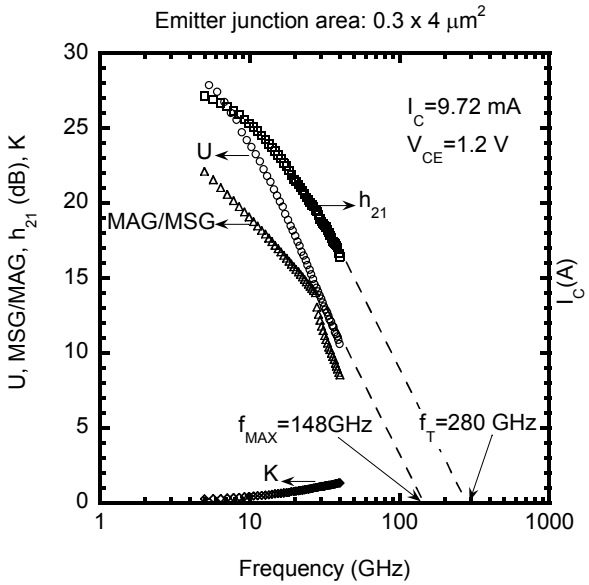


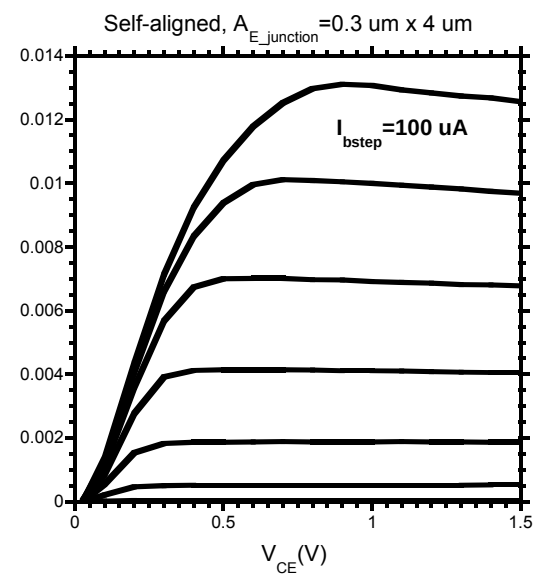
Urteaga, Rowell, Pierson, Brar: RSC

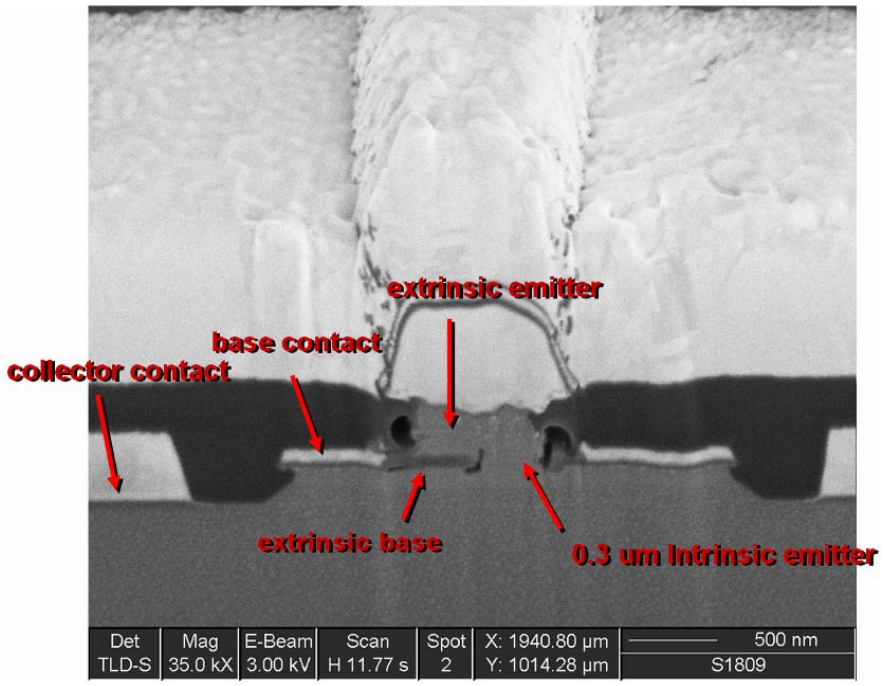
1st-Generation Polycrystalline Extrinsic Emitter

D. Scott, Y. Wei







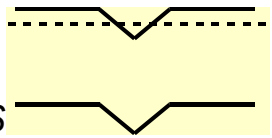


Approach

Wide emitter contact for low emitter access resistance
Thick extrinsic base for low base resistance
Self-aligned refractory base contacts

Enabling Technology

Low-resistance polycrystalline InAs
In-band Fermi-level pinning eliminates barriers

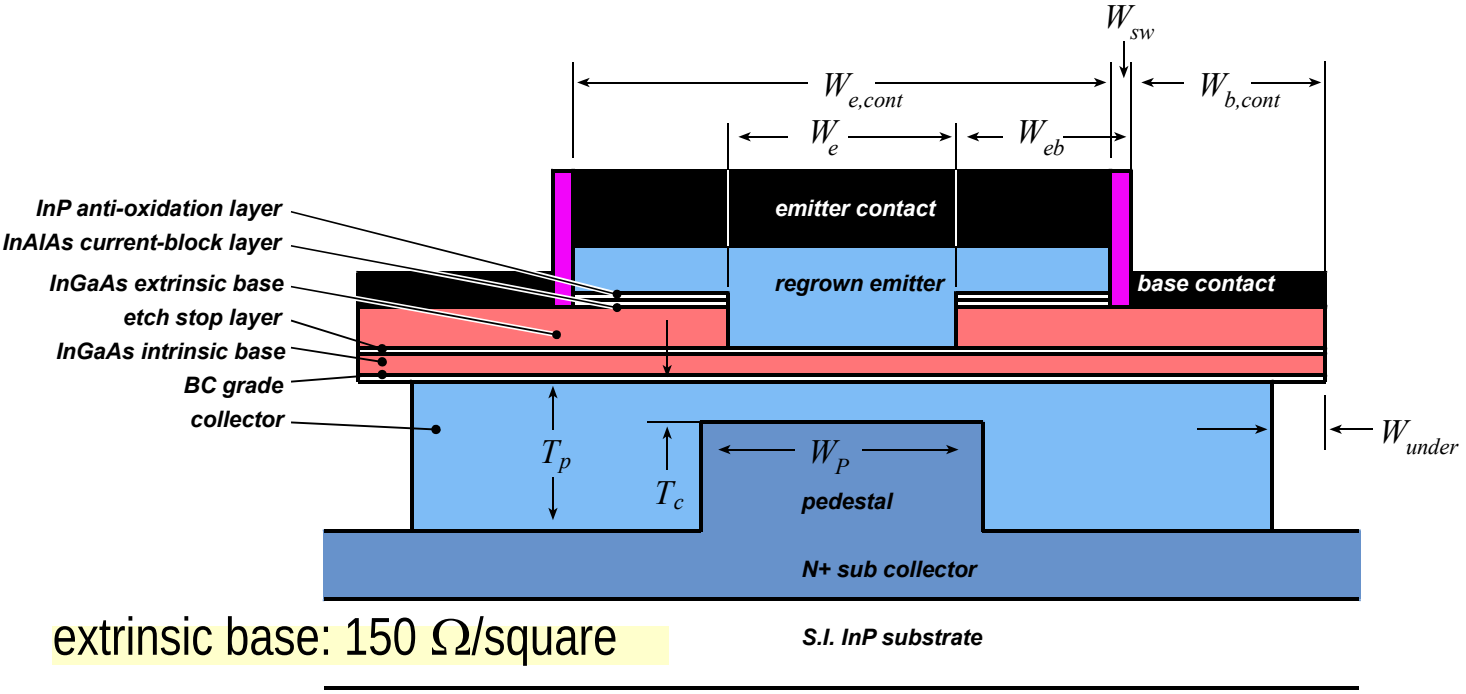


Challenges

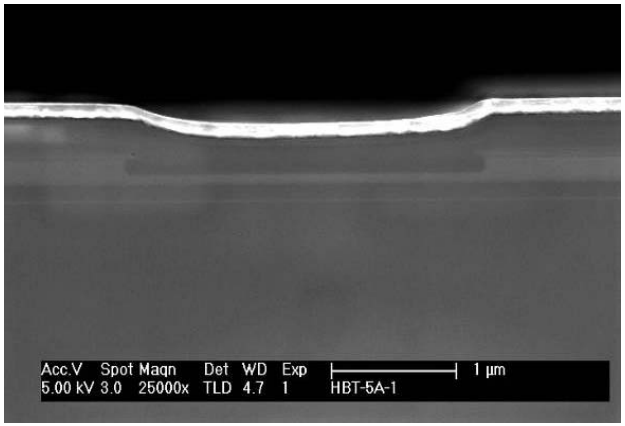
Very complex process
Hydrogen passivation
Resistance of Refractory contacts

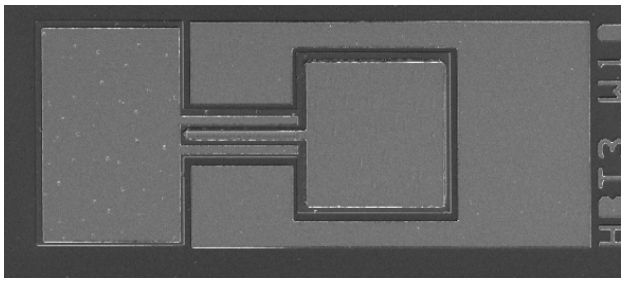
2nd-Generation Epitaxial Extrinsic Emitter

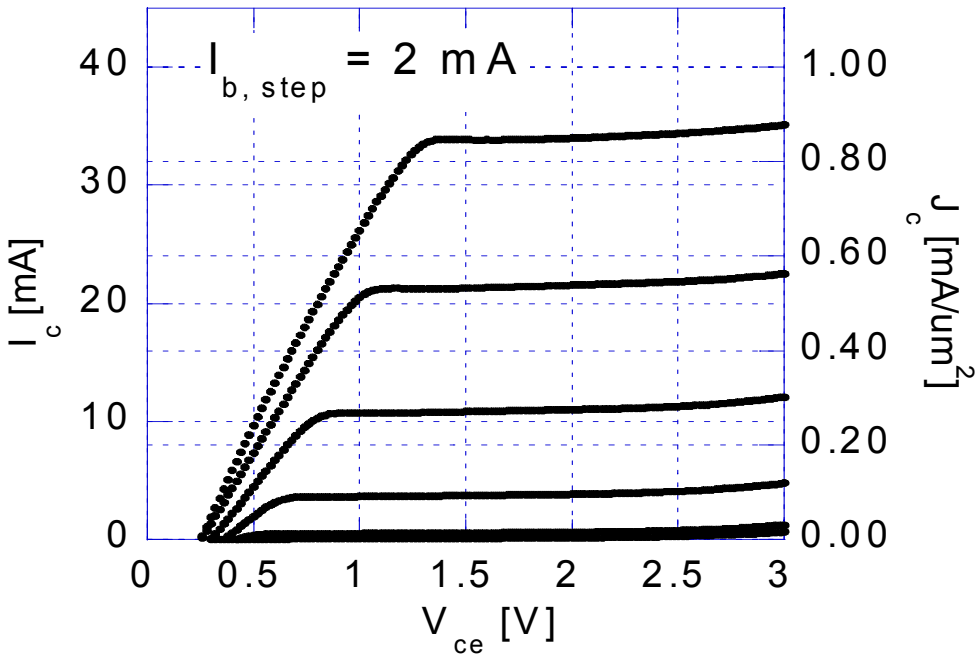
C. Kadow

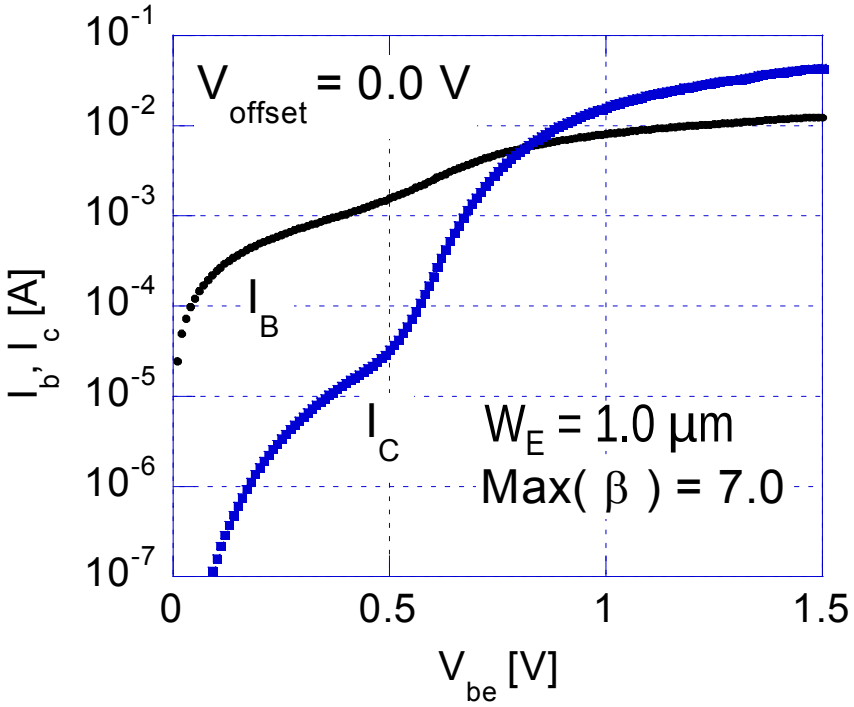


extrinsic base: 150 Ω/square



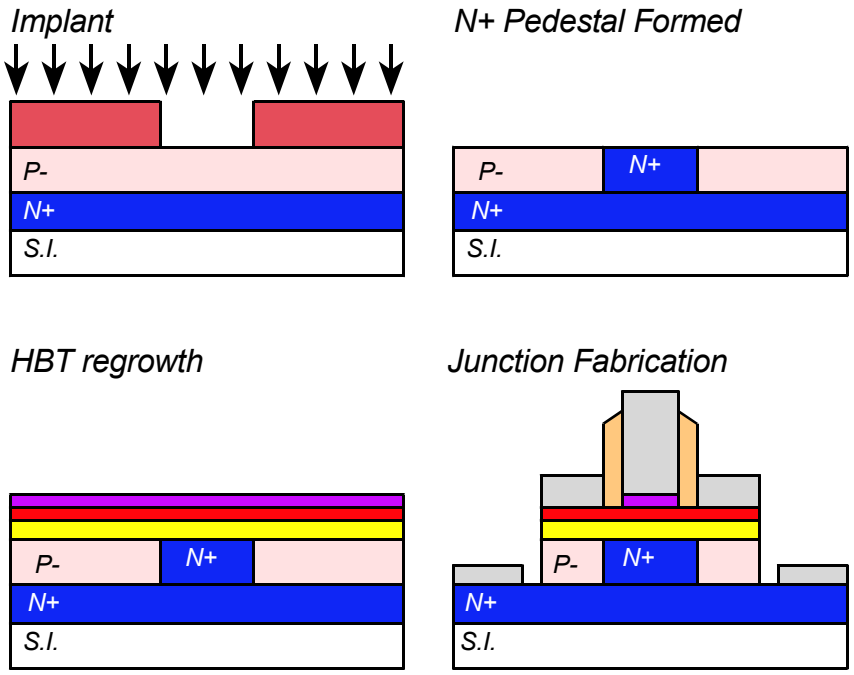


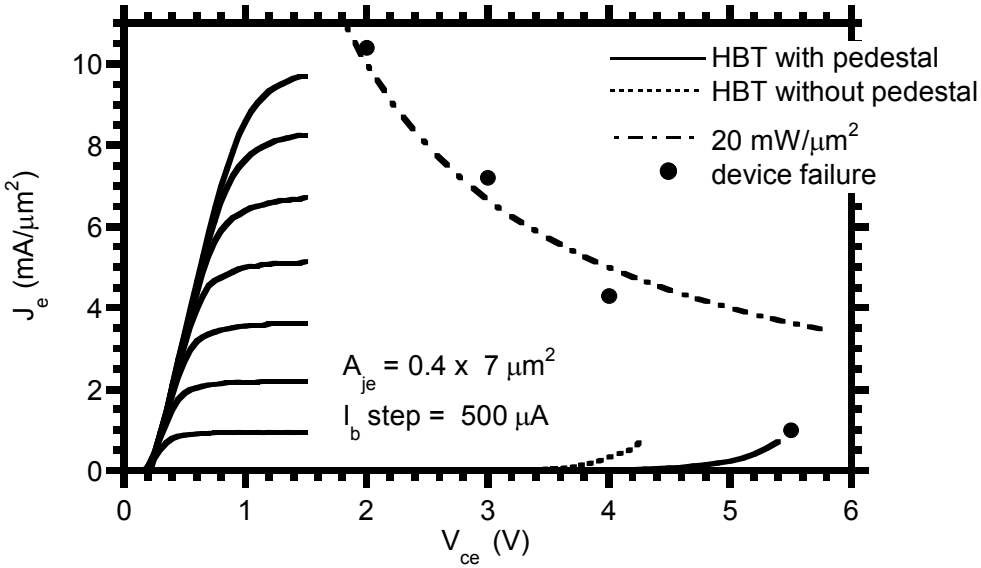




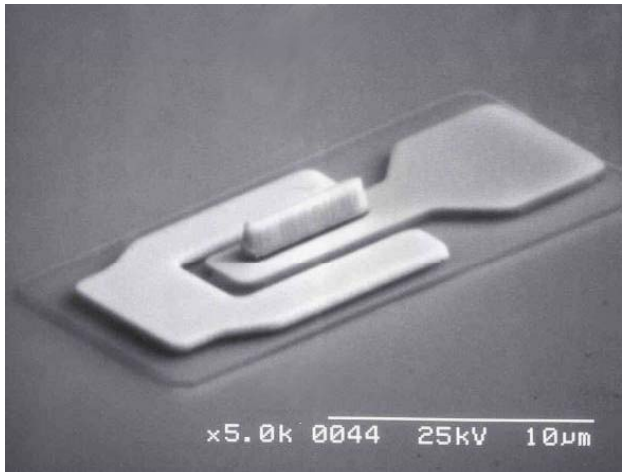
Y. Dong

1st-Generation Collector Pedestal Implant



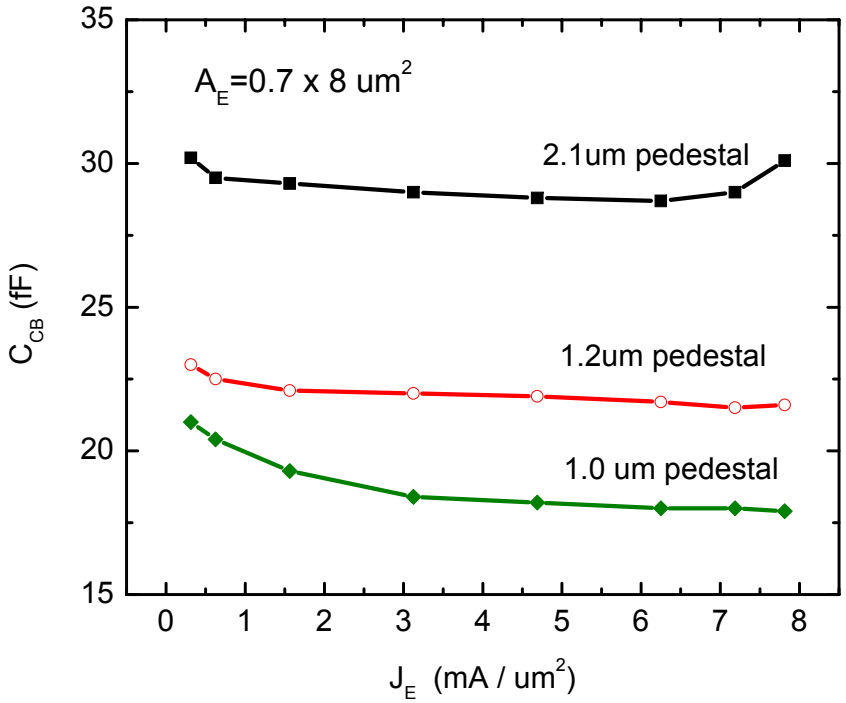


Good DC characteristics
5.4 V breakdown with a 90 nm thick collector



Reduced extrinsic Ccb

Reduced thermal resistance



~2:1 reduction in collector base capacitance

Pedestal: Projected Performance @ 300 nm

$\rho_{c,emitter} = R_{ex} A_E = 6\,\Omega\text{-}\mu\text{m}^2$

$\rho_{c,base} = 10\,\Omega\text{-}\mu\text{m}^2$

$J_e = 15\ \text{mA}/\mu\text{m}^2$

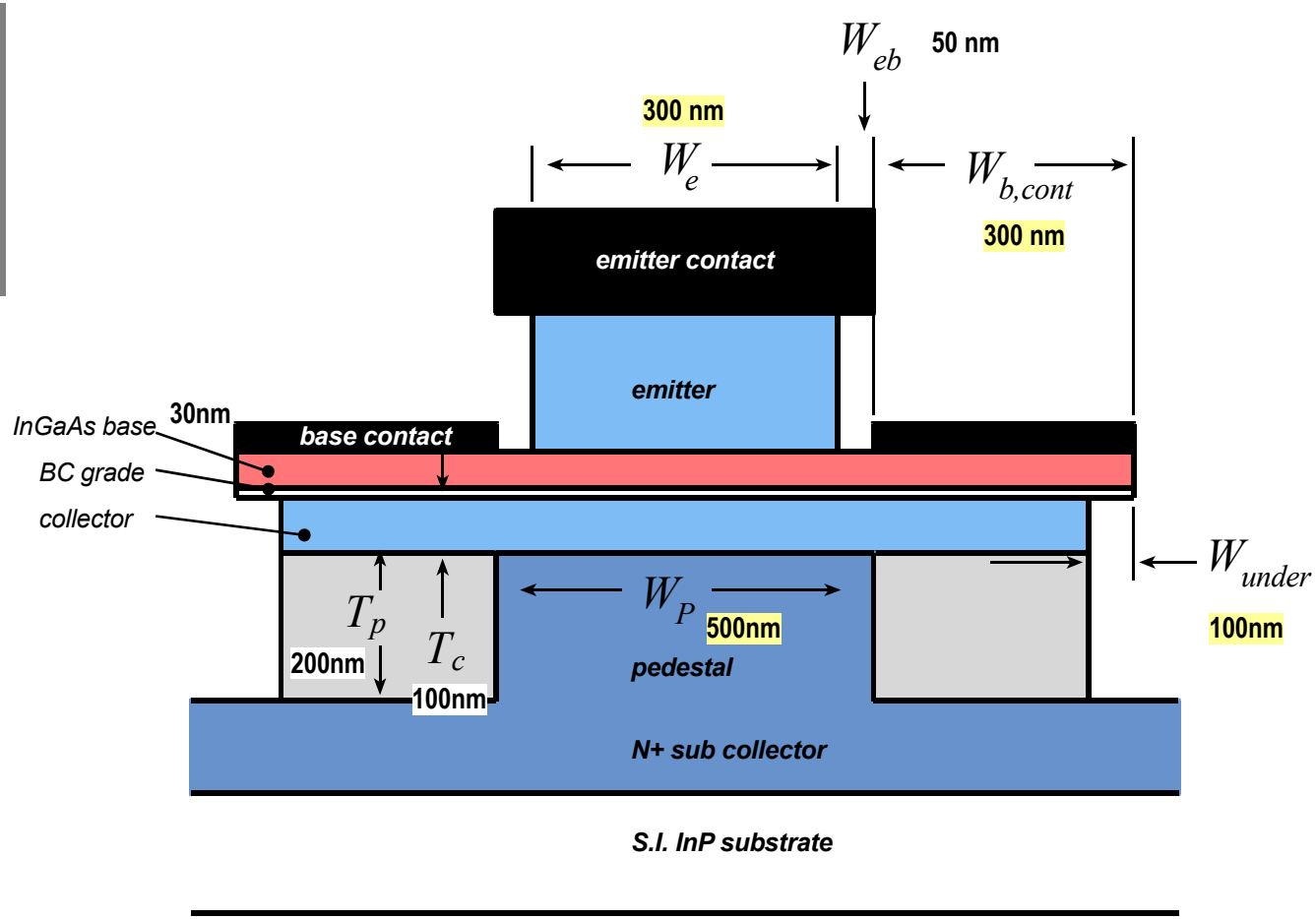
0.3 ps wiring delay on collector bus

$f_{\text{clock (divider)}} \cong 275\,\text{GHz}$

$f_\tau = 530\,\text{GHz} \quad f_{\max} = 770\,\text{GHz}$

$C_{cb} / I_c = 0.15\,\text{ps/V}$

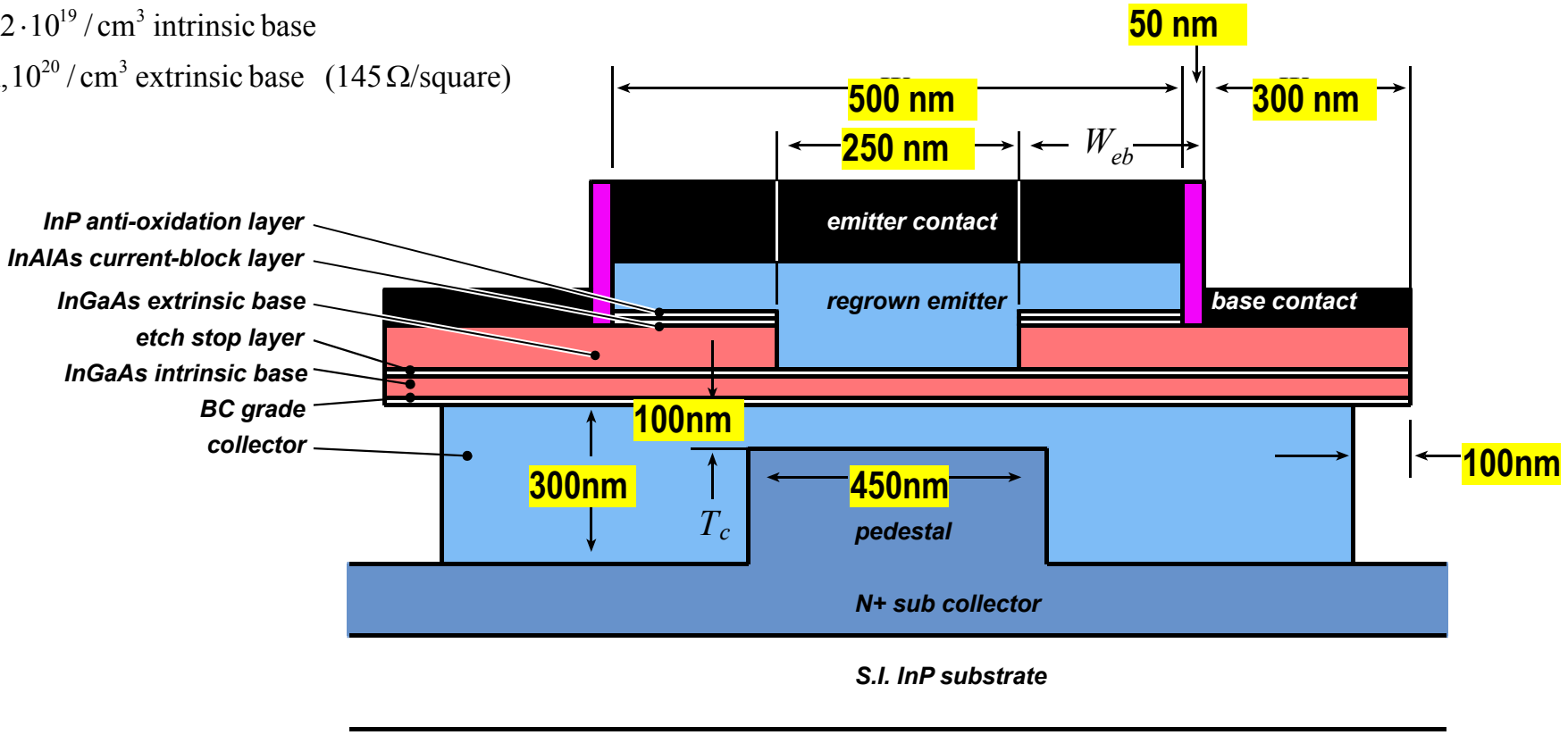
$V_{br,ceo} \cong 4\,\text{V}$



RGE+Pedestal: Projected Performance @ 250 nm

$20\ \text{nm}, 2\cdot10^{19}\ /\ \text{cm}^3$ intrinsic base

$100\ \text{nm}, 10^{20}\ /\ \text{cm}^3$ extrinsic base (145 Ω/square)



$\rho_{c,emitter} = 6\ \Omega\text{-}\mu\text{m}^2$

$\Rightarrow R_{ex}A_E \sim 3\ \Omega\text{-}\mu\text{m}^2$

$\rho_{c,base} = 10\ \Omega\text{-}\mu\text{m}^2$

$J_e = 17\ \text{mA}/\mu\text{m}^2$

0.3 ps wiring delay on collector bus

$f_{\text{clock (divider)}} \cong 330\ \text{GHz}$

$f_\tau = 650\ \text{GHz} \quad f_{\max} = 900\ \text{GHz}$

$C_{cb} / I_c = 0.17\ \text{ps/V}$

$V_{br,ceo} \cong 4\ \text{V}$

Indium Phosphide HBTs

InP HBT now: at 500 nm scaling generation

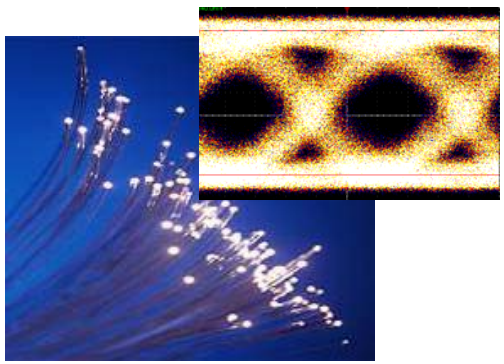
455 GHz f_t & 485 GHz f_{max}
150 GHz static dividers & 180 GHz amplifiers demonstrated
200 GHz digital latches & 300 GHz amplifiers are feasible

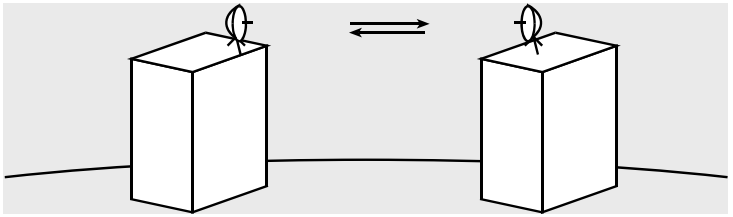
InP HBT: future, at 125 nm scaling generation

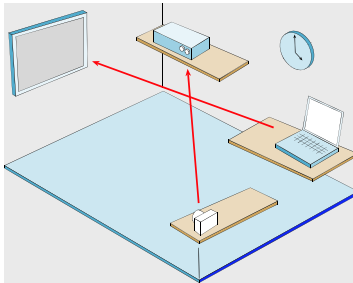
2:1 increase in bandwidth (?)
~1 THz f_t & f_{max} , 400 GHz digital latches & 600 GHz amplifiers ???
demands 4:1 better Ohmic contacts
demands 4:1 increased current density.

Applications:

160+ Gb/s fiber ICs,
300 GHz MIMICs for communications, radar, & imaging
GHz ADCs / DACs / DDFS / etc.
& applications unforeseen & unanticipated







End