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InP HBT Digital ICs and MMICs in the 140-220 GHz band

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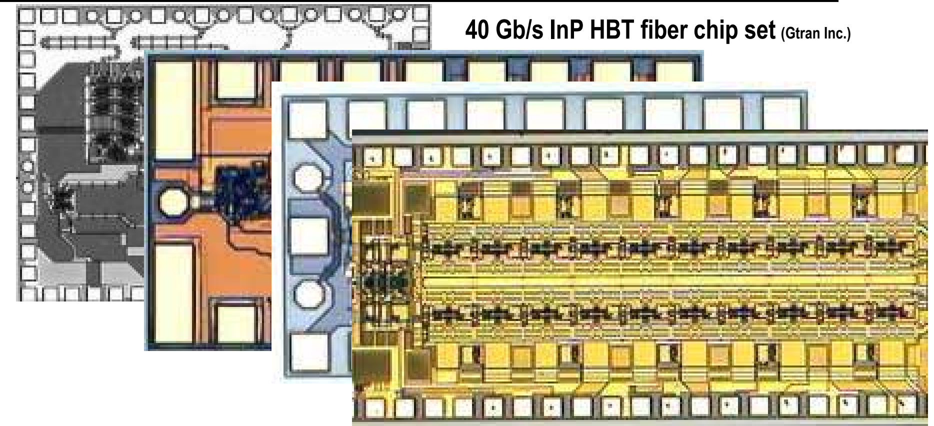
What could we do with 100-350 GHz integrated circuits ?

Optical Fiber Transmission

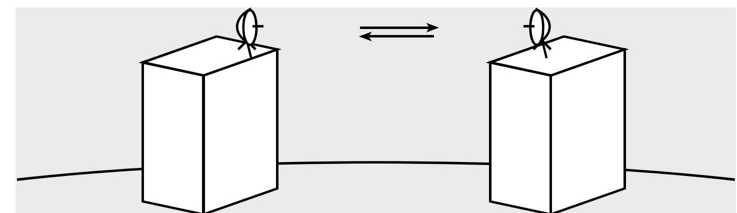
40 Gb/s: InP and SiGe ICs commercially available

80 & 160 Gb/s is feasible
80-160 Gb/s InP ICs now clearly feasible
~100 GHz modulators demonstrated
100 + GHz photodiodes are easy
challenge: fiber dispersion



40 Gb/s InP HBT fiber chip set (Gtran Inc.)

250 GHz digital radio: 100 Gb/s over 1 km in heavy rain

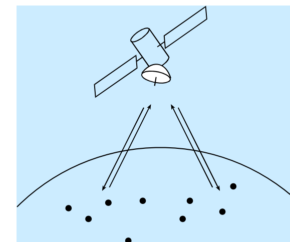


Radio-wave Transmission / Radar / Imaging

65-80 GHz, 120-160 GHz, 220-300 GHz
100 Gb/s transmission over 1 km in heavy rain
300 GHz imaging for foul-weather aviation

science
spectroscopy, radio astronomy

mm-wave sensor networks



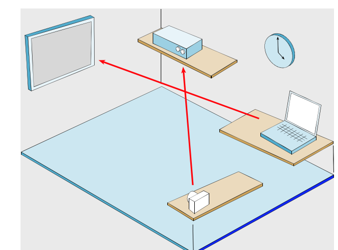
300 GHz imaging

Mixed-Signal ICs for Military Radar/Comms

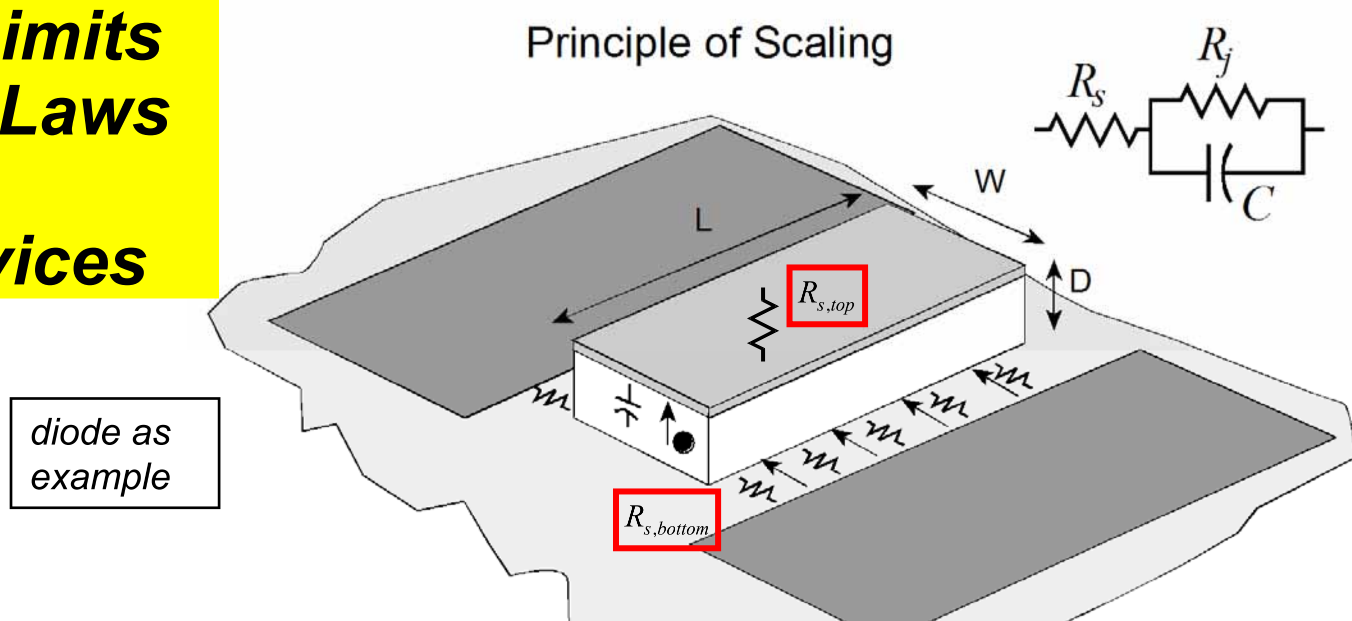
direct digital frequency synthesis, ADCs, DACs
high resolution at very high bandwidths sought

Why develop transistors for mm-wave & sub-mm-wave applications ?
→ compact ICs supporting complex high-frequency systems.

Gb/s Wireless Home Networks

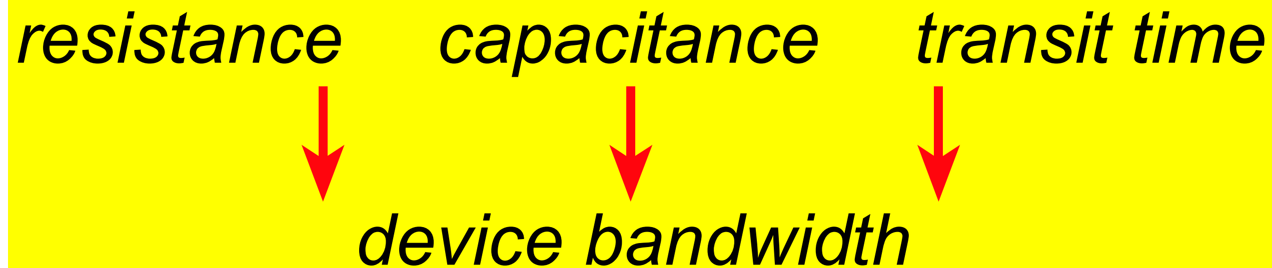


Frequency Limits and Scaling Laws of (most) Electron Devices



contributing parameters	*time constant*	*to double bandwidth*
transit time	$\tau \propto D / v_{electron}$	reduce D by 2 : 1
$C \propto WL / D$ $R_{s,bottom} \propto 1 / L$	$R_{s,bottom} C \propto W / D$	reduce W by 4 : 1
$C \propto WL / D$ $R_{s,top} \propto \rho_{contact} / WL$	$R_{s,top} C \propto \rho_{contact} / D$	reduce $\rho_{contact}$ by 4 : 1 use Schottky : $\rho_{contact} = 0$ use flared contact : $R_{s,top} L \sim \rho_c \ln(1/W)$
$C \propto WL / D$ $R_{junction} \propto kT / qI$	$R_{junction} C \propto WL / ID$ $\propto 1 / JD$	increase J by 4 : 1
space - charge limited J		$J_{\max} \propto (V + \phi) v_{electron} / D^2$, increases 4 : 1

R/C/τ Limits the Bandwidth of (most) Electron Devices

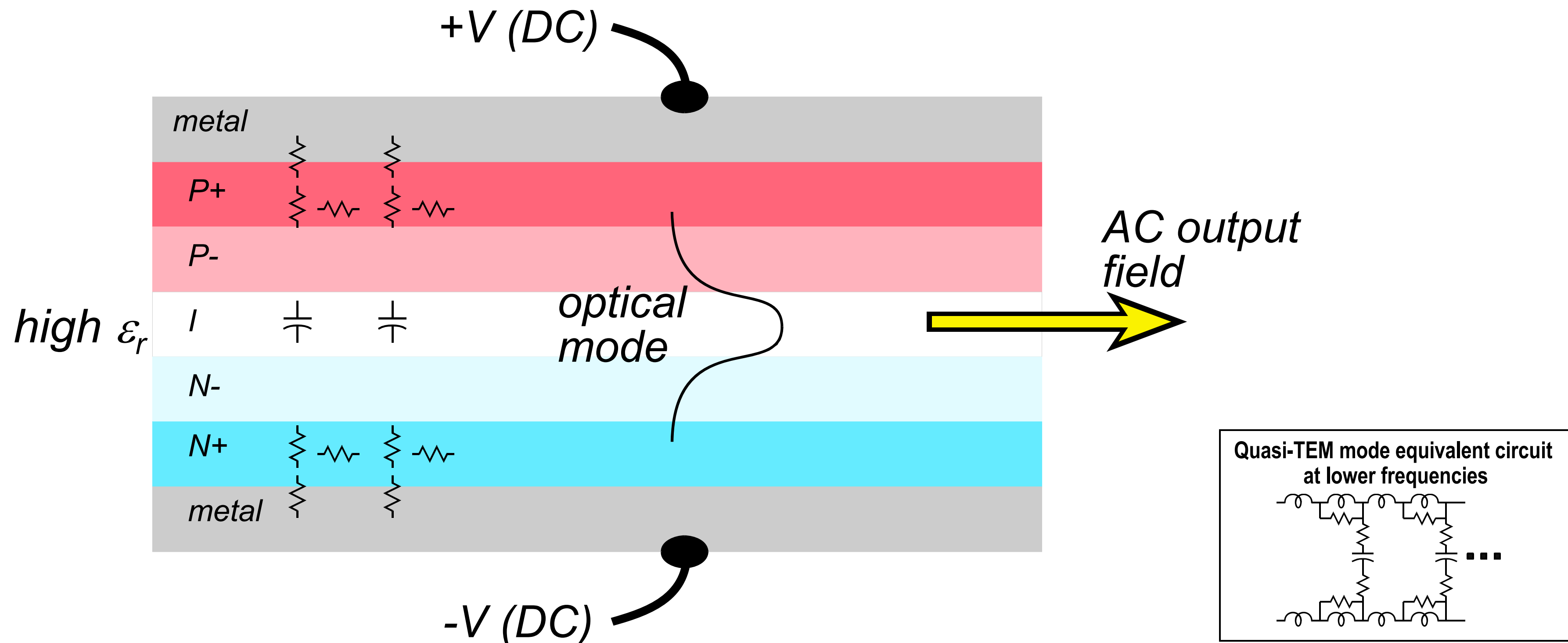


applies to:
bipolar transistors, field-effect transistors, Schottky diodes
RTDs, photomixers, photodiodes

Applies whenever AC signals are removed though Ohmic contacts

Effective THz devices
must minimize, eliminate, or circumvent
contact resistance, capacitance, & transit time

Why aren't semiconductor lasers R/C/τ limited ?



dielectric waveguide mode confines AC field away from resistive bulk and contact regions.

AC signal is not coupled through electrical contacts

dielectric mode confinement is harder at lower frequencies

Diode & Transistor Integrated Circuits to ~ 1 THz

10-nm to 100-nm electron drift devices:

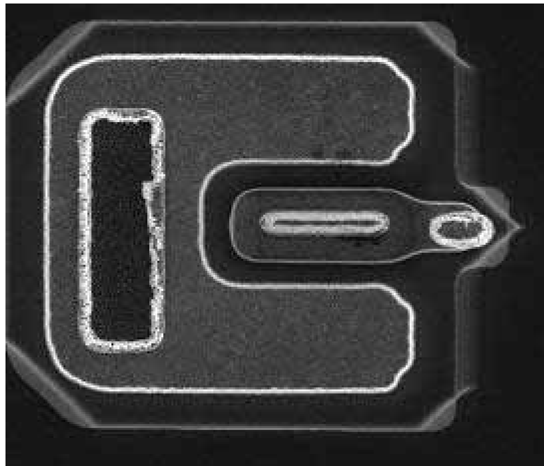
100 nm-generation InP DHBTs
signal generation with power to ~500 GHz

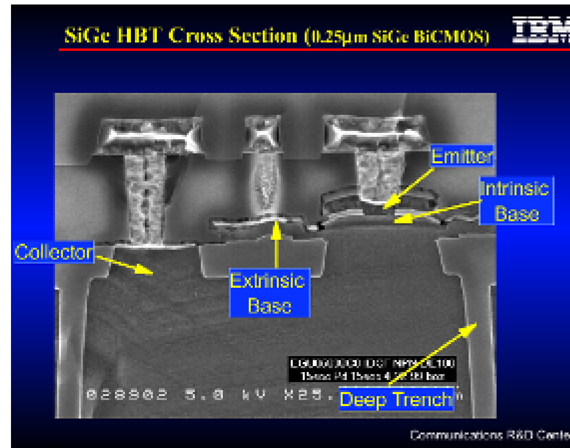
< 30 nm-generation InP HEMTs
30 nm devices now get ~600 GHz f_t
→ low noise figure at 300 GHz

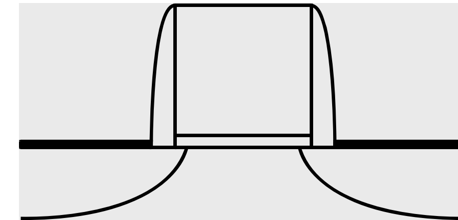
<50 nm-generation InP or GaAs Schottky mixer diodes
many THz RC and transit time frequencies

And Silicon VLSI for applications below ~150 GHz !

Fast IC Technologies







InP HBT: 500 nm emitter
455 GHz f_{τ} / 485 GHz f_{max}
~4 V breakdown
150 GHz static dividers
178 GHz amplifiers

SiGe HBT: 130 nm emitter
300 GHz f_{τ} / 350 GHz f_{max}
96 GHz static dividers
77 GHz amplifiers
150 GHz push-push VCO- 75 GHz fundamental

CMOS: 90 nm node:
~200 GHz f_{τ} / 250 GHz f_{max}
60 GHz 2:1 mux
91 GHz amplifiers

InP HBTs:
450 GHz bandwidth at 500 nm scaling
Potential for much wider bandwidths at 100 nm scaling

We design HBTs for fast logic, not for high f_τ & f_{max}

Gate Delay Determined by :

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C}\right)\left(C_{cb} + C_{be,\text{depletion}}\right)$$

Depletion capacitance charging through the base resistance

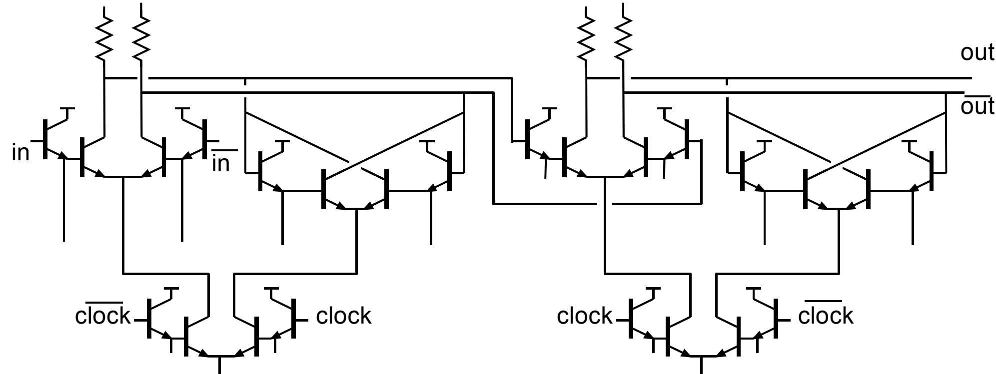
$$R_{\text{bb}}\left(C_{cbi} + C_{be,\text{depletion}}\right)$$

Supplying base + collector stored charge through the base resistance

$$R_{\text{bb}}(\tau_b + \tau_c)\left(\frac{I_C}{\Delta V_{LOGIC}}\right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 4 \cdot \left(\frac{kT}{q} + R_{ex} I_c\right)$$



$(\tau_b + \tau_c)$ typically 10 - 25% of total delay;
Delay not well correlated with f_τ

$(\Delta V_{LOGIC} / I_C)(C_{cb} + C_{be,\text{depl}})$ is 55% - 80% of total.

High (I_C / C_{cb}) is a key HBT design objective.

$$J_{\max,Kirk} = 2\varepsilon \overline{v}_{electron}(V_{ce,\text{ operating}} + V_{ce,\text{full depletion}}) / T_c^2$$

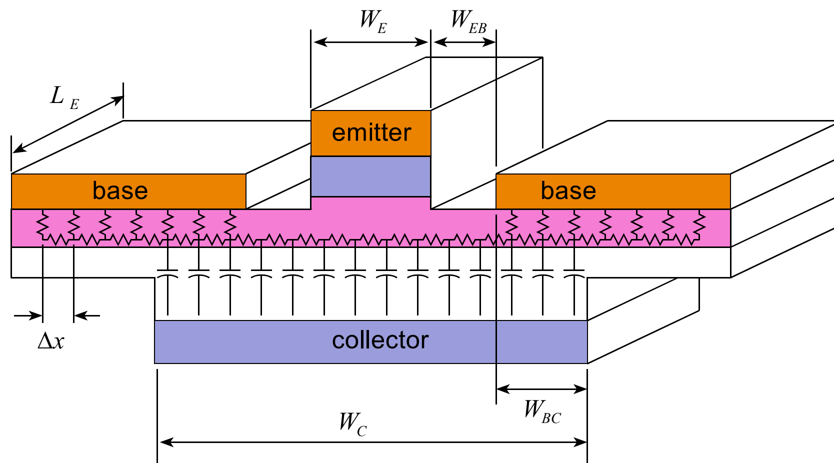
$$\Rightarrow \frac{C_{cb}\Delta V_{LOGIC}}{I_C} = \frac{\Delta V_{LOGIC}}{2V_{CE,\min}}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2\overline{v}_{electron}}\right)$$

R_{ex} must be very low for low ΔV_{logic} at high J

Bipolar Transistor Scaling Laws & Scaling Roadmaps

Scaling Laws:
design changes required
to double transistor bandwidth

key device parameter	required change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter resistance per unit emitter area	decrease 4:1
current density	increase 4:1
base contact resistivity (if contacts lie above collector junction)	decrease 4:1
base contact resistivity (if contacts do not lie above collector junction)	unchanged



InP Technology Roadmap
40 / 80 / 160 Gb/s digital clock rate

Parameter	Gen. 1	Gen. 2	Gen. 3
MS-DFF speed	60 GHz	121 GHz	260 GHz
Emitter Width	1 μm	0.8 μm	0.3 μm
Parasitic Resistivity	50 Ω-μm²	20 Ω-μm²	5 Ω-μm²
Base Thickness	400Å	400Å	300 Å
Doping	5 10^{19}/cm²	7 10^{19}/cm²	7 10^{19}/cm²
Sheet resistance	750 Ω	700 Ω	700 Ω
Contact resistance	150 Ω-μm²	20 Ω-μm²	20 Ω-μm²
Collector Width	3 μm	1.6 μm	0.7 μm
Collector Thickness	3000 Å	2000 Å	1000 Å
Current Density	1 mA/μm²	2.3 mA/μm²	12 mA/μm²
$A_{collector}/A_{emitter}$	4.55	2.6	2.9
f_τ	170 GHz	248 GHz	570 GHz
f_{max}	170 GHz	411 GHz	680 GHz
I_E / L_E	1 mA/μm	1.9 mA/μm	3.7 mA/μm
τ_f	0.67 ps	0.50 ps	0.22 ps
C_{cb} / I_c	1.7 ps/V	0.62 ps/V	0.26 ps/V
$C_{cb}\Delta V_{logic} / I_c$	0.5 ps	0.19 ps	0.09 ps
$R_{bb} /(\Delta V_{logic} / I_c)$	0.8	0.68	0.99
$C_{je}(\Delta V_{logic} / I_C)$	1.7 ps	0.72 ps	0.15 ps
$R_{ex} /(\Delta V_{logic} / I_c)$	0.1	0.15	0.17

key figures of merit for logic speed

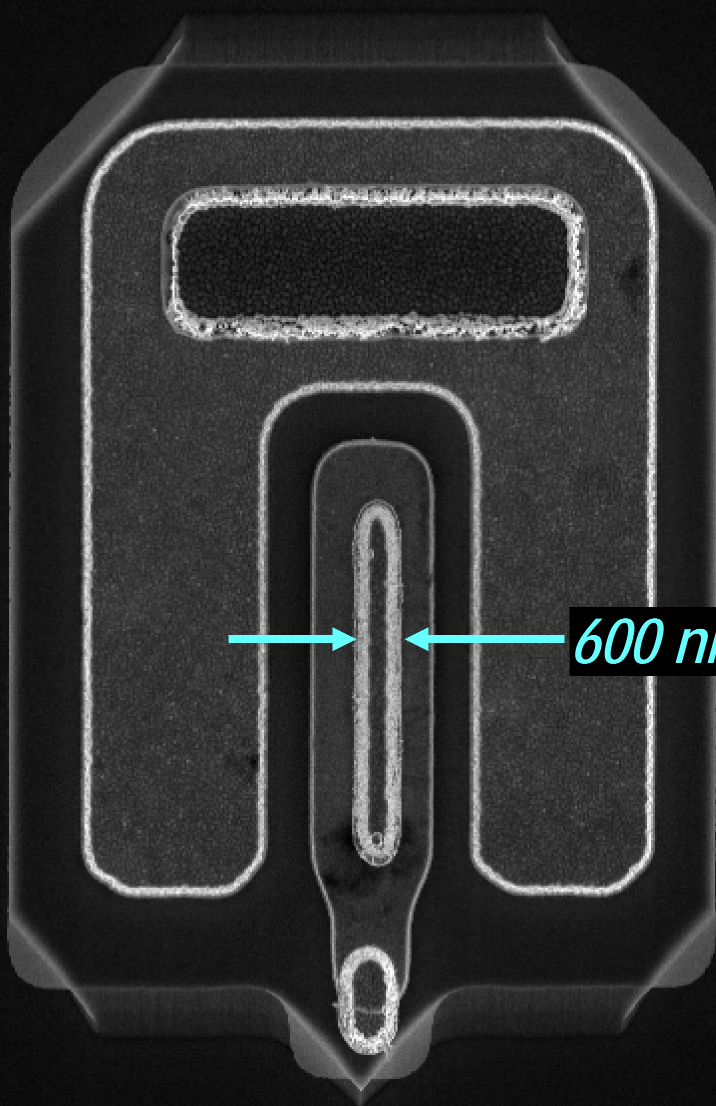
Key scaling challenges →
emitter & base contact resistivity
current density→ device heating
collector-base junction width scaling
& Yield !

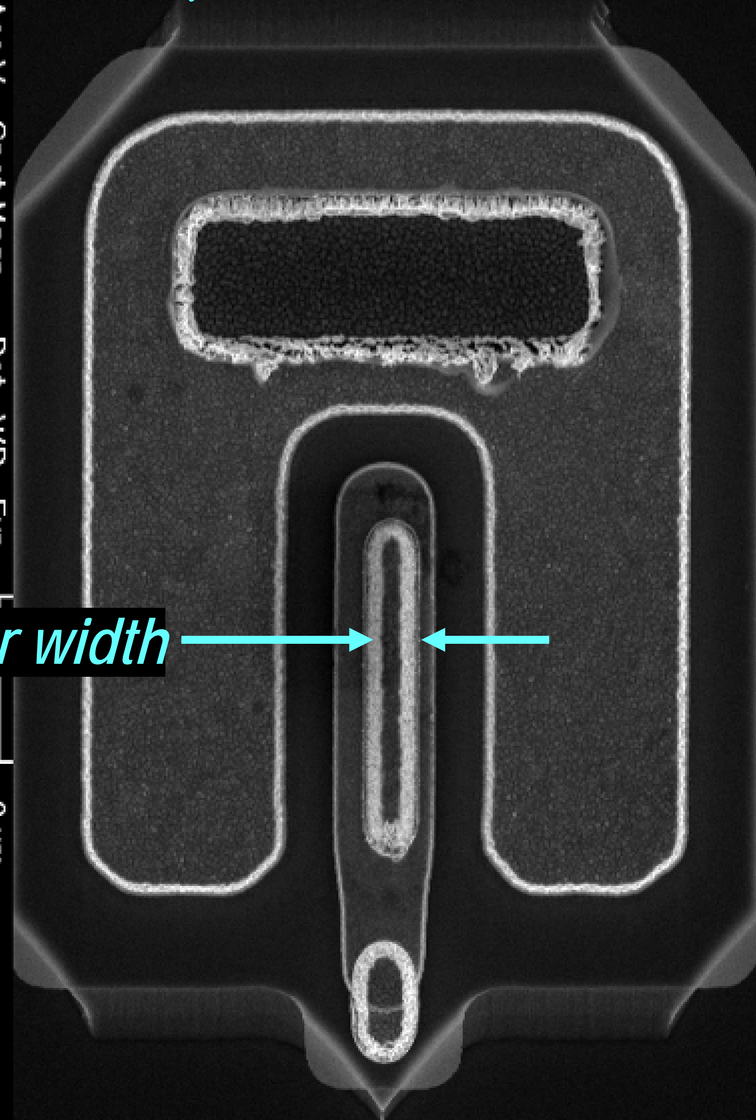
Zach Griffith

Transistors & ICs at 500-600 nm Scaling Generation

1.7 µm base-collector mesa

1.3 µm base-collector mesa





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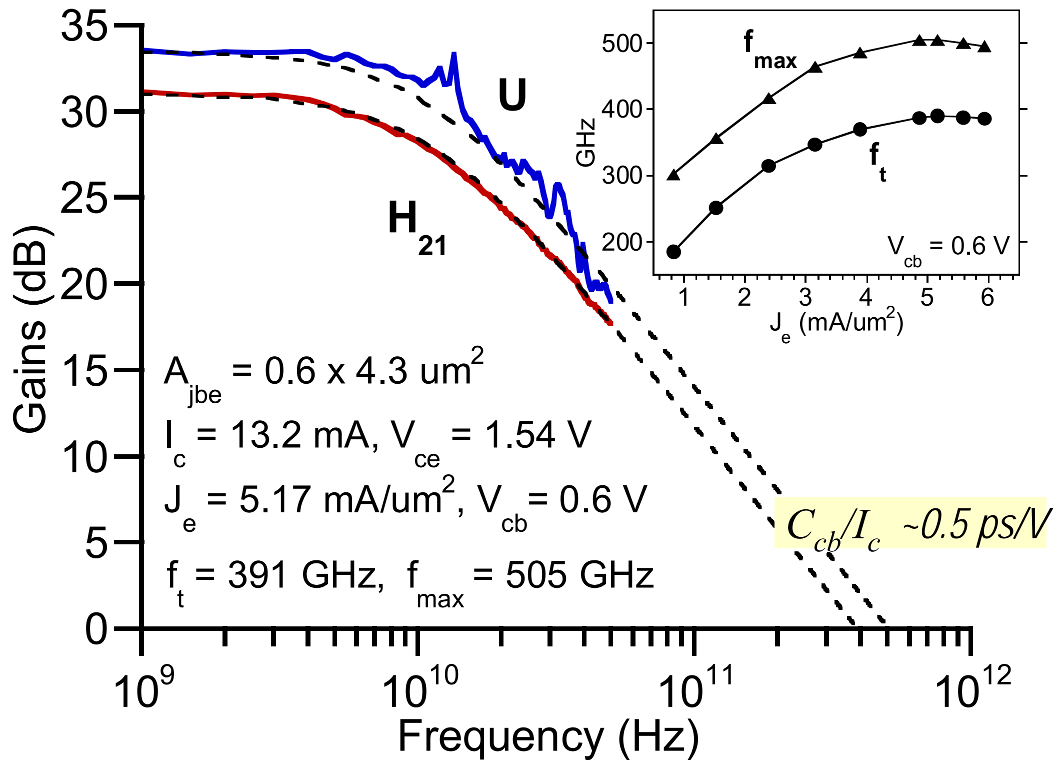
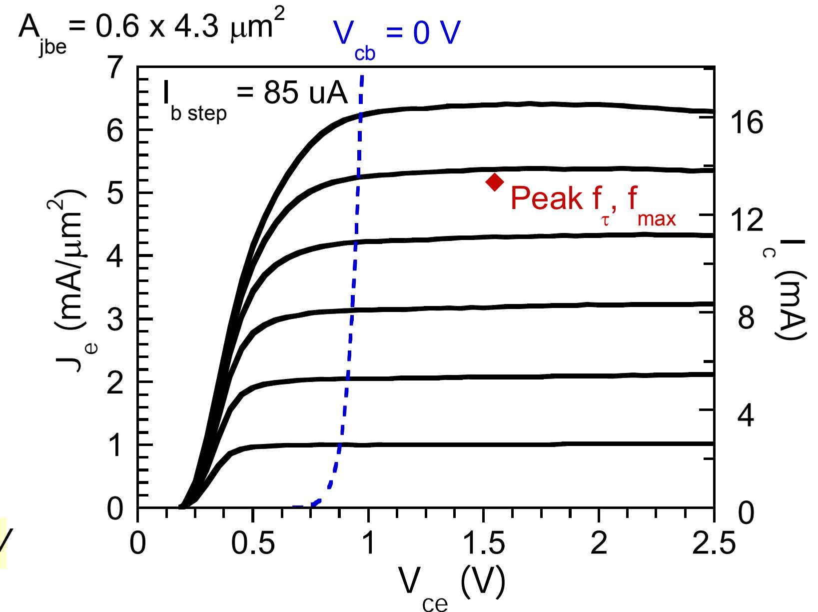
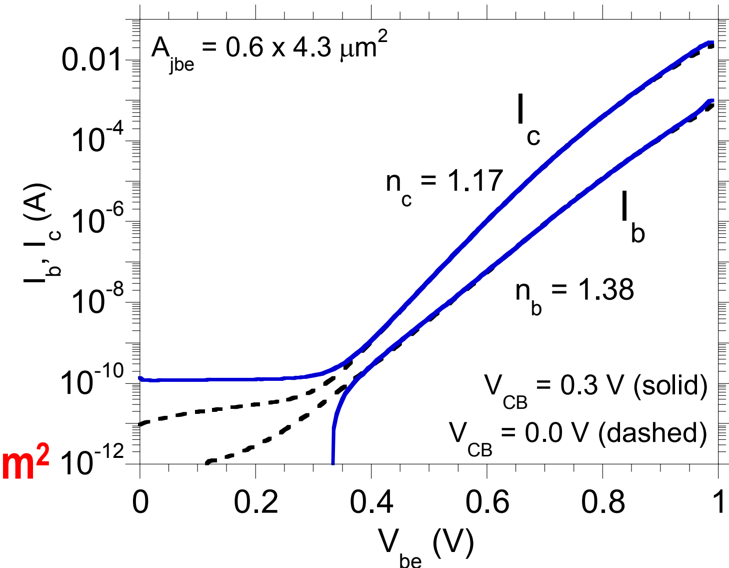
InP DHBT: 600 nm lithography, 150 nm thick collector, 30 nm thick base







Average $\beta \approx 36$, $V_{BR,CEO}$ = 5.1 V (I_c = 50 μA)

Emitter contact (from RF extraction), R_{cont} = 10.1 Ω·μm²

Base (from TLM) : R_{sheet} = 564 Ω/sq, R_{cont} = 9.6 Ω·μm²

Collector (from TLM) : R_{sheet} = 11.9 Ω/sq, R_{cont} = 5.4 Ω·μm²

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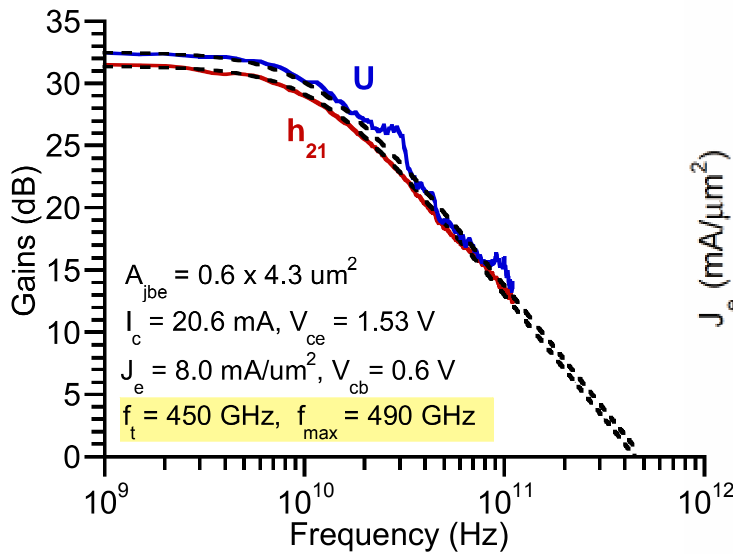
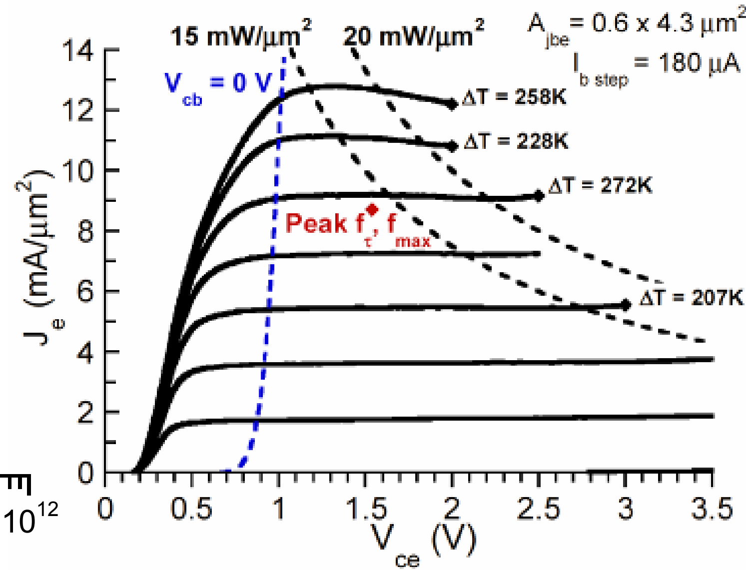
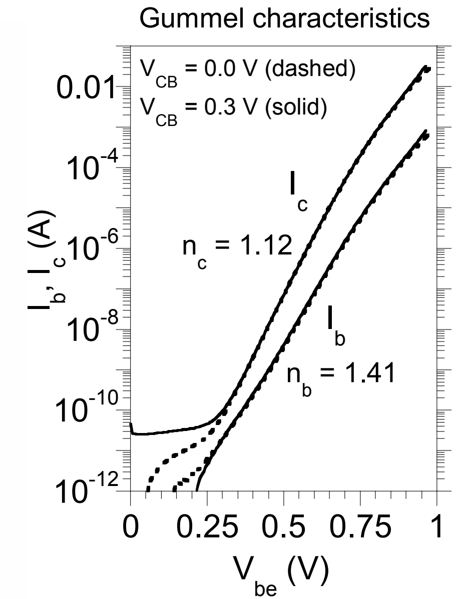
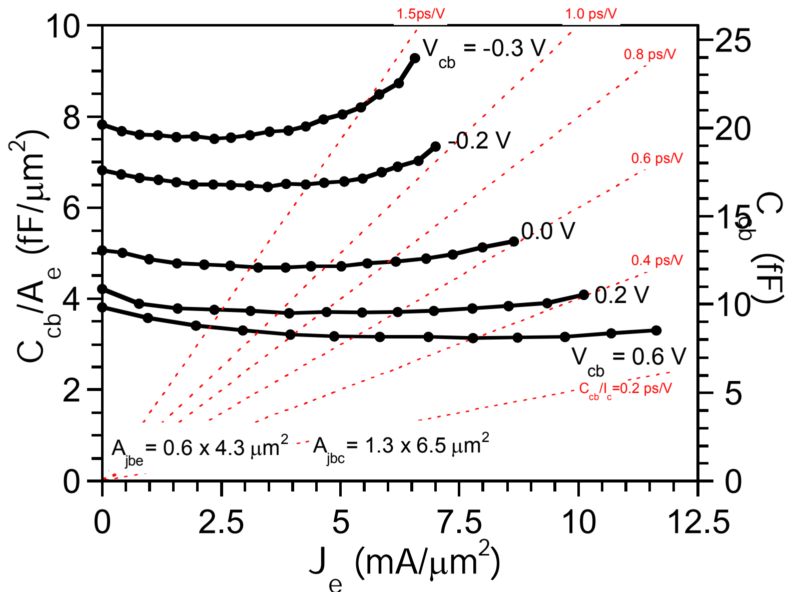
InP DHBT: 600 nm lithography, 120 nm thick collector, 30 nm thick base









$\beta \approx 40$, $V_{BR,CEO} = 3.9$ V.

Emitter contact $R_{cont} < 10\ \Omega\cdot\mu m^2$

Base : $R_{sheet} = 610\ \Omega$/sq, $R_{cont} = 4.6\ \Omega\cdot\mu m^2$

Collector : $R_{sheet} = 12.1\ \Omega$/sq, $R_{cont} = 8.4\ \Omega\cdot\mu m^2$

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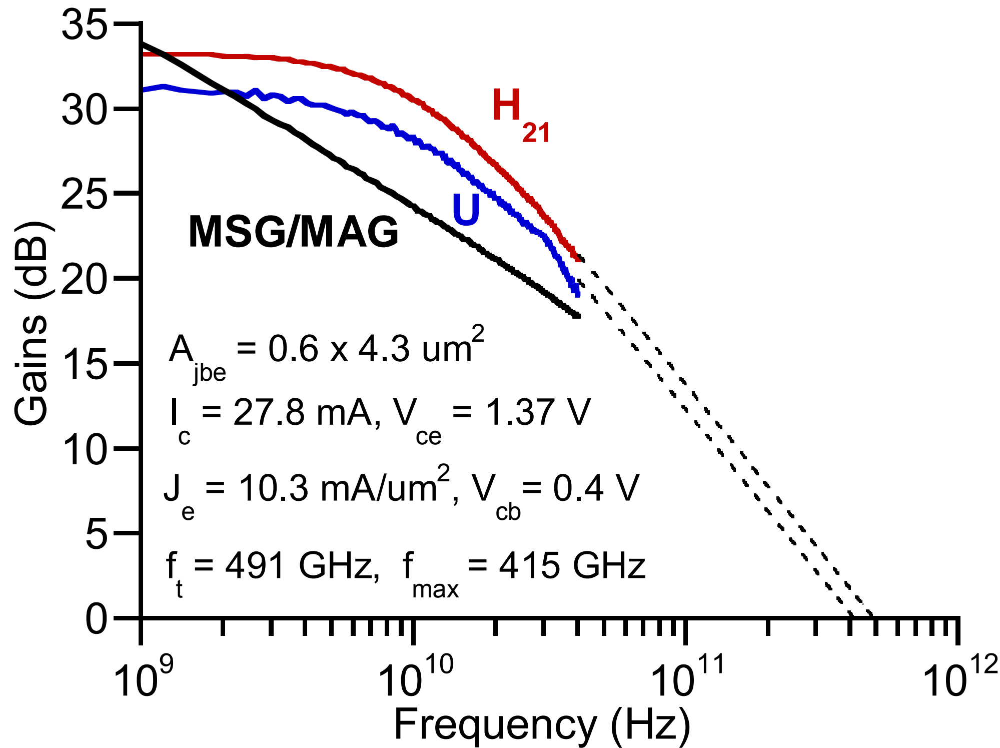
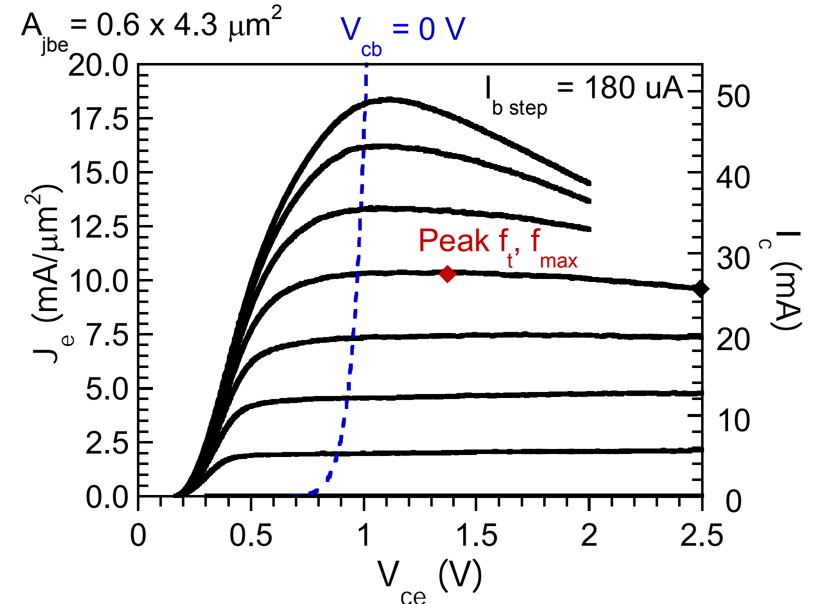
InP DHBT: 600 nm lithography, 100 nm thick collector, 30 nm thick base





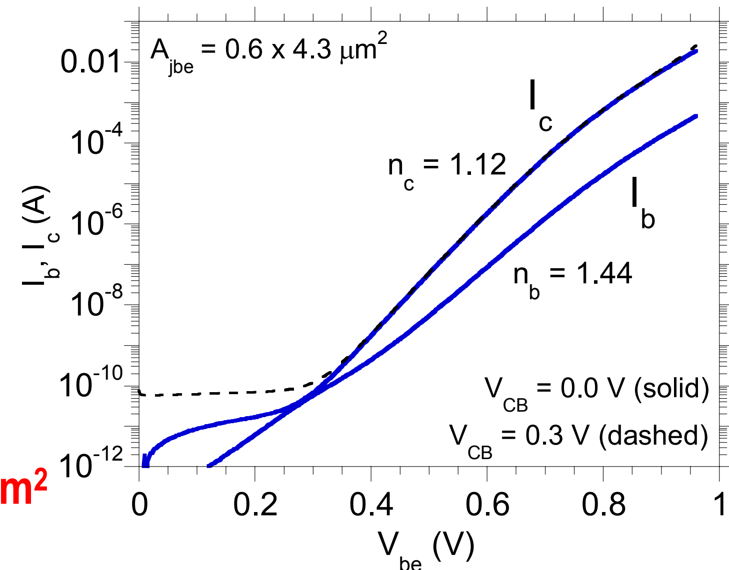
Summary of device parameters—

Average β ≈ 40, $V_{BR, CEO}$ = 3.1 V (I_c = 50 μA)

Emitter contact (from RF extraction), R_{cont} ≈ 7.8 Ω·μm²

Base (from TLM) : R_{sheet} = 629 Ω/sq, R_{cont} = 6.2 Ω·μm²

Collector (from TLM) : R_{sheet} = 12.9 Ω/sq, R_{cont} = 4.0 Ω·μm²



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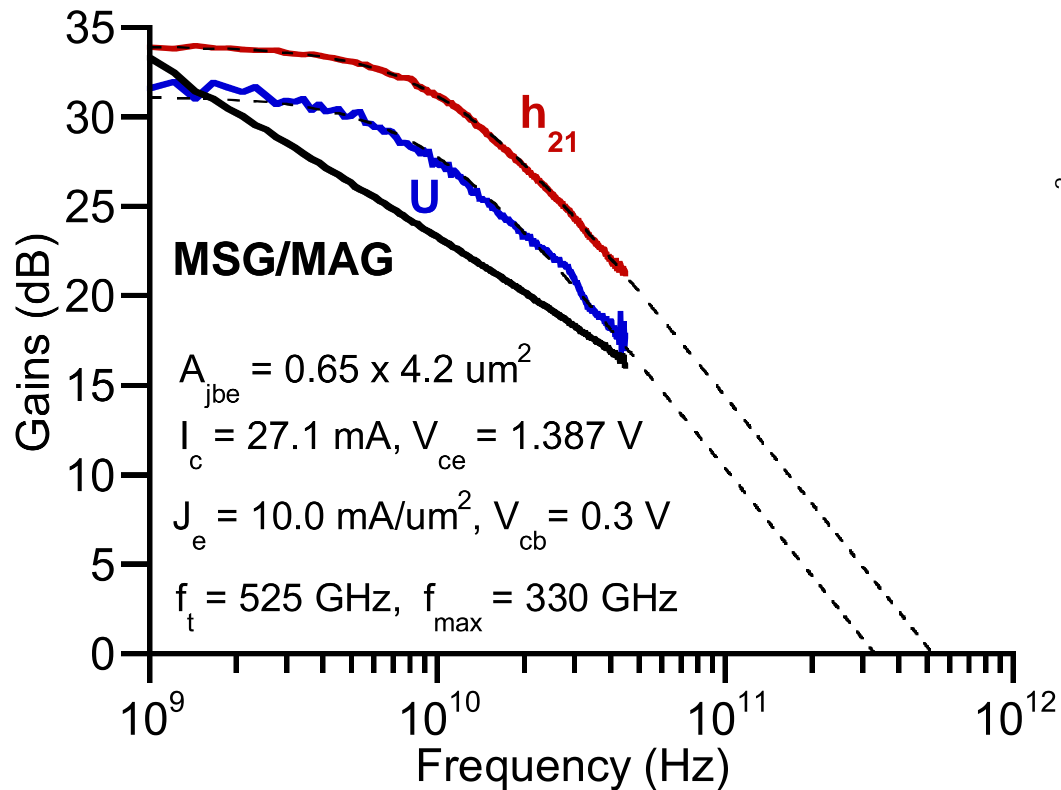
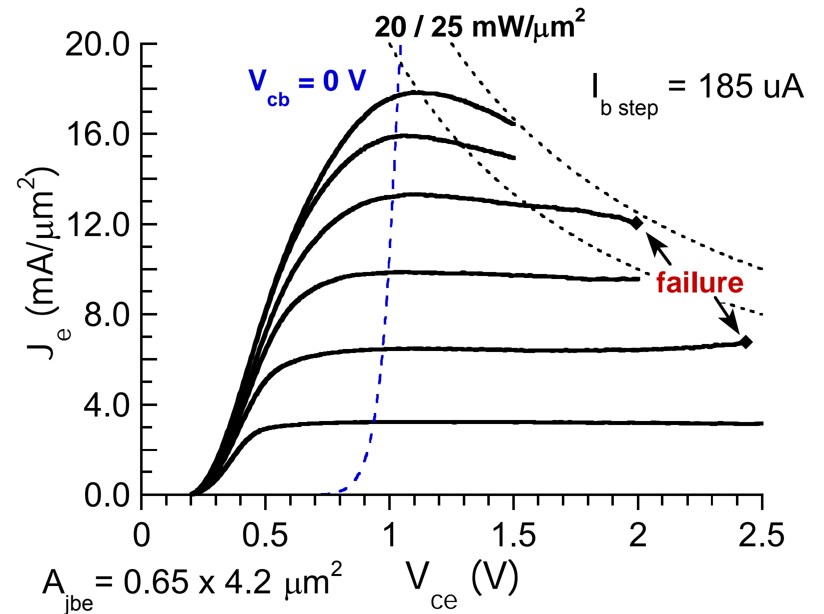
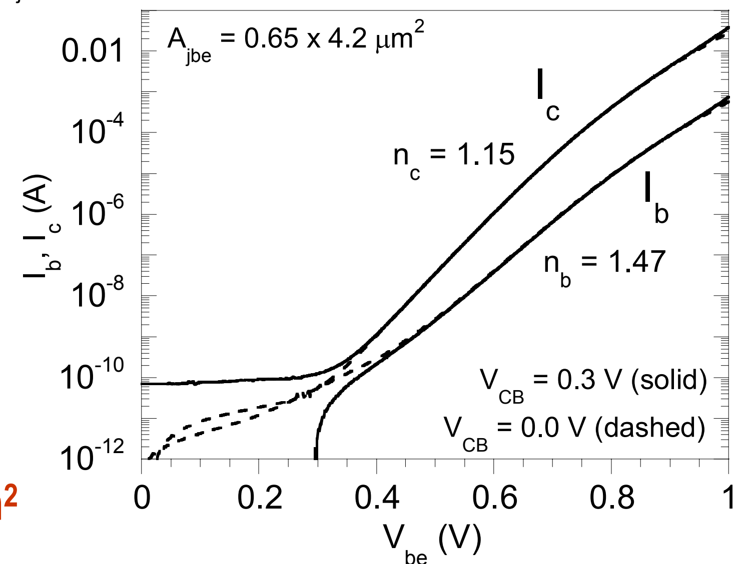
InP DHBT: 600 nm lithography, 75 nm thick collector, 25 nm thick base







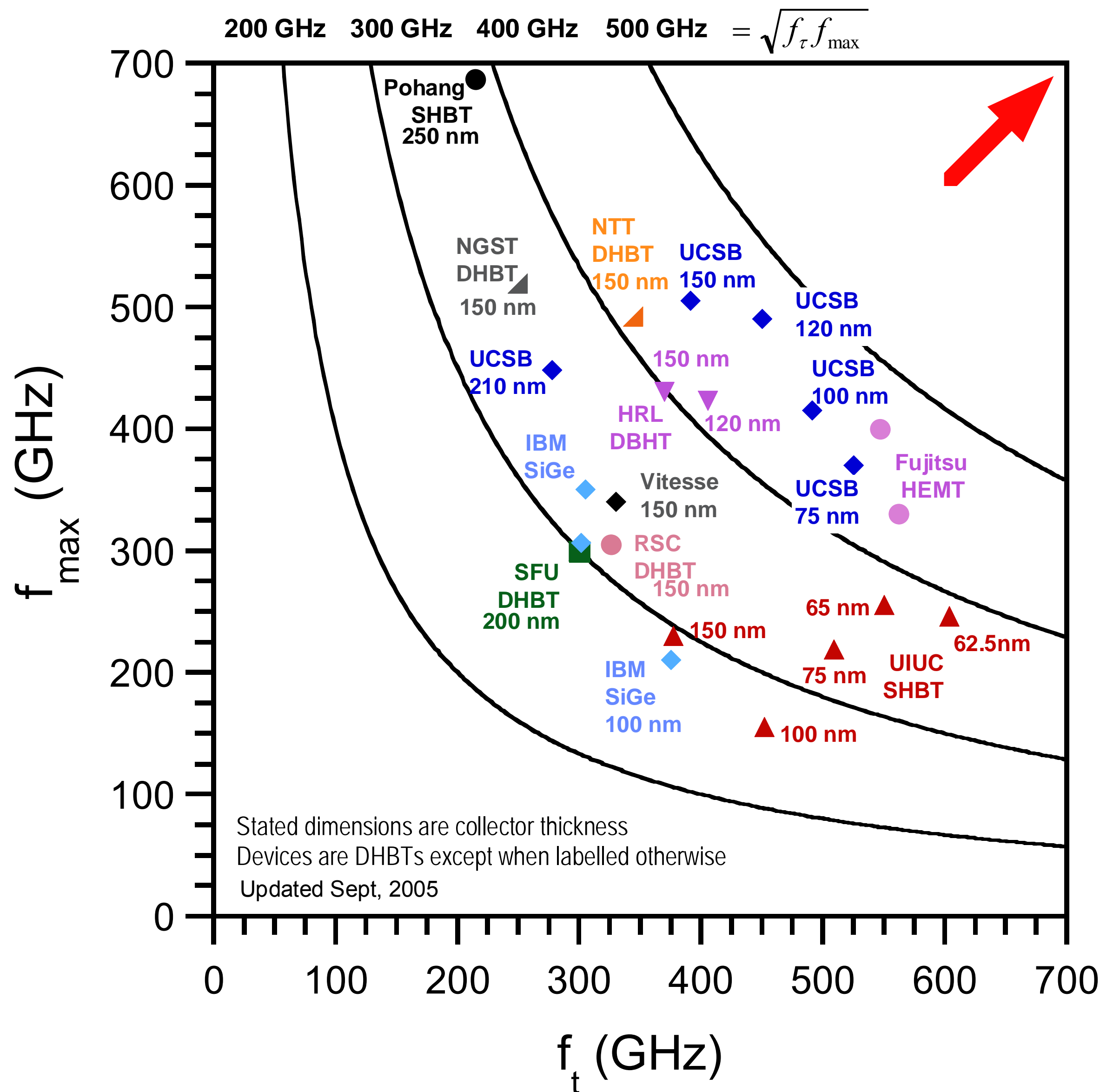
Average $\beta \approx 50$, BV_{CEO} = 3.1 V, BV_{CBO} = 3.4 V (I_c = 50 µA)

Emitter contact (from RF extraction), $R_{cont} \approx$ TBD $\Omega \cdot \mu m^2$

Base (from TLM) : R_{sheet} = 805 Ω/sq, R_{cont} = 16 $\Omega \cdot \mu m^2$

Collector (from TLM) : R_{sheet} = 12.0 Ω/sq, R_{cont} = 4.7 $\Omega \cdot \mu m^2$

Summary of published HBT performance



popular metrics :

$(f_\tau + f_{max})/2$

$\sqrt{f_\tau f_{max}}$

$(1/f_\tau + 1/f_{max})^{-1}$

better metrics :

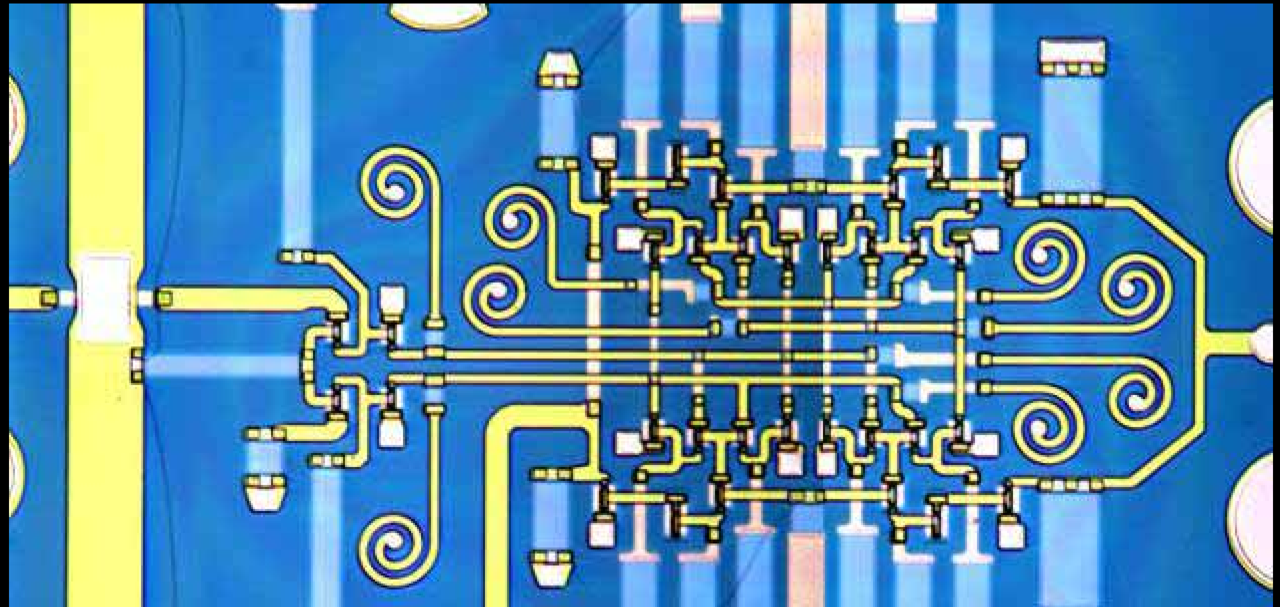
power amplifiers :
- PAE,
- associated gain,
- $mW/\mu m$

low noise amplifiers :
- F_{min},
- associated gain,
- associated DC power

digital :
- f_{clock}, hence
- $(C_{cb}\Delta V / I_c)$,
- $(R_{ex} I_c / \Delta V)$,
- $(R_{bb} I_c / \Delta V)$,
- $(\tau_b + \tau_c)$

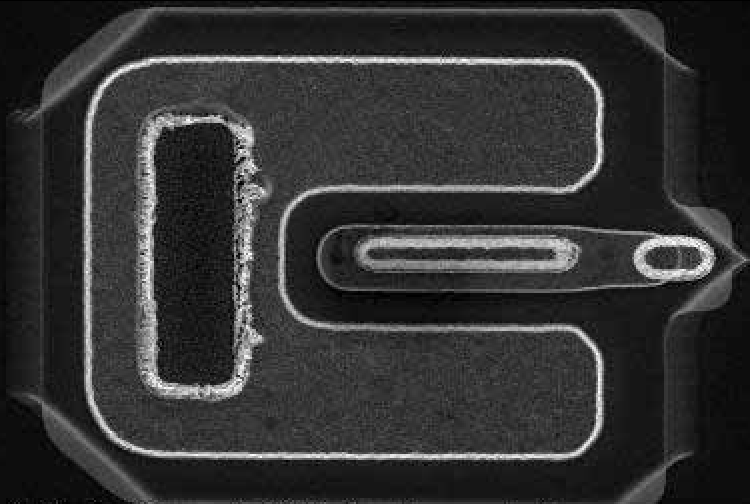
UCSB results are @ 600 nm; further progress requires scaling to 250 nm

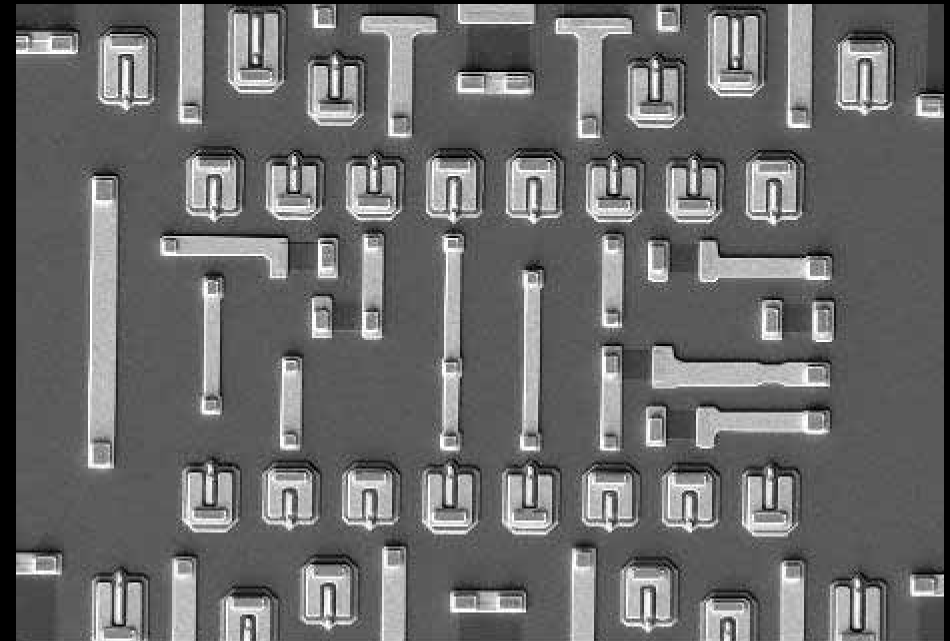
Digital circuits: towards 200 GHz clock rate



142 GHz latch from NNIN @ UCSB,
150 GHz ICs from UCSB/GSC/RSC
200 GHz is the next goal

underlying technology:
400-500 GHz InP transistors





Z Griffith

Static Frequency Divider: Standard Digital Benchmark

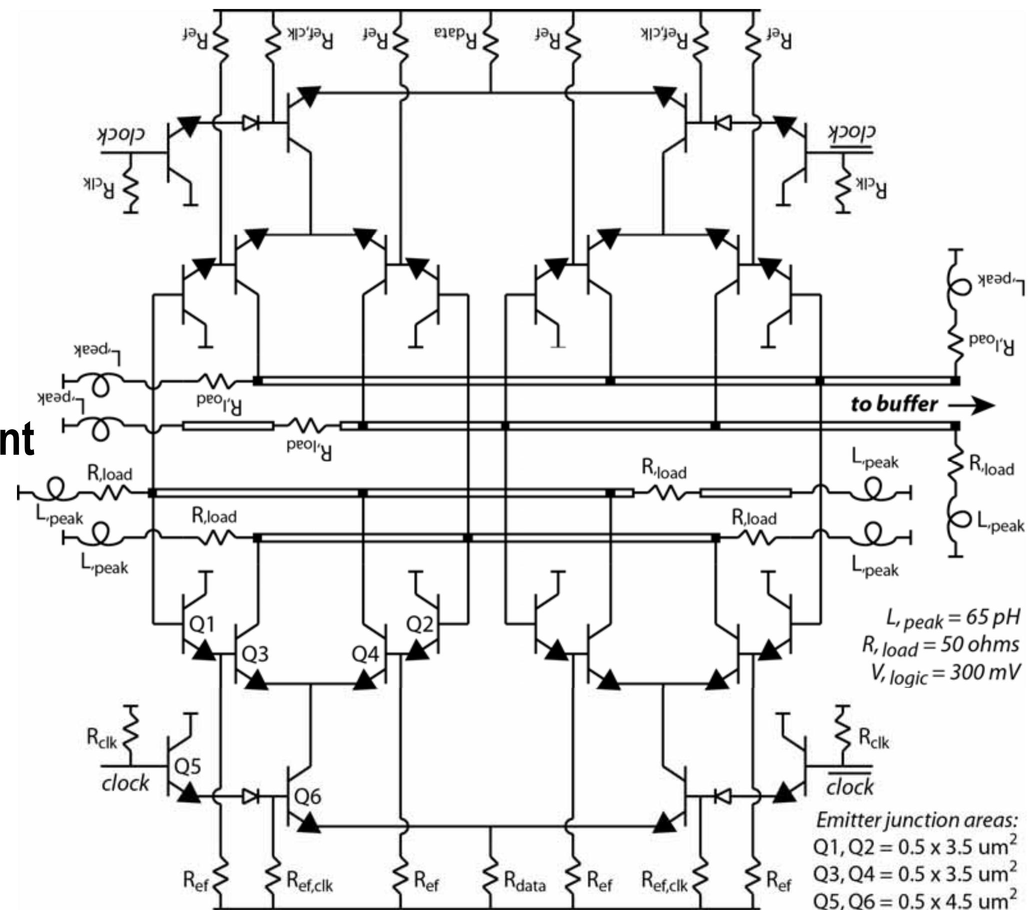
ECL Master-Slave Latch with Inverting Feedback

Forms 2:1 Frequency Divider.

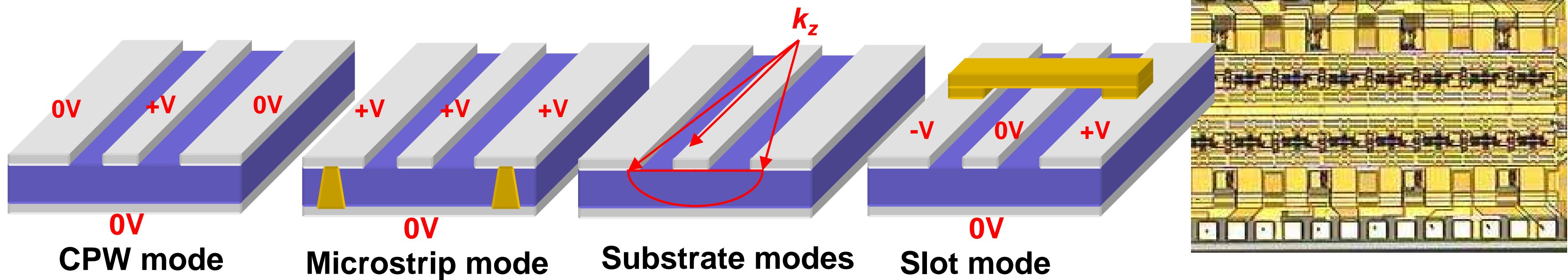
Maximum clock frequency is measure of technology speed.

Standard circuit configuration for consistent benchmarking - no tricks.

Small inductive peaking (L/R~1.3 ps).



CPW has parasitic modes, coupling from poor ground plane integrity



ground straps suppress slot mode, but multiple ground breaks in complex ICs produce ground return inductance
ground vias suppress microstrip mode, wafer thinning suppresses substrate modes

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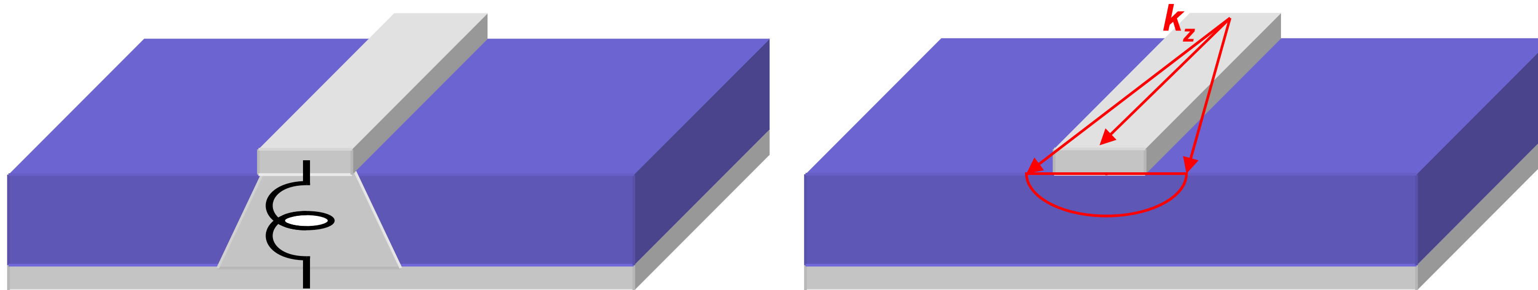
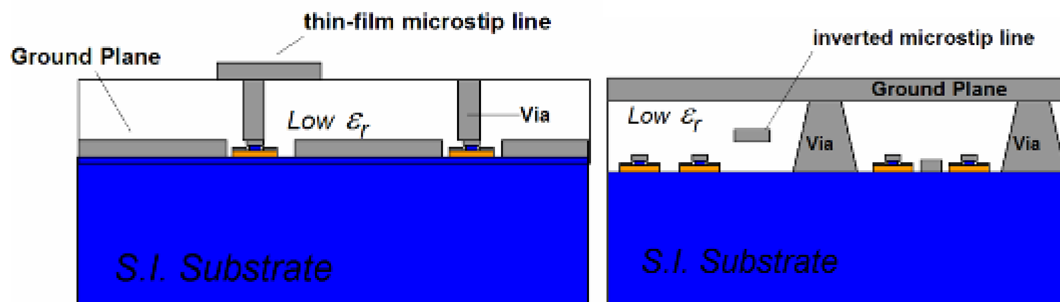
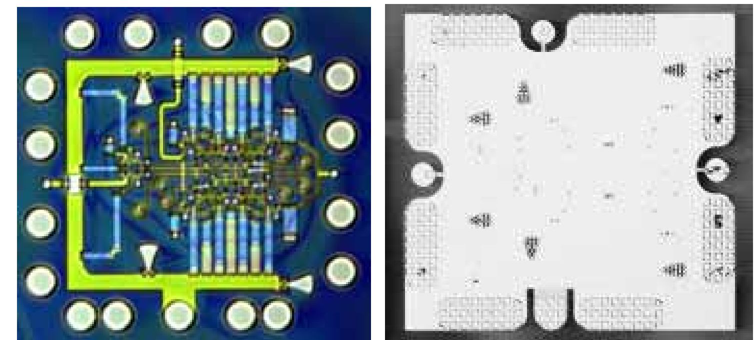
Microstrip has high via inductance, has mode coupling unless substrate is thin.



We prefer (credit to NTT) thin-film microstrip wiring, inverted is best for complex ICs



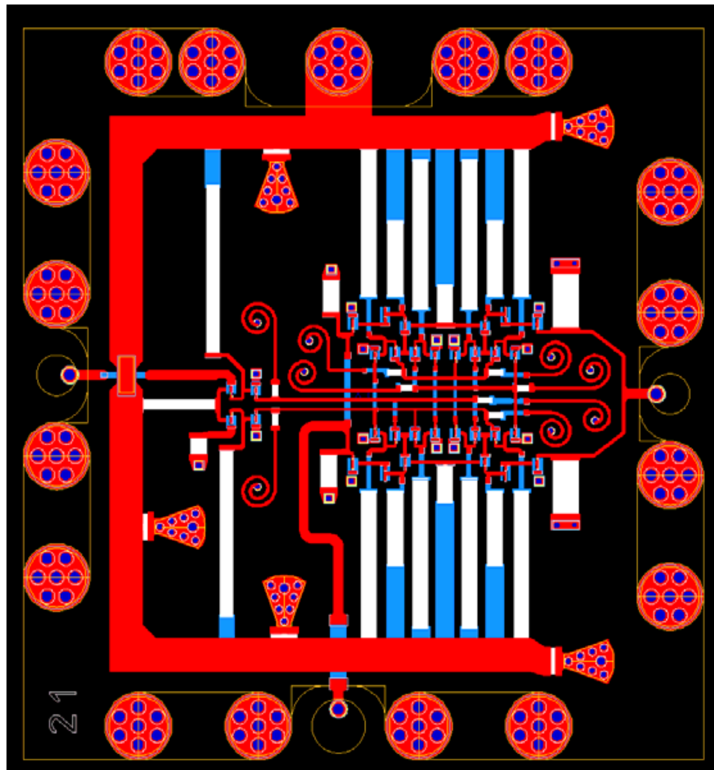


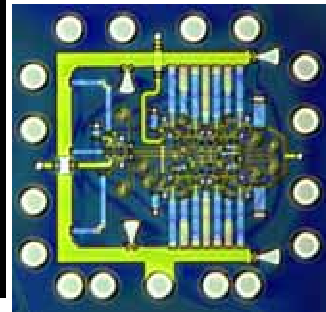
M. Urteaga, Z. Griffith, S. Krishnan

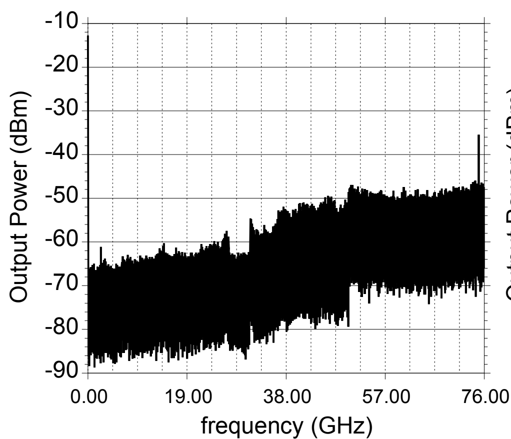
UCSB / RSC / GCS 150 GHz Static Frequency Dividers

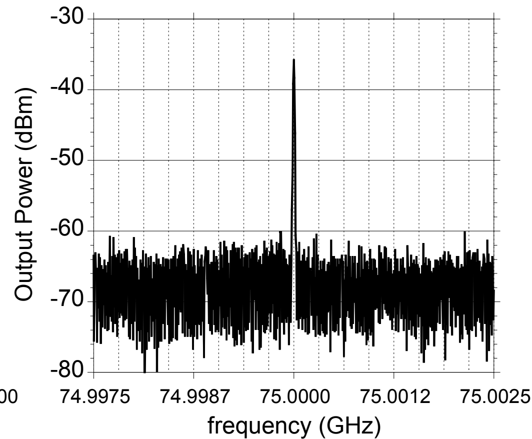
IC design: Z. Griffith, UCSB
HBT design: RSC / UCSB / GCS
IC Process / Fabrication: GCS
Test: UCSB / RSC / Mayo

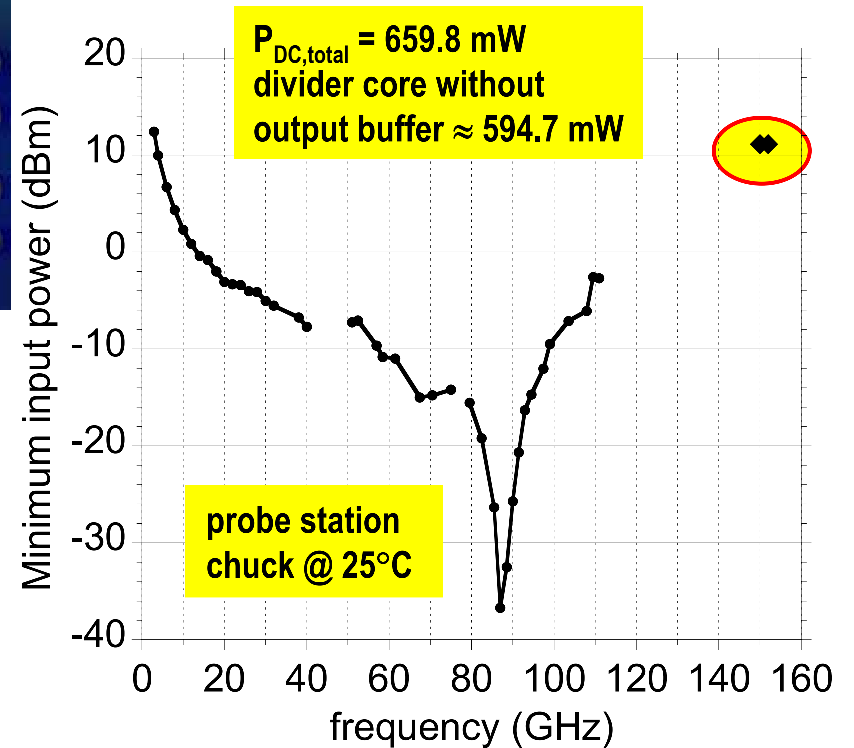
	units	data current steering	data emitter followers	clock current steering	clock emitter followers
size	μm^2	0.5 x 3.5	0.5 x 4.5	0.5 x 4.5	0.5 x 5.5
current density	$mA/\mu m^2$	6.9	4.4	4.4	4.4
C_{cb}/I_c	psec / V	0.59	0.99	0.74	0.86
V_{cb}	V	0.6	0	0.6	1.7
f_τ	GHz	301	260	301	280
f_{max}	GHz	358	268	358	280











Z. Griffith, M. Dahlström

UCSB 142 GHz Master-Slave Latches (Static Frequency Dividers)

Static 2:1 divider:
Standard digital benchmark.
Master-slave latch
with inverting feedback.
Performance comparison
between digital technologies

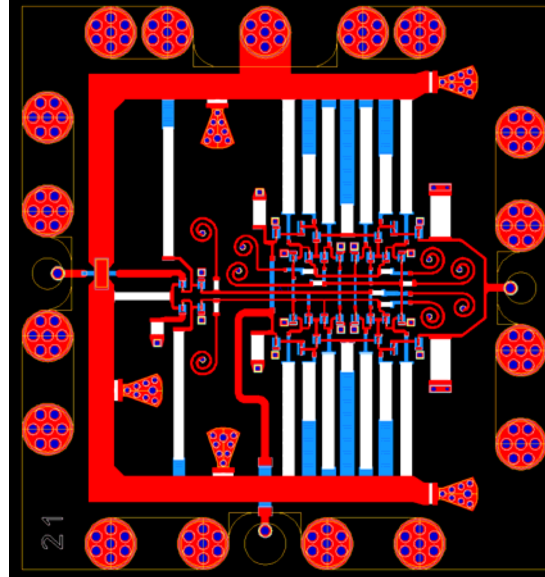
UCSB technology 2004:
InP mesa HBT technology
12-mask process
600 nm emitter width
142 GHz maximum clock.

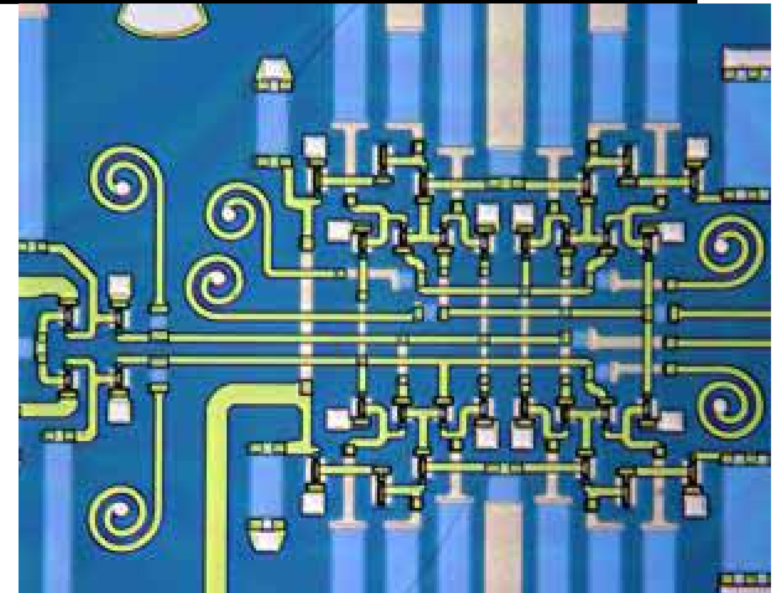
Implications:

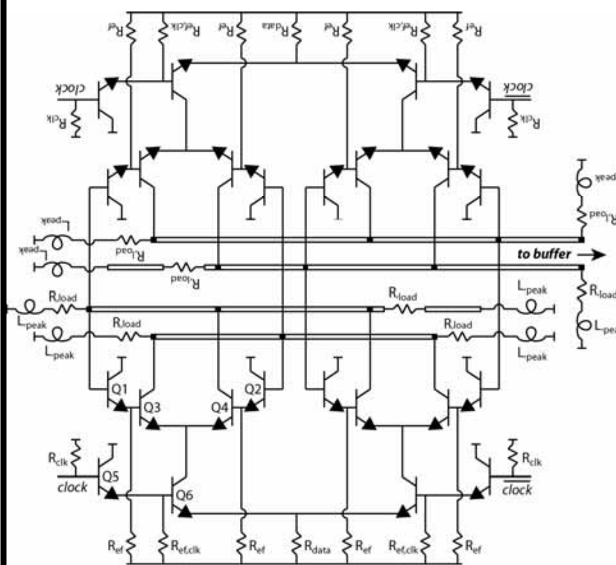
160 Gb/s fiber ICs

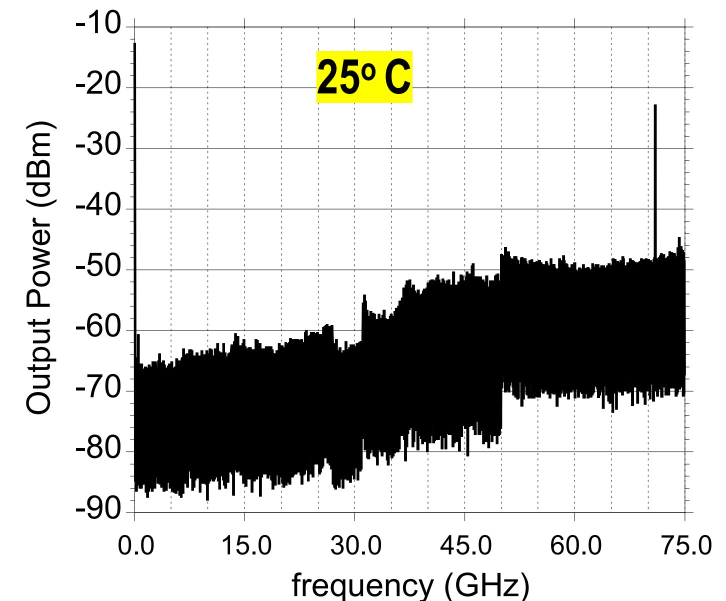
100 + Gb/s serial links

Target is 260 GHz clock rate
at 300 nm scaling generation

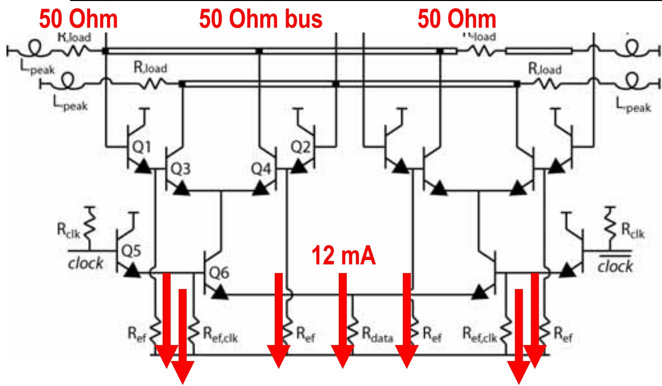




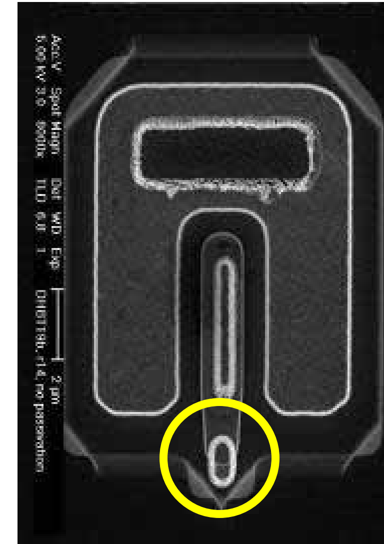


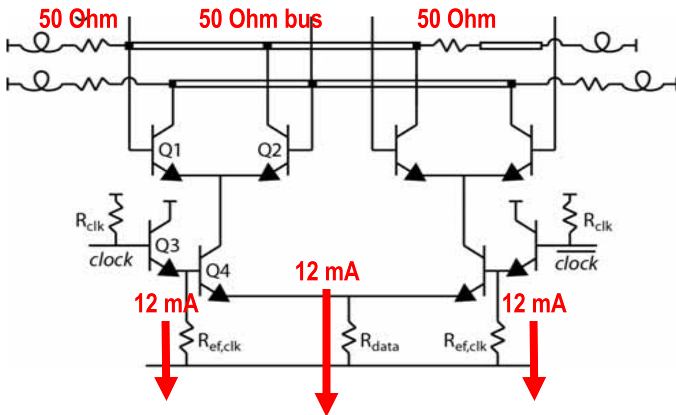


Reducing Digital Circuit Dissipation

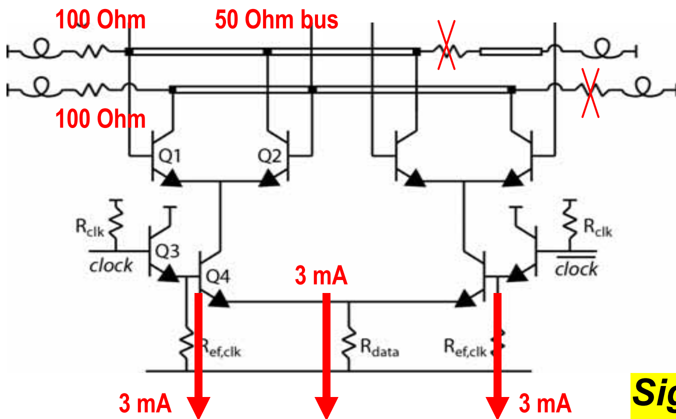


ECL with impedance-matched 50 Ohm bus:
25 Ohm load→ switch 12 mA
12 mA x 7 x 4 V = 336 mW/latch





CML with impedance-matched 50 Ohm bus:
25 Ohm load→ switch 12 mA
12 mA x 3 x 3 V = 108 mW/latch



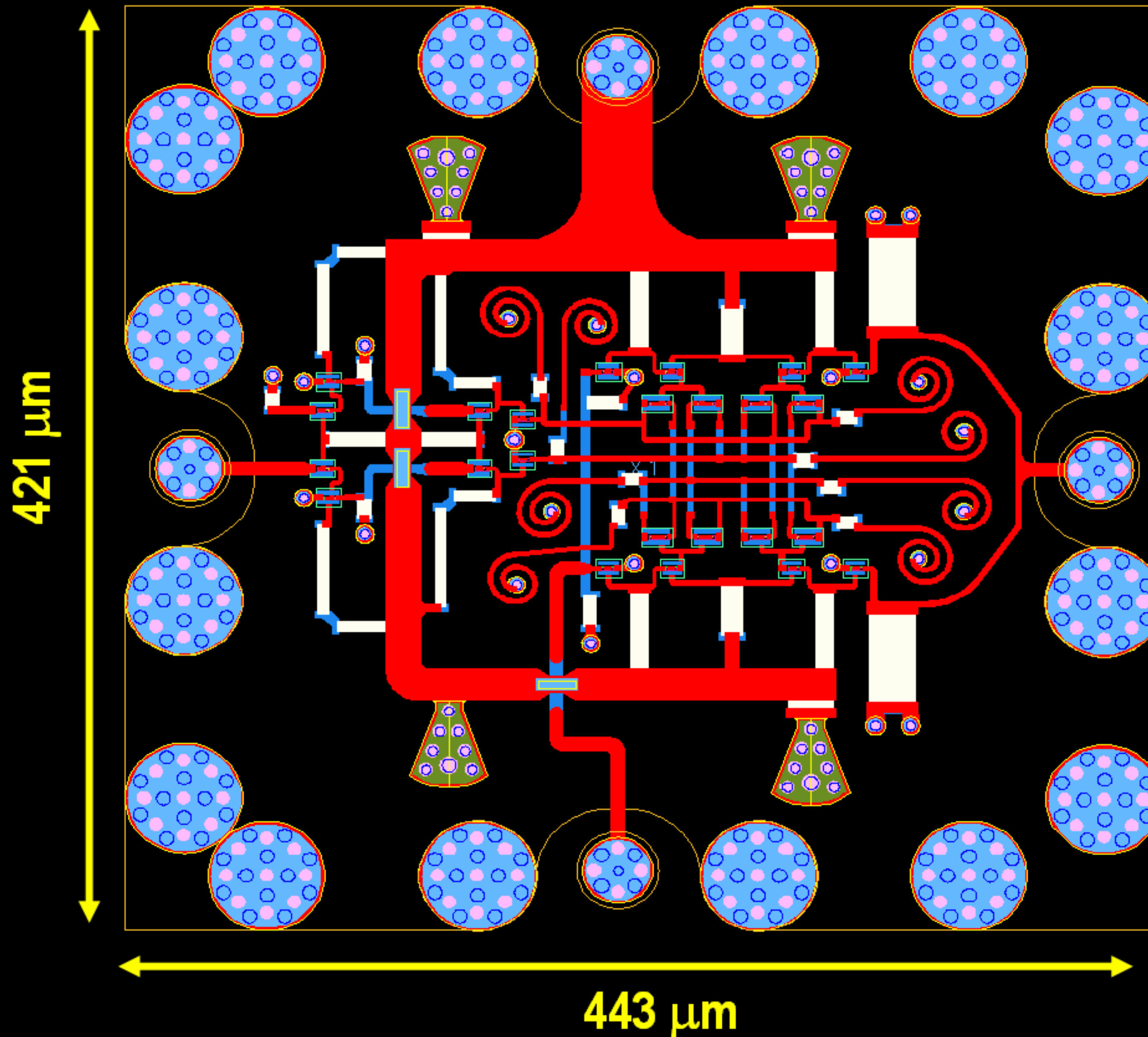
Low-Power CML
100 Ohm loaded → switch 3 mA
3 mA x 3 x 3 V = 27 mW/latch

$$\text{High speed @ low power} = \text{low } C_{wiring}, \text{ low } C_{cb,pad}$$

Significant dissipation in the clock emitter-follower level-shifters; some published work omits this from stated dissipation

Zach Griffith

Low Power CML Static Divider Designs



Simulated divider speed...

Without C_{cb} reduction

A_{jbe} = 3.0 μm², f_{max} = 130 GHz

A_{jbe} = 2.5 μm², f_{max} = 136 GHz

With Implanted Sub-collector

A_{jbe} = 3.0 μm², f_{max} = 143 GHz

A_{jbe} = 2.5 μm², f_{max} = 151 GHz

With Pedestal

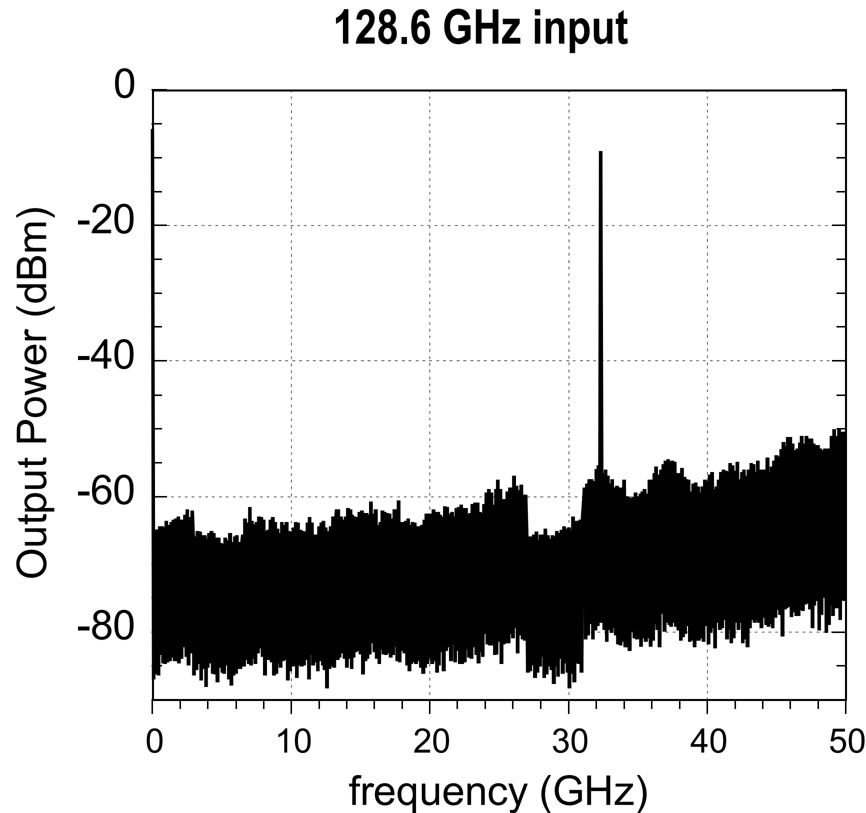
A_{jbe} = 3.0 μm², f_{max} = 156 GHz

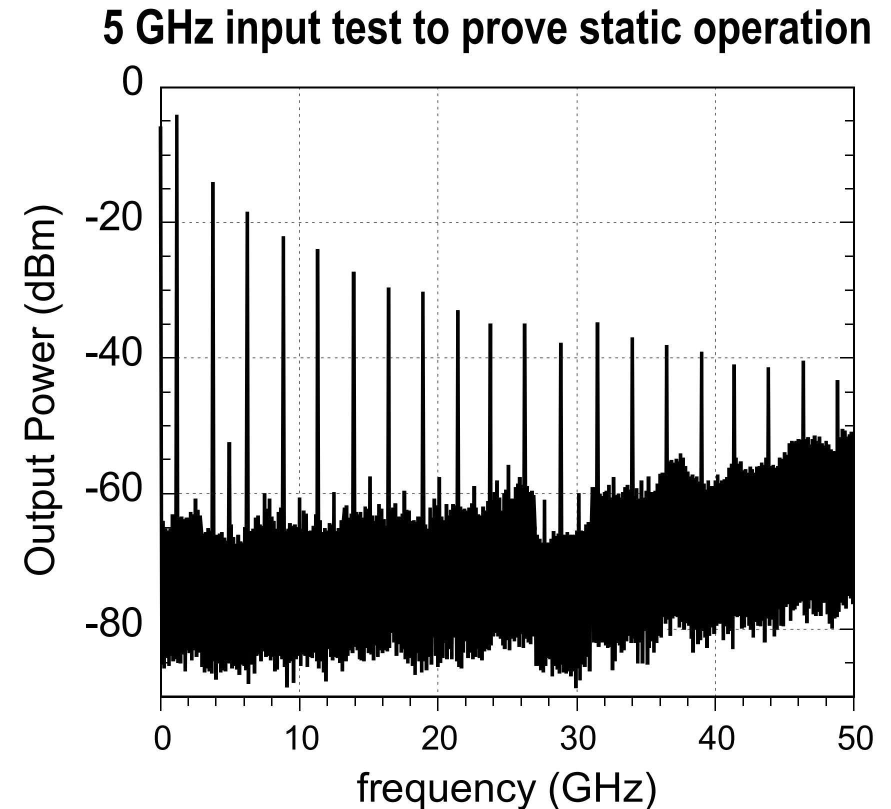
A_{jbe} = 2.5 μm², f_{max} = 164 GHz

$P_{divider\ core,}$ ≈ 214 mW

Zach Griffith

Divide-by-4 at 128.6 GHz, S^3 RSC Technology

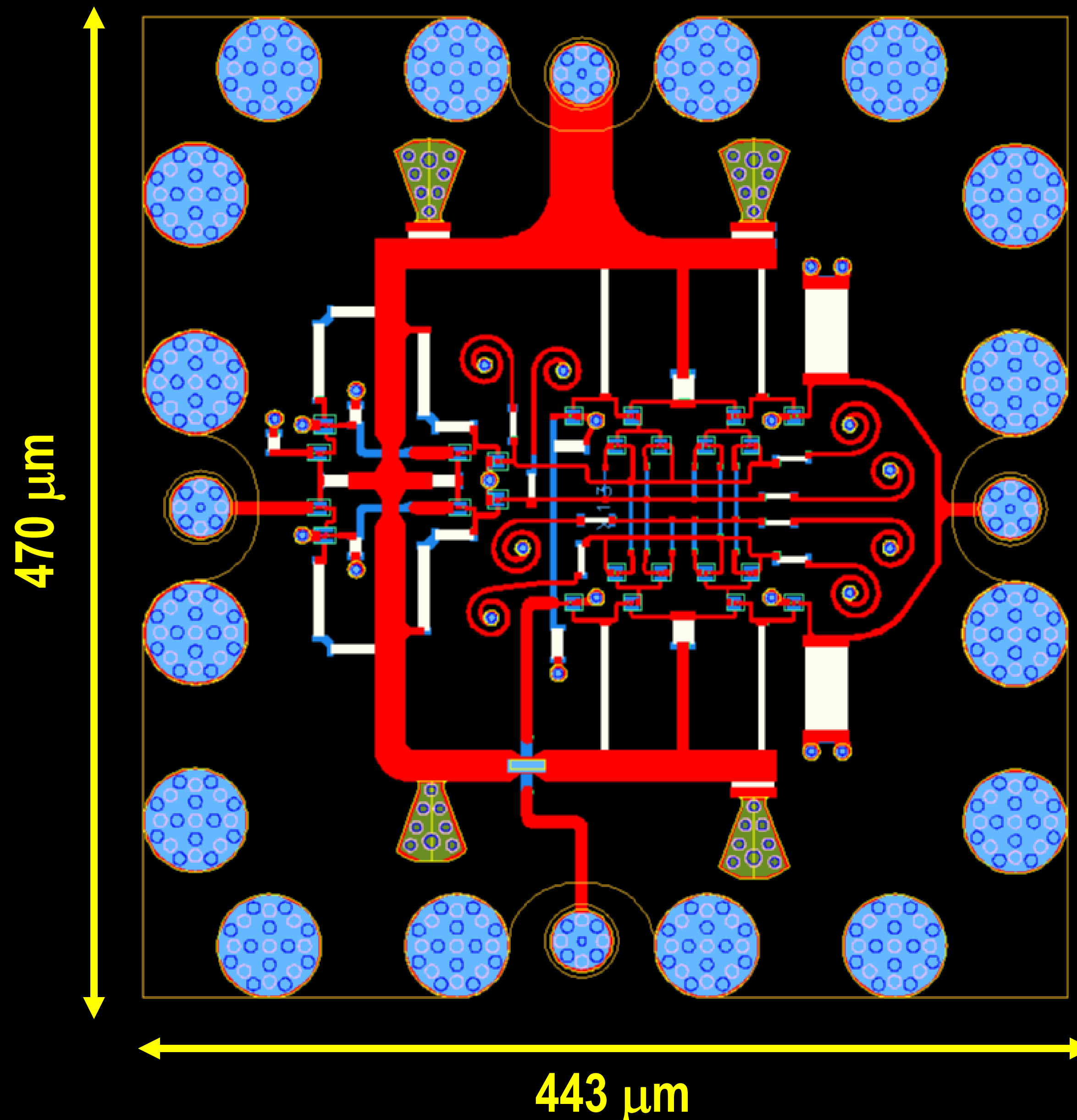




Measurements performed at UCSB, GUNN Source Used For CLK Input
RSC Wafer # xxxx, Divider ID: R3C2 #5A, Fabricated at RSC, Design at UCSB
$V_{clk\ offset}$ = -0.45 V, $V_{EE,\ div1,2}$ = -3.4 V, $I_{EE,\ total}$ = 192 mA – $I_{div1,2}$ at $f_{clk,max}$ ≤ 65 mA per divider ckt
Power dissipation of input divider core w/out output buffer < 221 mW — room temp, no cooling

Zach Griffith

Ultra Low Power CML Static Divider Design



Simulated divider speed…

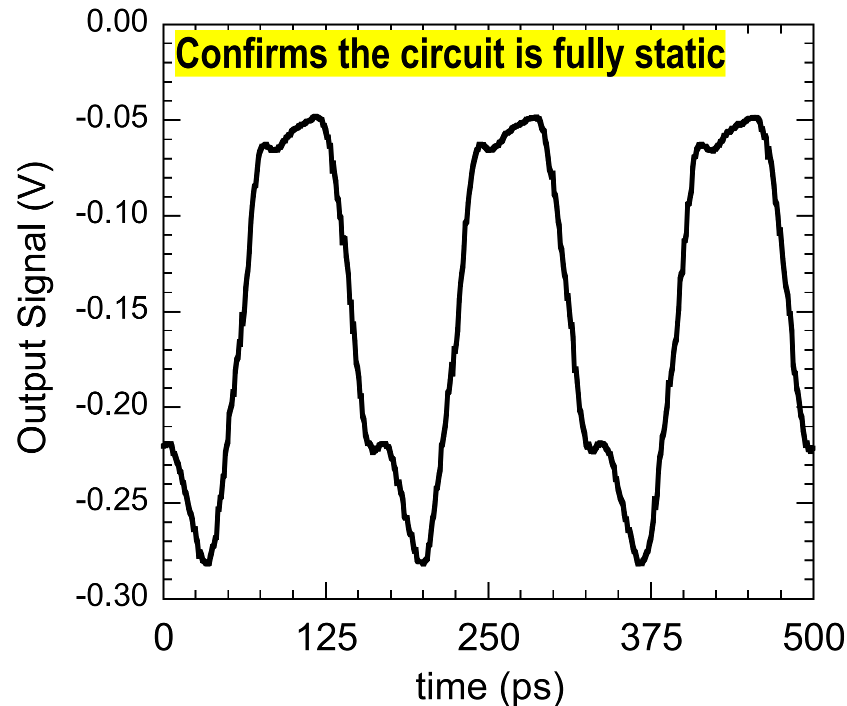
With Collector Pedestal

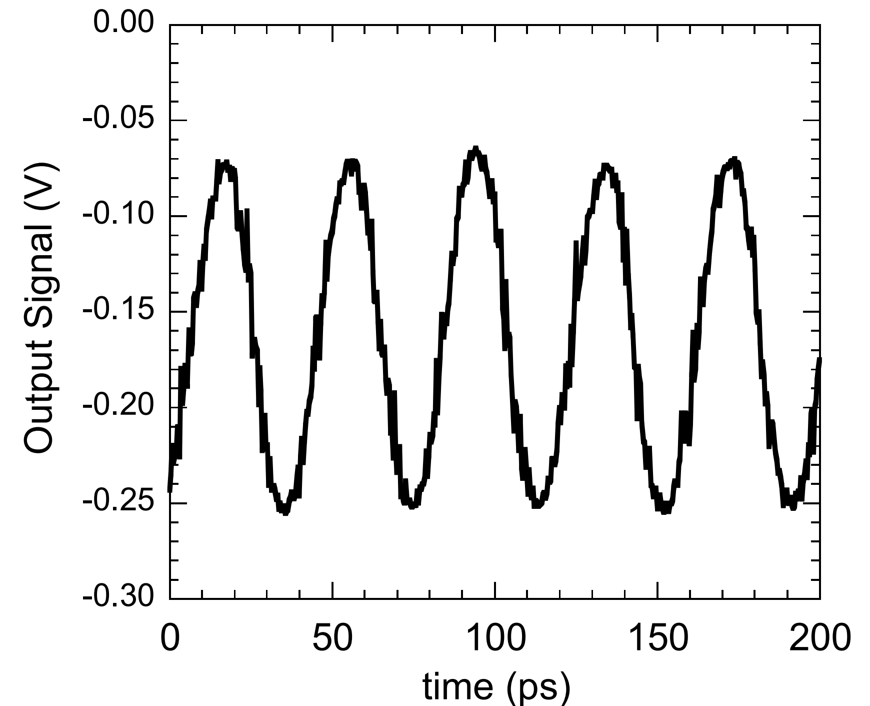
A_{jbe} = 1.0 µm^2, f_{max} = 100 GHz

$P_{divider\ core,}$ ≈ 31 mW

Zach Griffith

Ultra low-power RSC / UCSB CML dividers





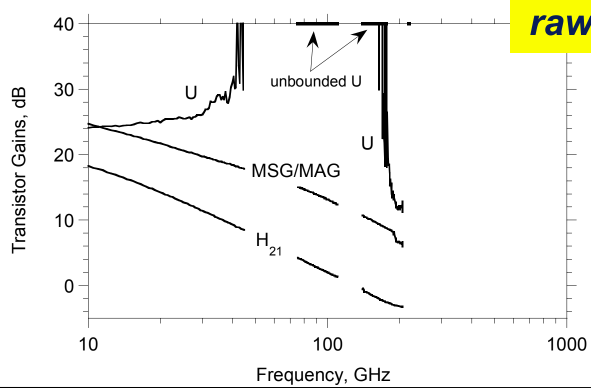
The divider is operational from 12 GHz to 51 GHz

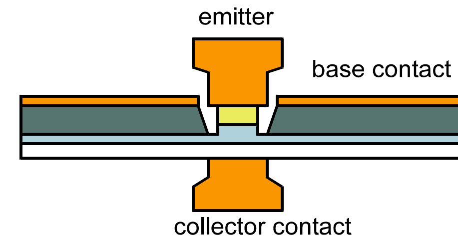
At f_{clk} = 51 GHz, $P_{flip\text{-}flop}$ = 29.2 mW → Latch power × delay = 143 fJ, no emitter followers = 79.0 fJ

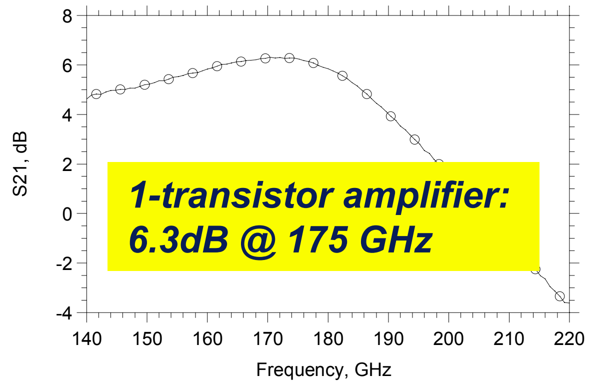
M. Urteaga

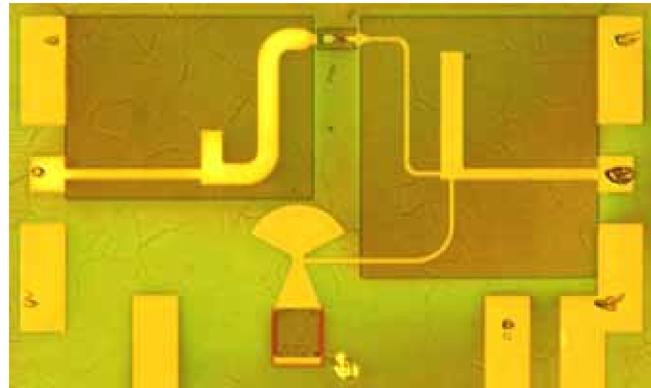
Deep Submicron Bipolar Transistors for 140-220 GHz Amplification

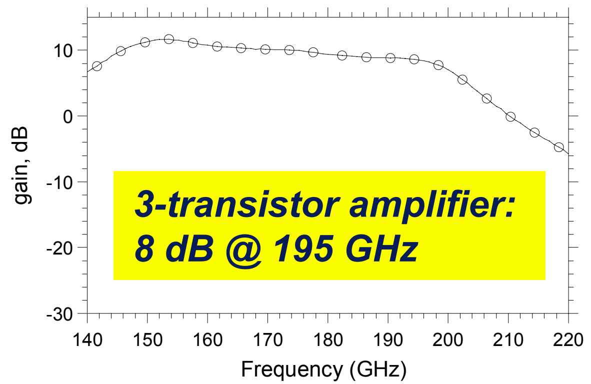
raw 0.3 μm transistor: high power gain @ 200 GHz

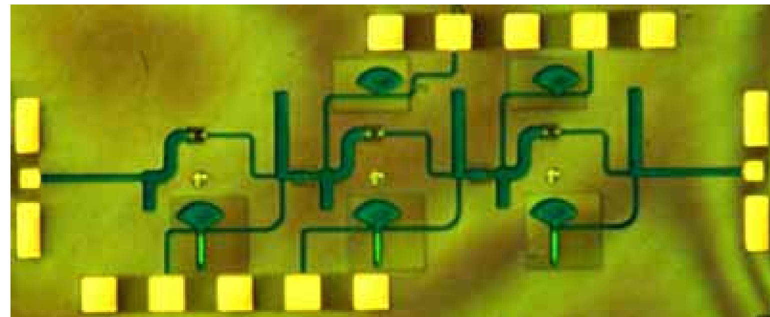






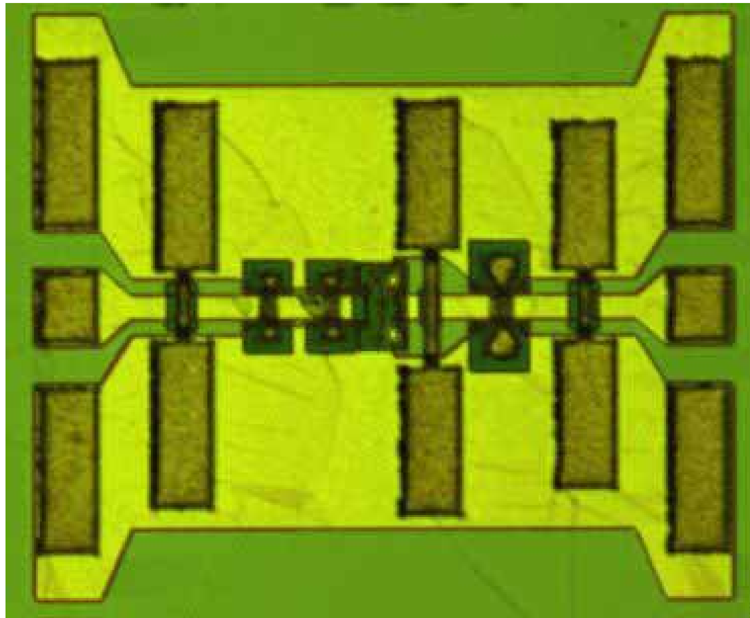


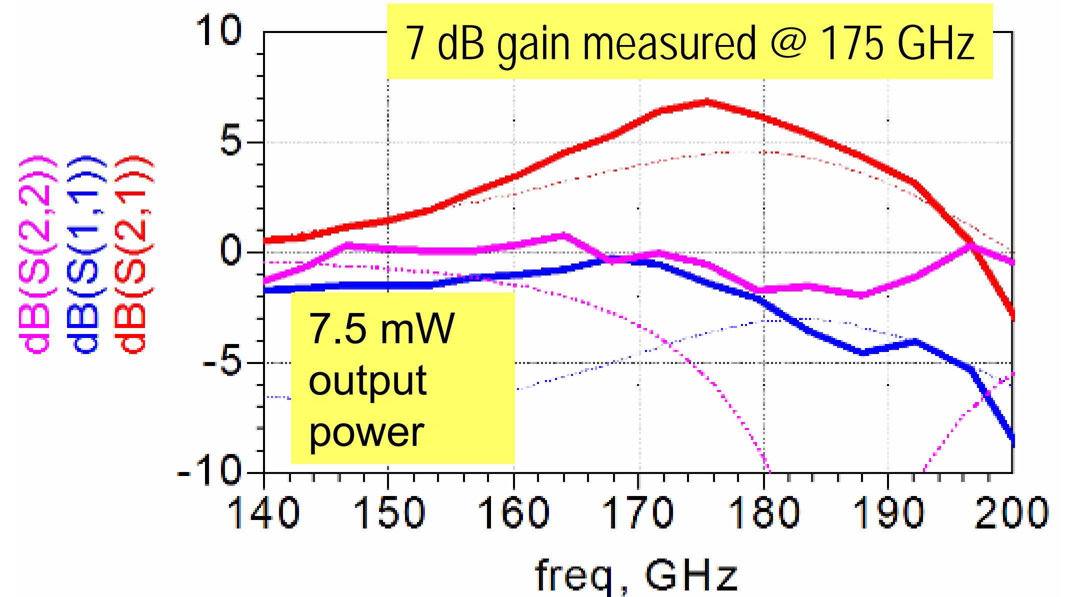




V. Paidi, Z. Griffith, M. Dahlström

Mesa DHBT Power Amplifiers for 100-200 GHz Communications





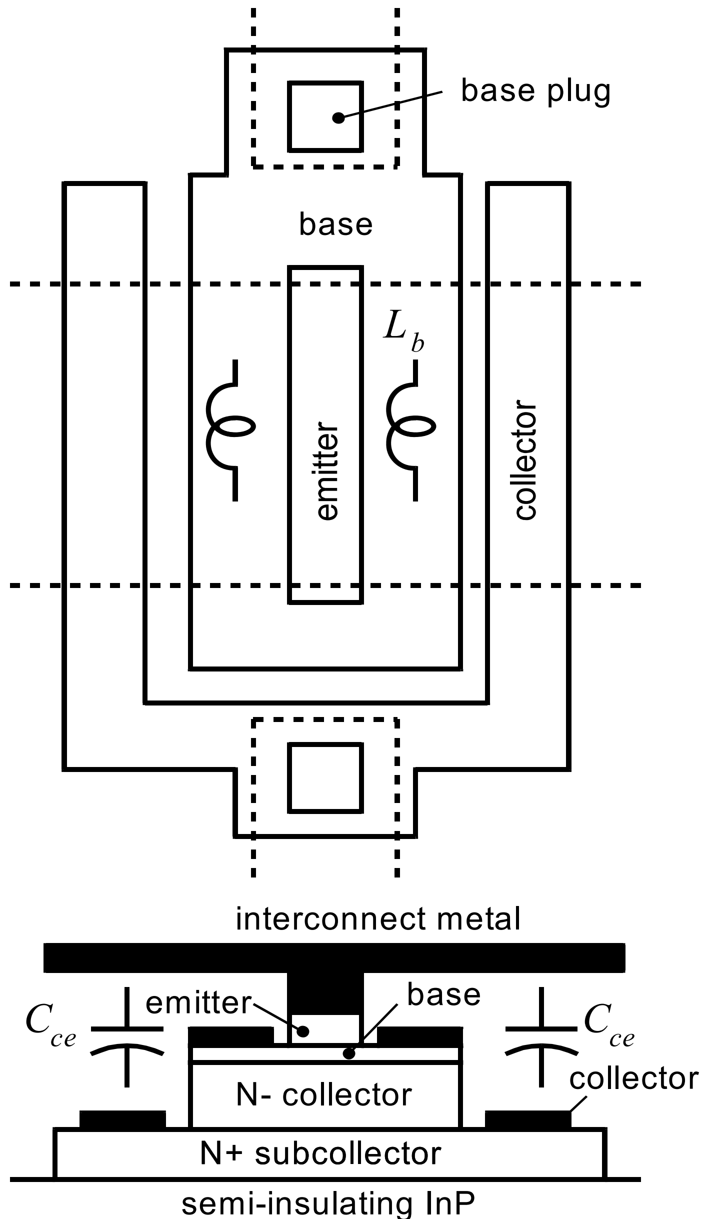
175 GHz Power Amplifier Demonstrated in a 300 GHz fmax process

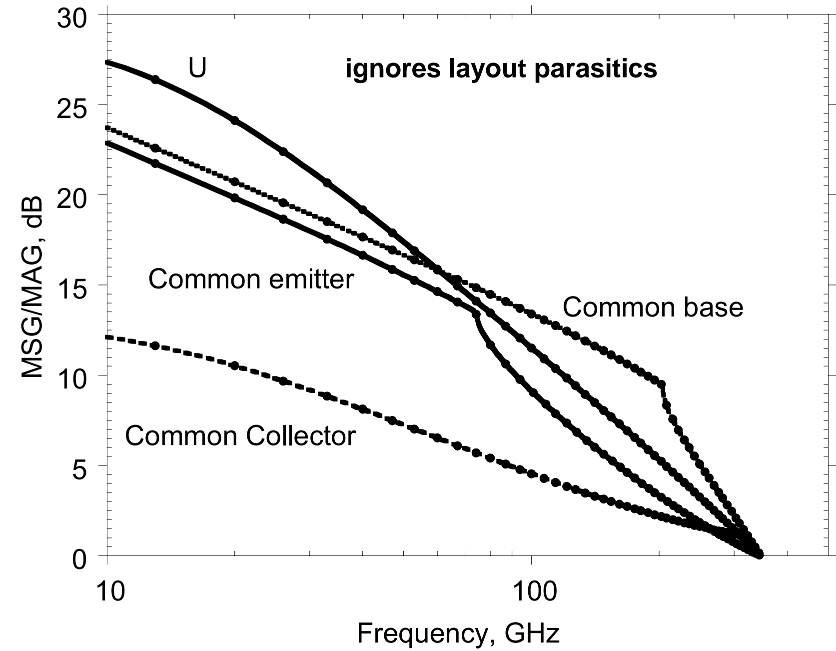
500 GHz f_{max} DHBTs available now, 600 GHz should be feasible soon

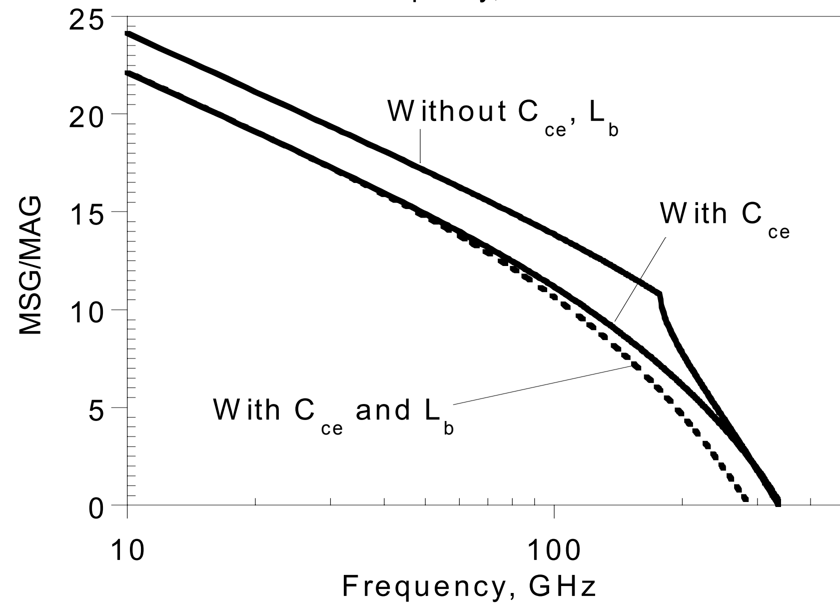
- → ***feasibility of power amplifiers to 350 GHz***
- → ***Ultra high frequency communications***

2 fingers x 0.8 um x 12 um, ~250 GHz f_τ, 300 GHz f_{max} , V_{br} ~ 7V, ~ 3 mA/um^2 current density

Common-Base Has Highest Gain, but Layout Parasitics Matter !

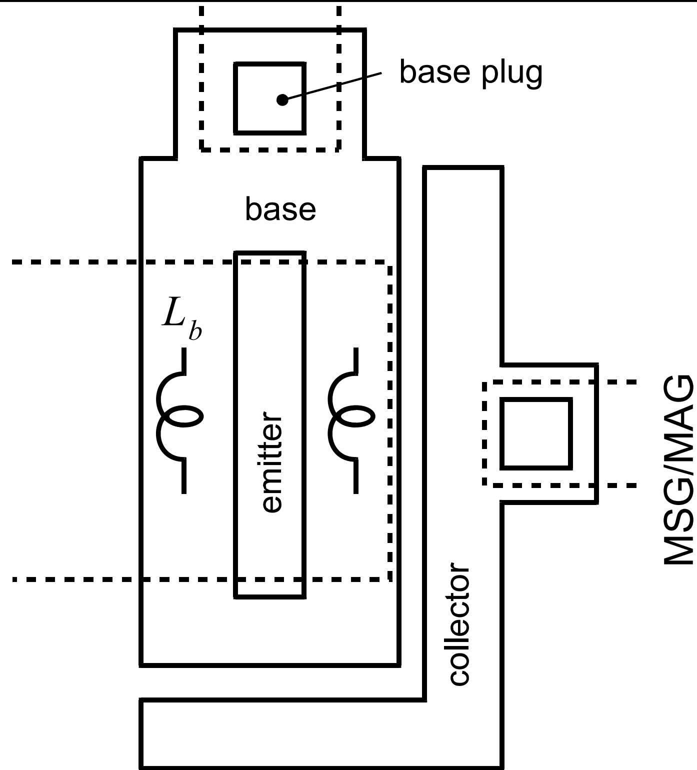


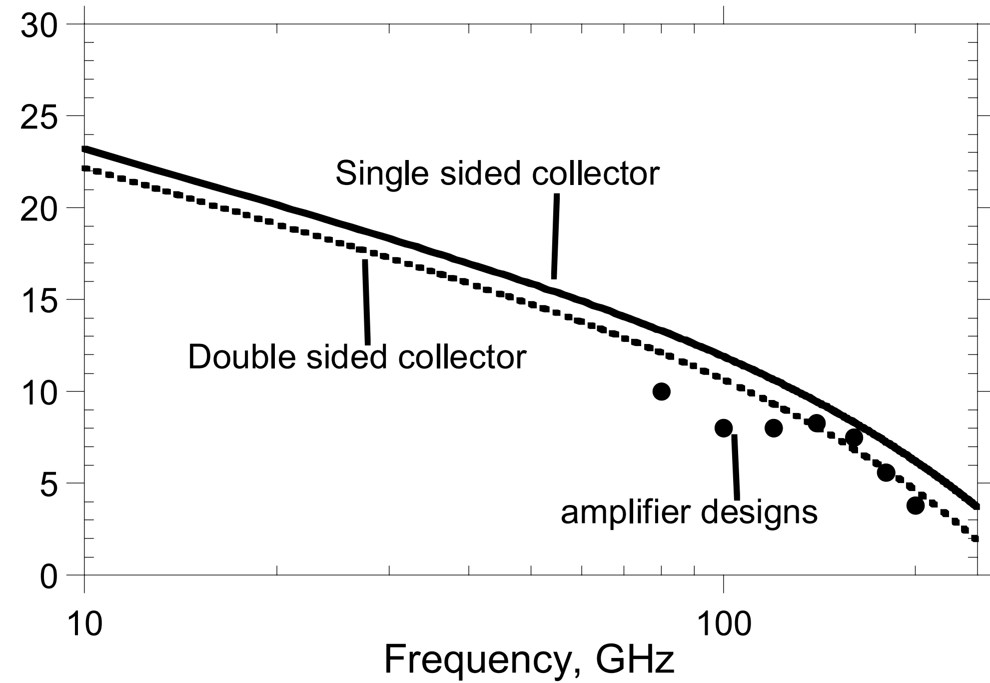


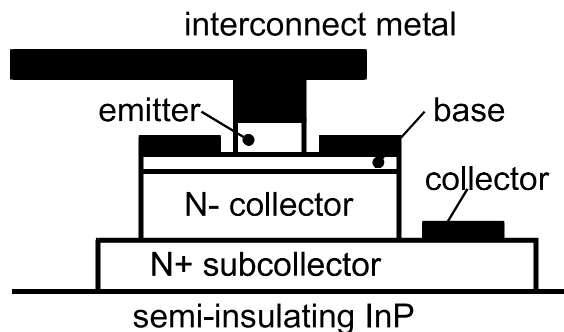


V. Paidi, Z. Griffith, M. Dahlström

Single-Sided Collector Contacts Improve Common-Base Gain

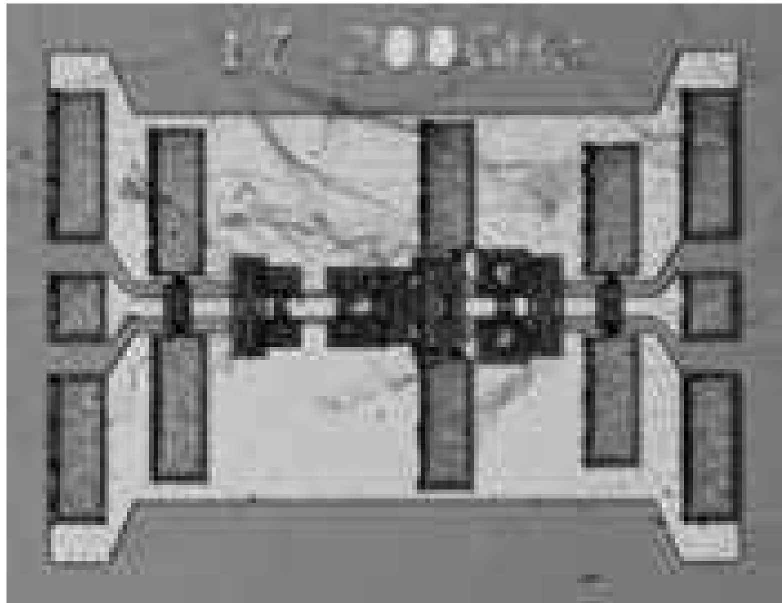


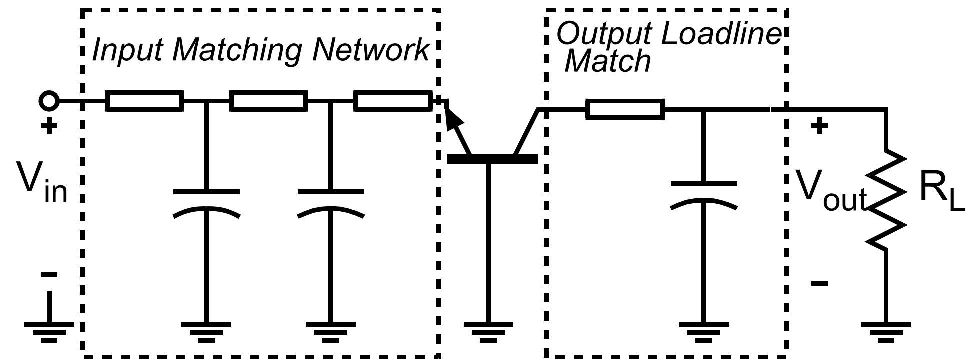




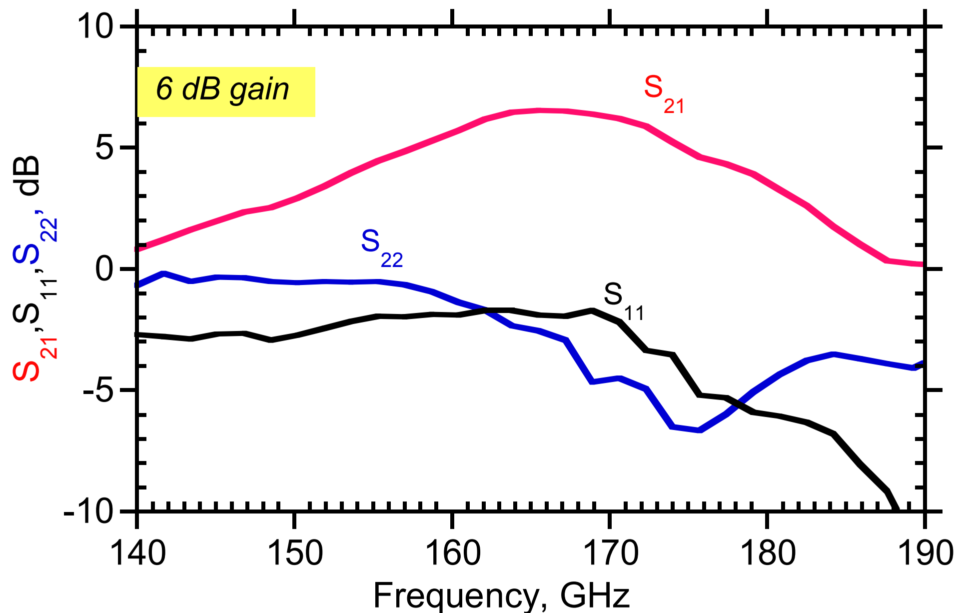
V. Paidi, Z. Griffith, M. Dahlström

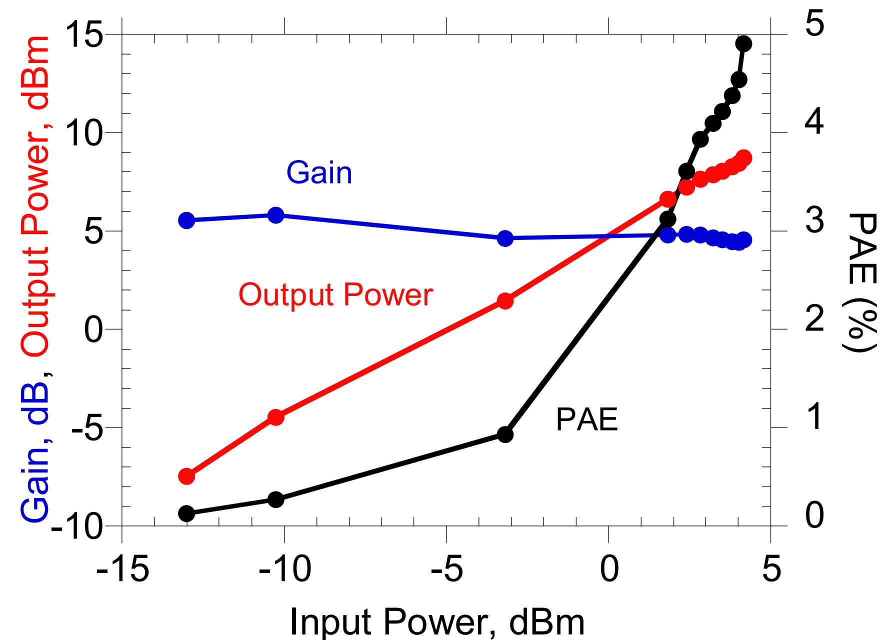
172 GHz Common-Base Power Amplifier





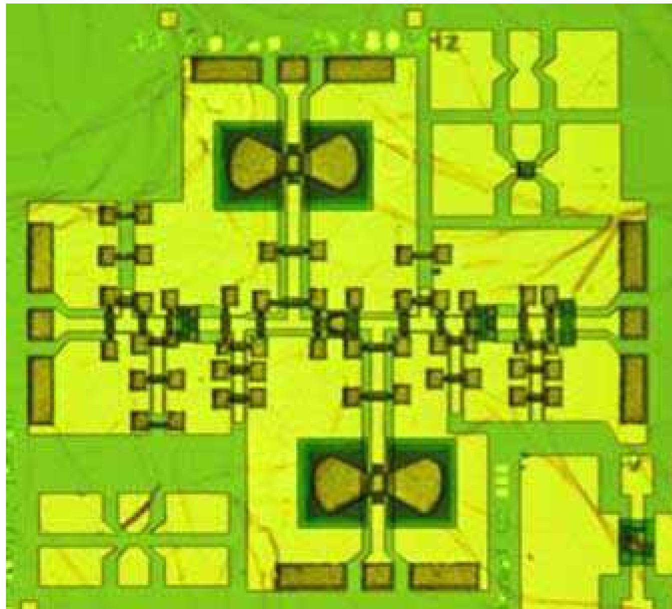
8.3 dBm saturated output power
4.5-dB associated power gain at 172 GHz
DC bias: Ic=47 mA, Vcb=2.1V.





176 GHz Two-Stage Amplifier

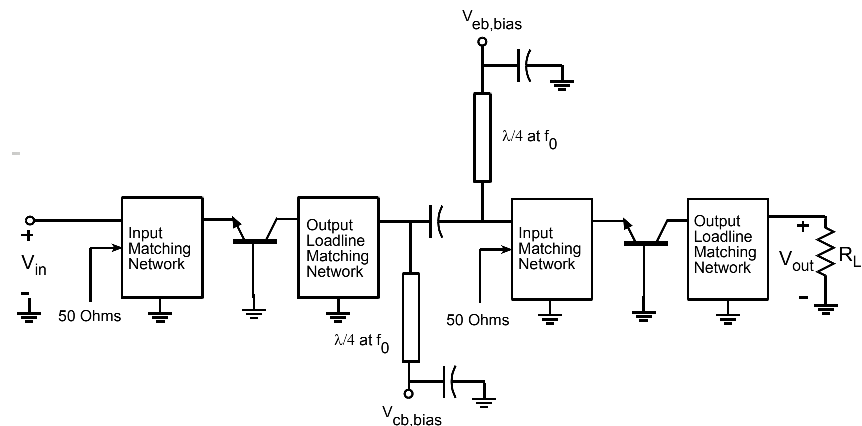
V. Paidi, Z. Griffith, M. Dahlström

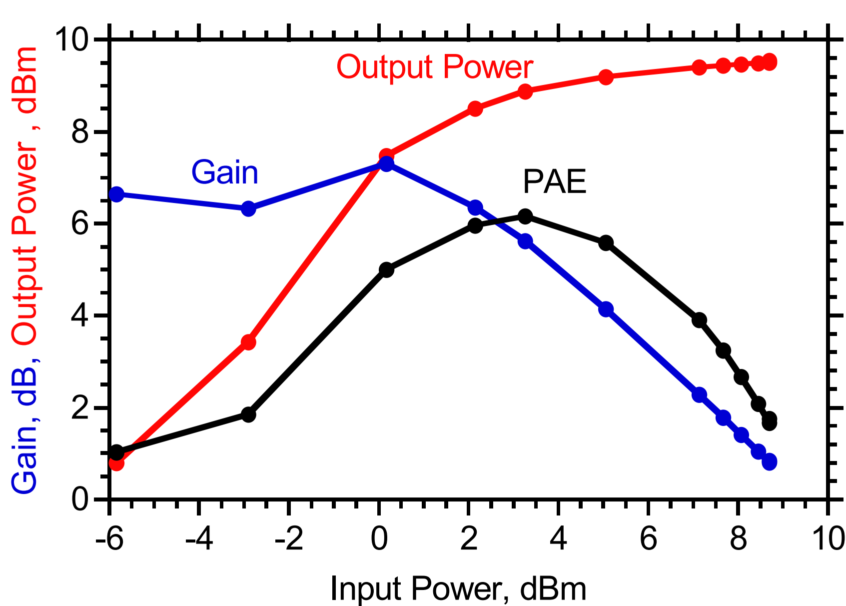


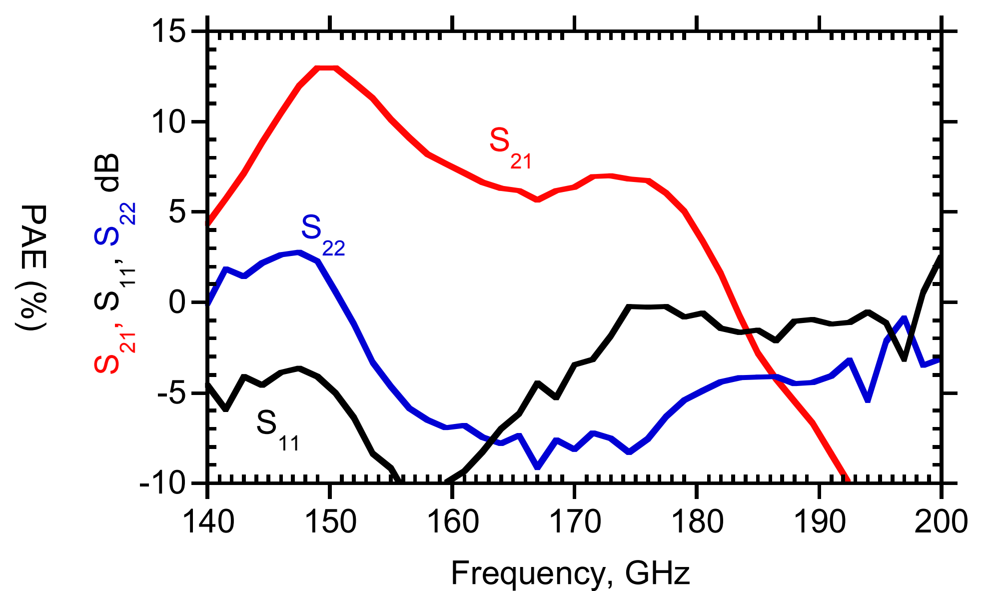
7-dB gain at 176 GHz

8.1 dBm output power, 6.3 dB power gain at 176 GHz

9.1 dBm saturated output power at 176 GHz

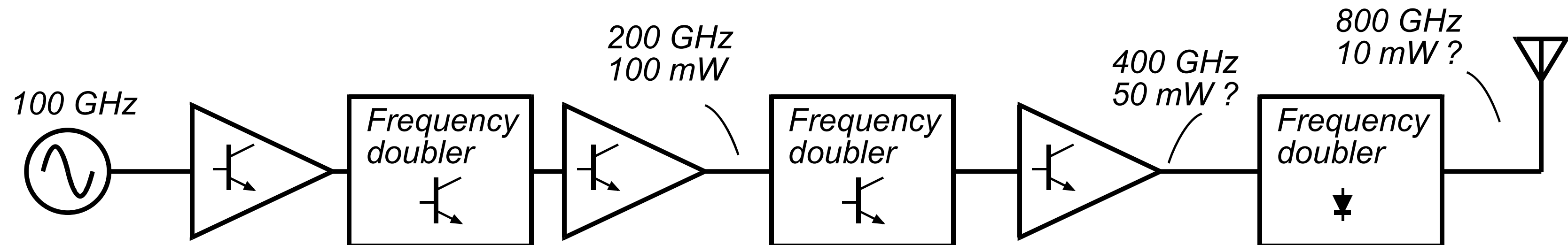




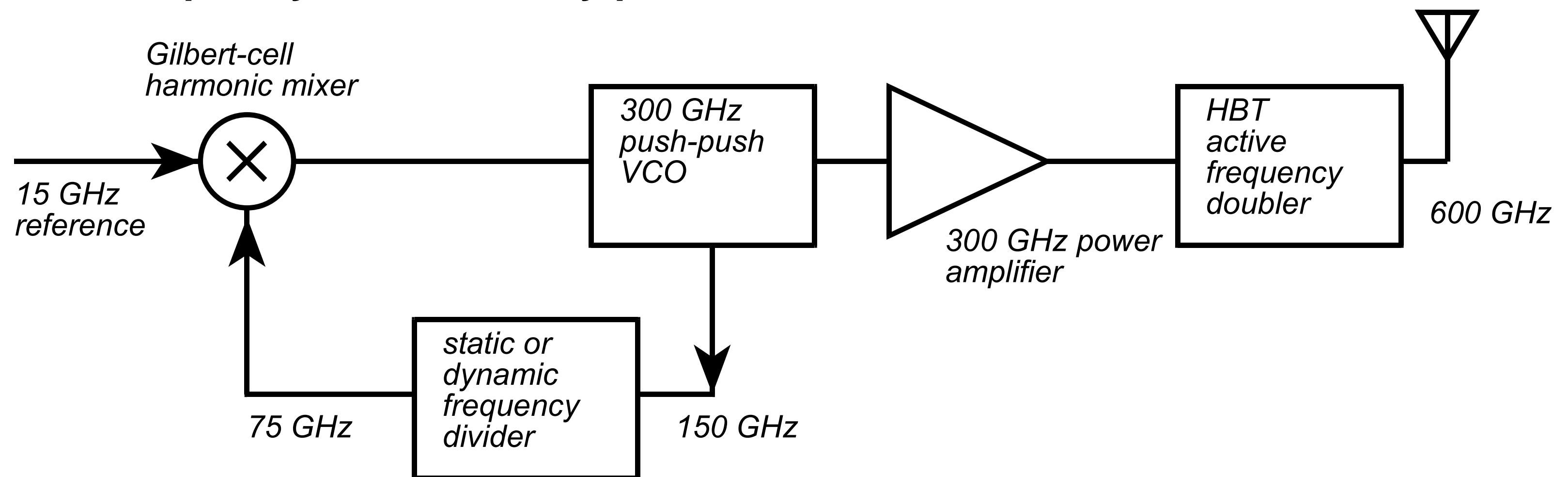


Transistor ICs → compact sub-mm-wave systems

Compact, Single-Chip Monolithic Frequency Multiplier Chains



Sub-mm-wave Frequency Generation by phase-locked source

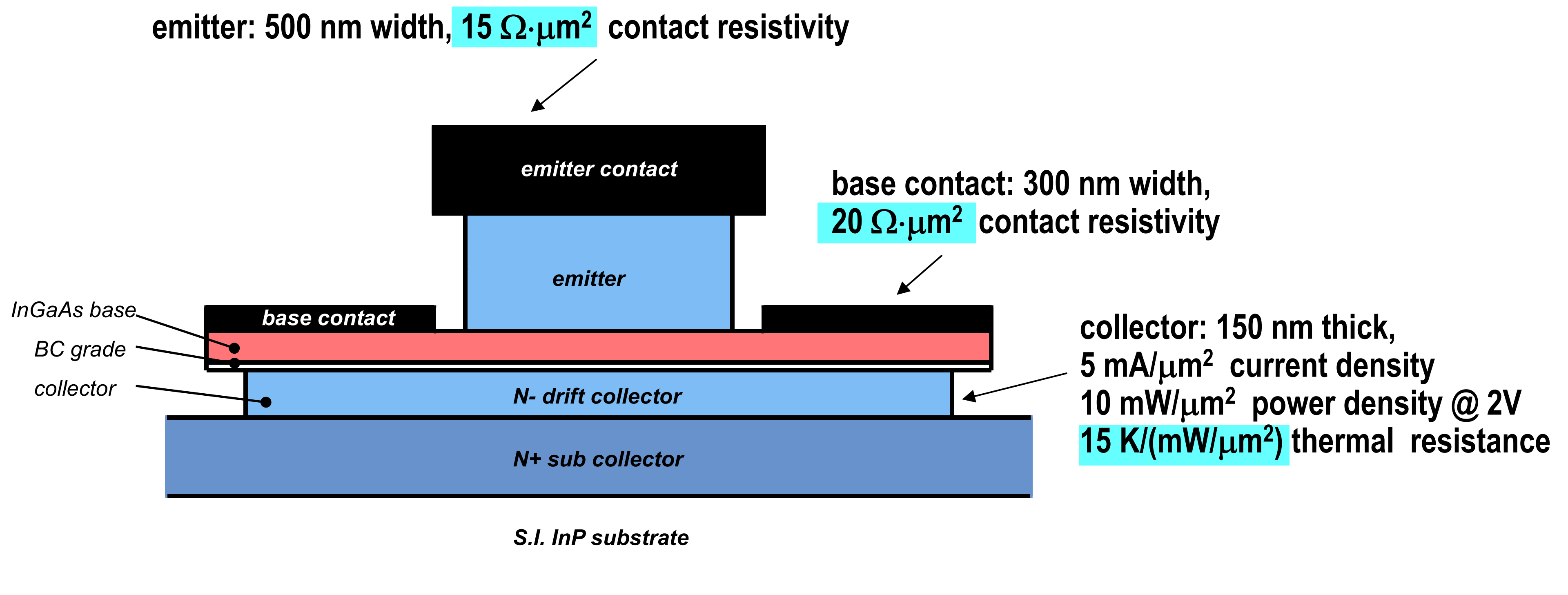


Today: InP DHBTs @ 500 nm Scaling Generation

Device Performance:~ 400 GHz f_τ and ~500 GHz f_{max}

Has enabled 150 GHz digital clock rate (static dividers)

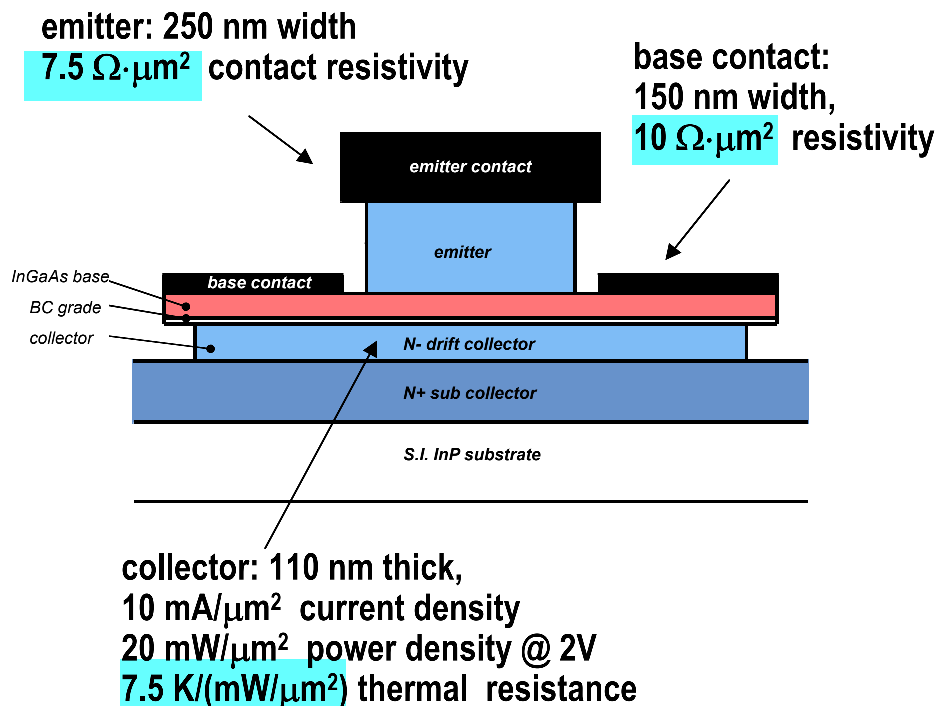
Should enable 300 GHz power amplifiers (175 GHz realized with 300 GHz fmax)



Next: 250 nm Scaling Generation, 1.414:1 faster

Goals: 500 GHz f_τ and 700 GHz f_{max}
230 GHz digital clock rate (static dividers)
400 GHz power amplifiers

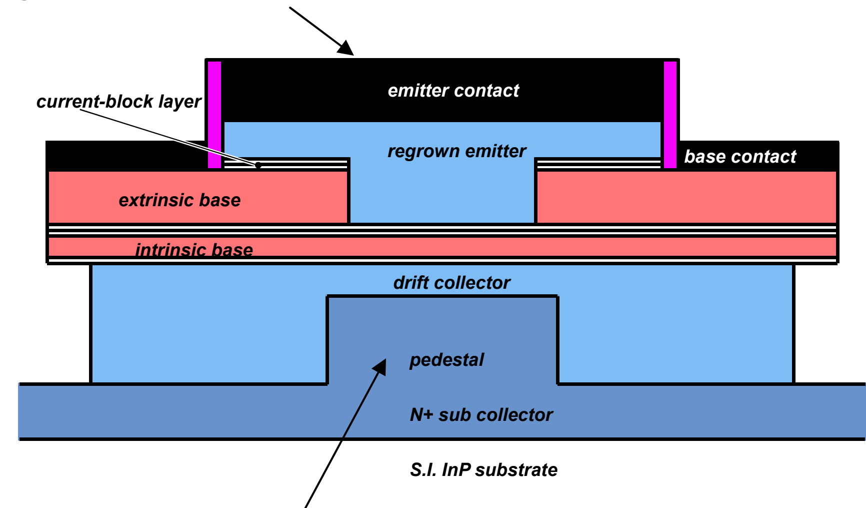
Direct, brute-force scaling



Requires innovations in emitter & base contacts: processes & metallurgy

Parasitic Reduction

regrown emitter with wide contact: reduces access resistance

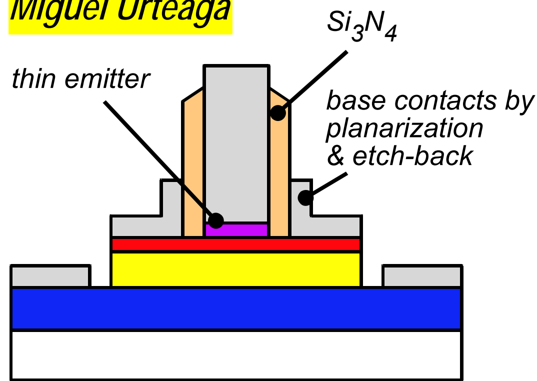


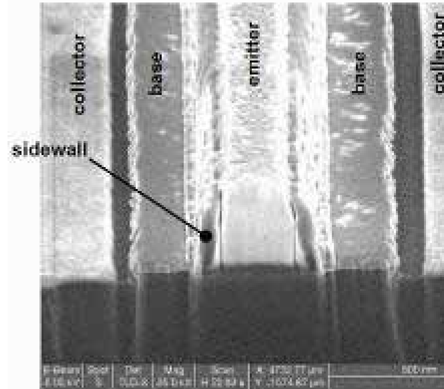
collector pedestal:
reduces capacitance under base contacts,
allows wider & more resistive base contacts

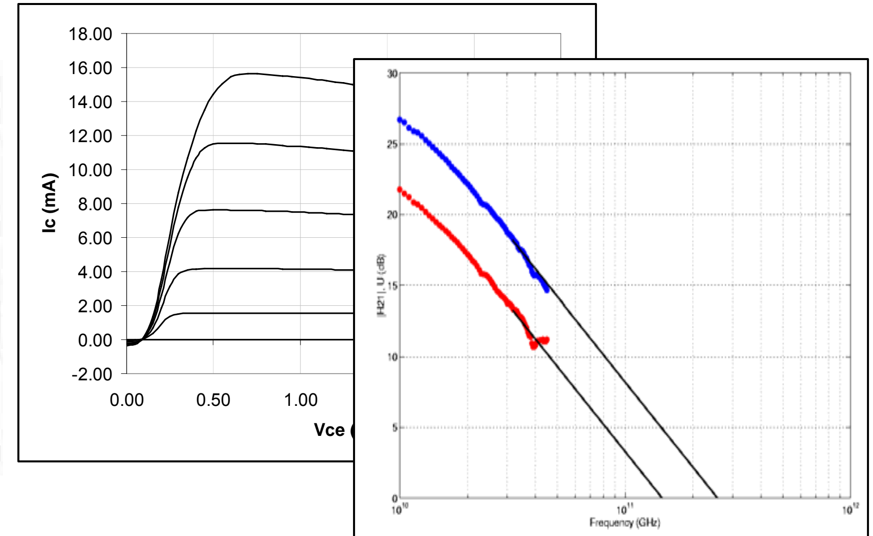
Requires implants and regrowth processes

Manufacturable Emitter Dielectric Sidewall Processes

First-Generation: UCSB and Rockwell Scientific
Miguel Urteaga



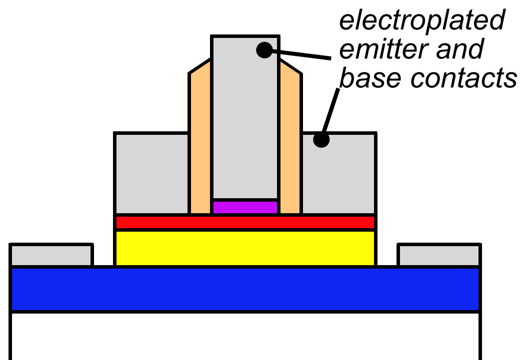


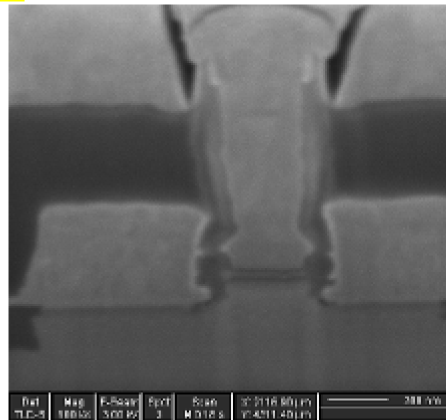


Urteaga, Rodwell , Pierson, Rowell , Brar, Nguyen, Nguyen: UCSB, RSC, GCS

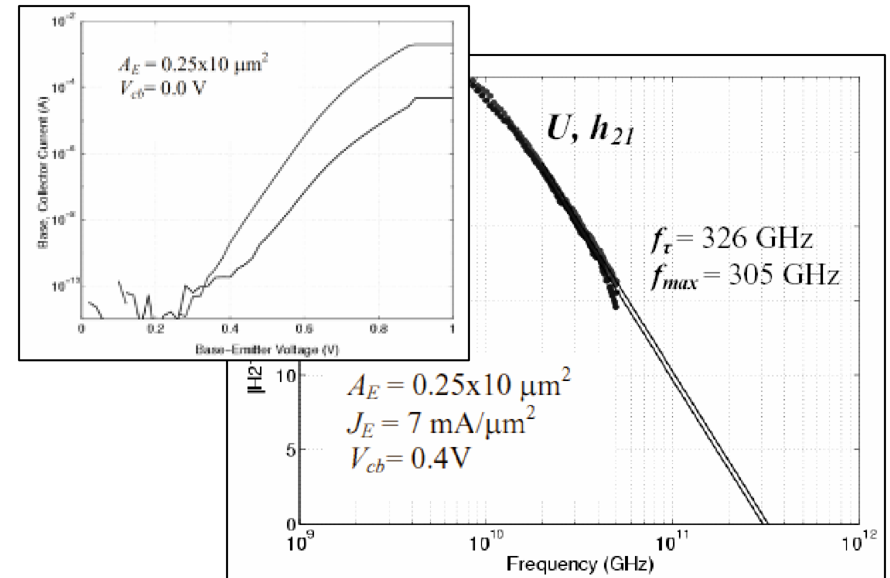
266 GHz f_t, 133 GHz f_{max}, , C_{cb}/I_c=0.4 ps/V

2nd-Generation: Rockwell Scientific
Miguel Urteaga, Petra Rowell





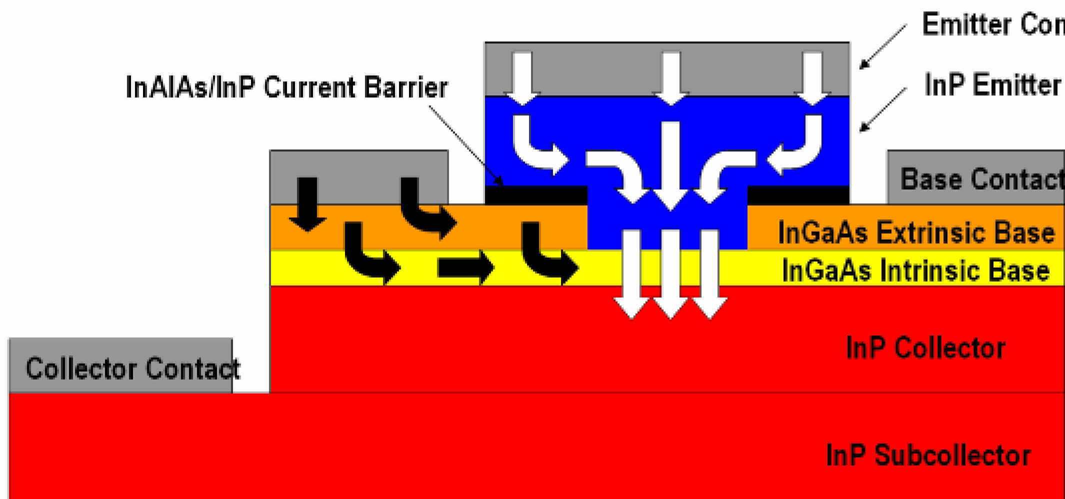
250 nm emitter

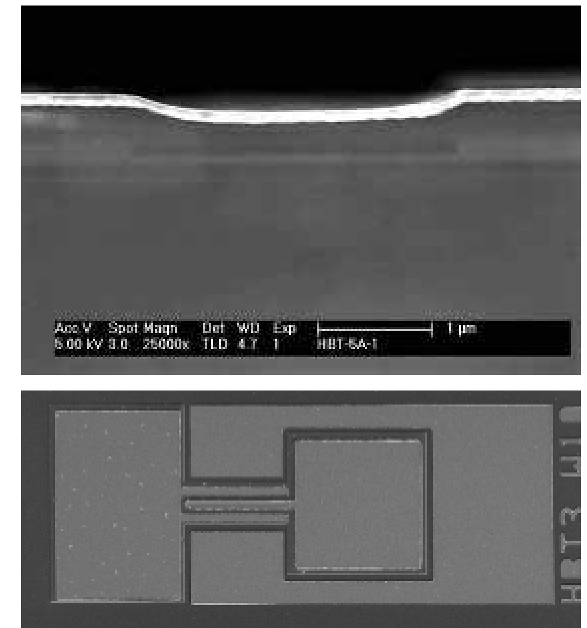


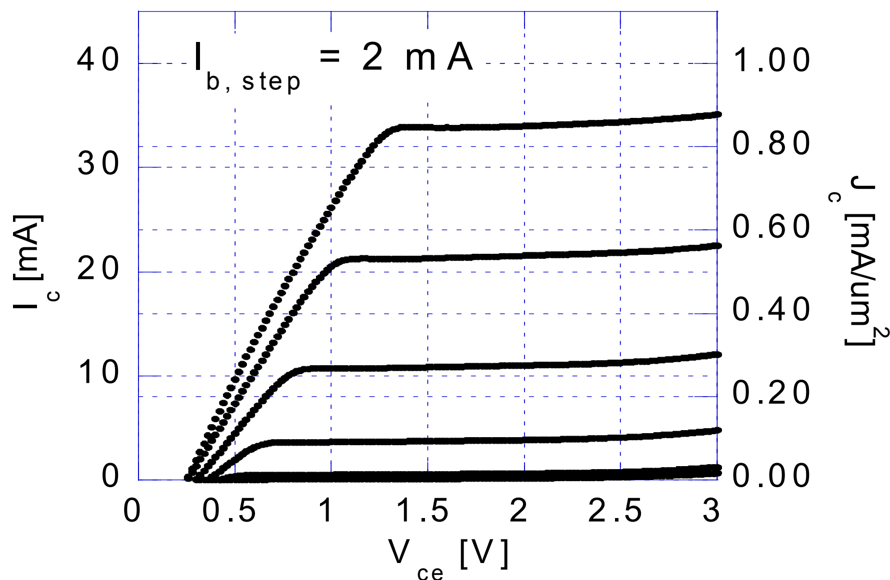
Urteaga, Rowell, Pierson, Brar: RSC

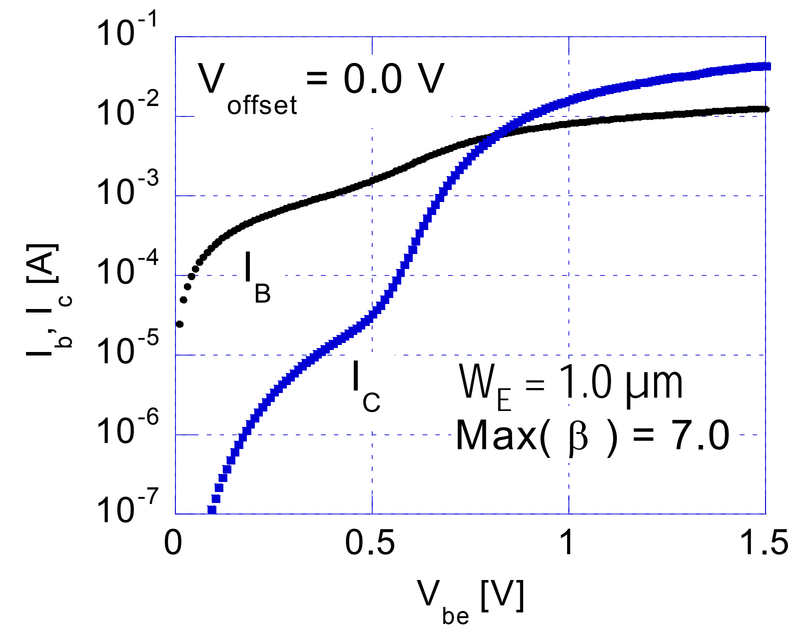
HBT with Epitaxial Extrinsic Emitter

C. Kadow



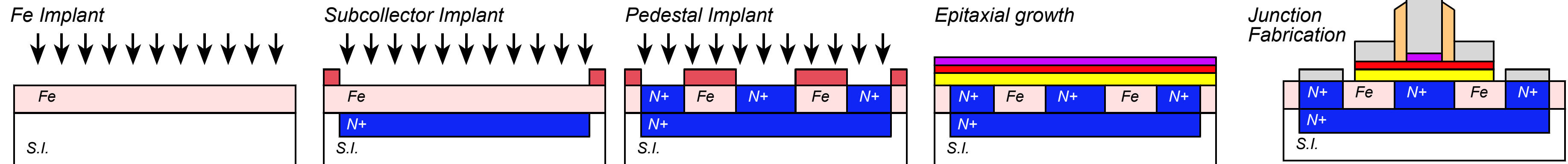


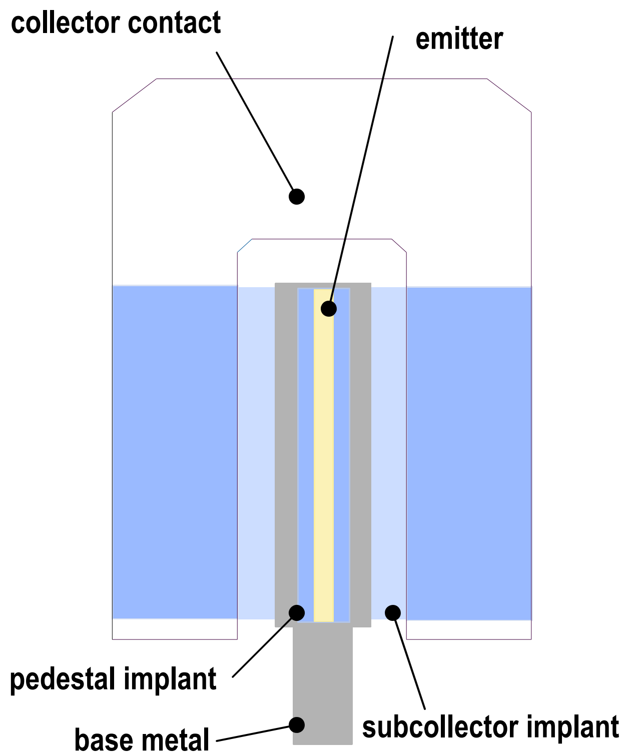


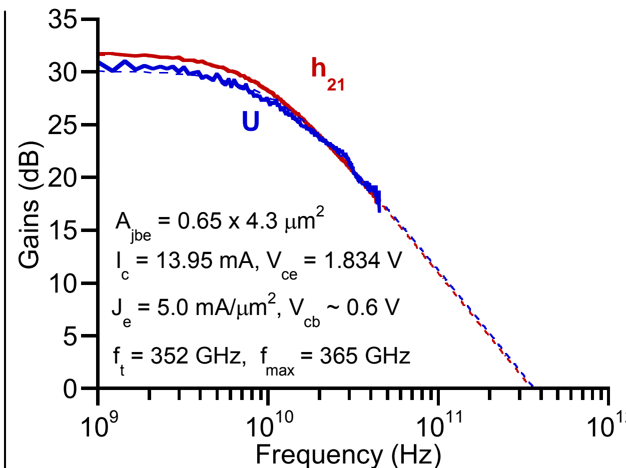


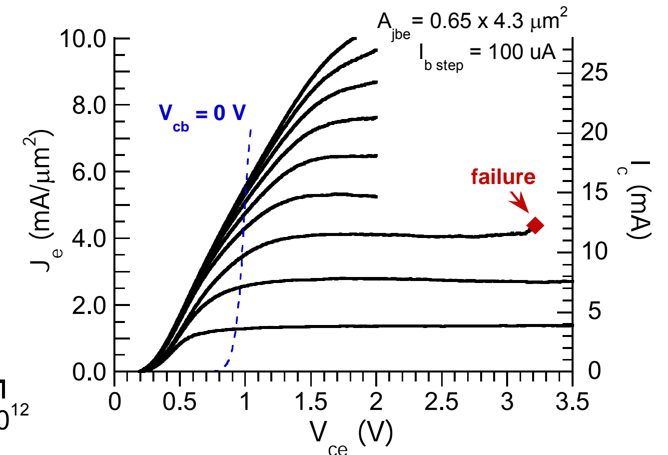
Navin Parthasarathy

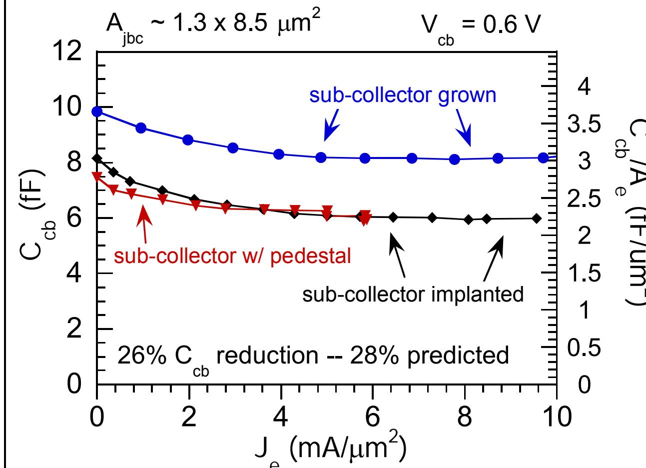
Subcollector & Pedestal Implant

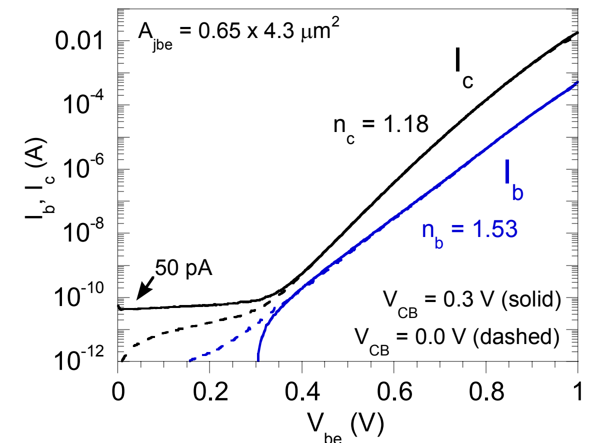












Subcollector implant eliminates C_{cb} in base pad area -key for high speed in lower-power logic.

Pedestal further reduces C_{cb}.

Roadmap for the 125 nm Scaling Generation

Target transistor performance: 700 GHz f_τ , 1100 GHz f_{max} ,

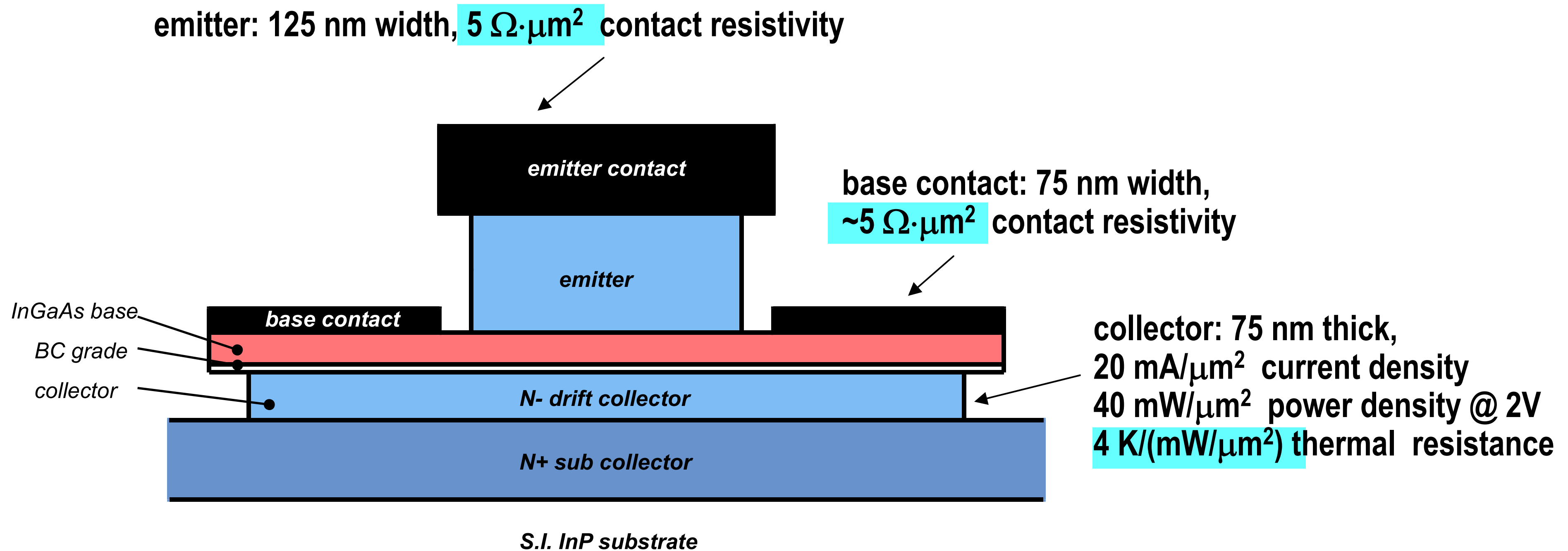
comparable improvement of other key parameters: $C_{cb}\Delta V/I_c$, $R_{ex}I_c/\Delta V$, $R_{bb}I_c/\Delta V$

Target circuit performance

330 GHz digital clock rate (static dividers)

600 GHz power amplifiers

What would be needed to obtain this ?



Indium Phosphide HBTs for 100-600 GHz ICs

InP HBT now: at 500 nm scaling generation

455 GHz f_t & 485 GHz f_{max}

150 GHz static dividers & 180 GHz amplifiers demonstrated

200 GHz digital latches & 300 GHz amplifiers are feasible

InP HBT: future, at 125 nm scaling generation

2:1 increase in bandwidth (?)

700 GHz f_t & 1.1 THz f_{max} , 330 GHz digital latches & 600 GHz amplifiers ?

demands 4:1 better Ohmic contacts

demands 4:1 increased current density.

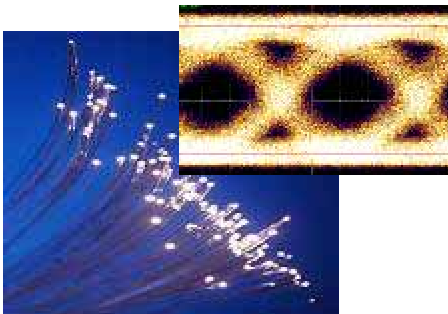
Applications:

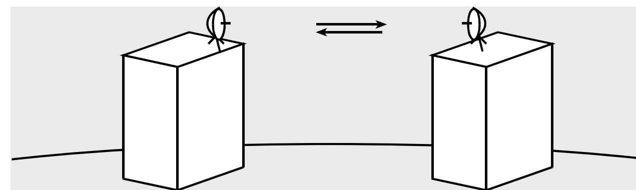
160+ Gb/s fiber ICs,

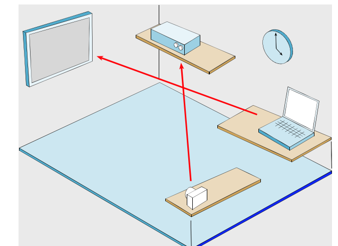
300 GHz MIMICs for communications, radar, & imaging

GHz ADCs / DACs / DDFS / etc.

& applications unforeseen & unanticipated

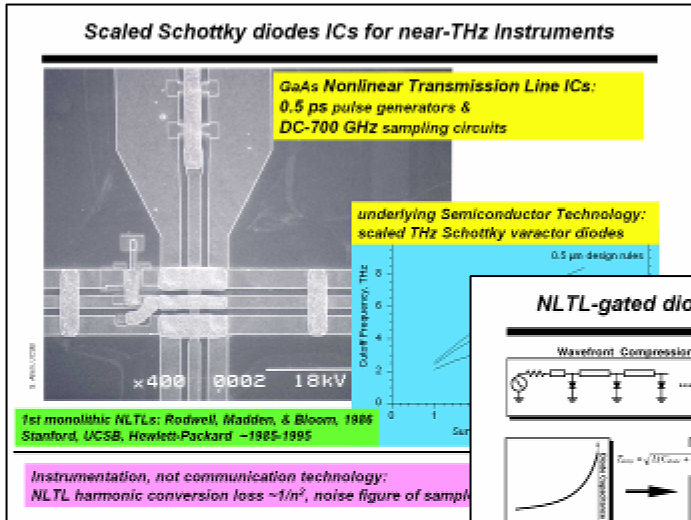


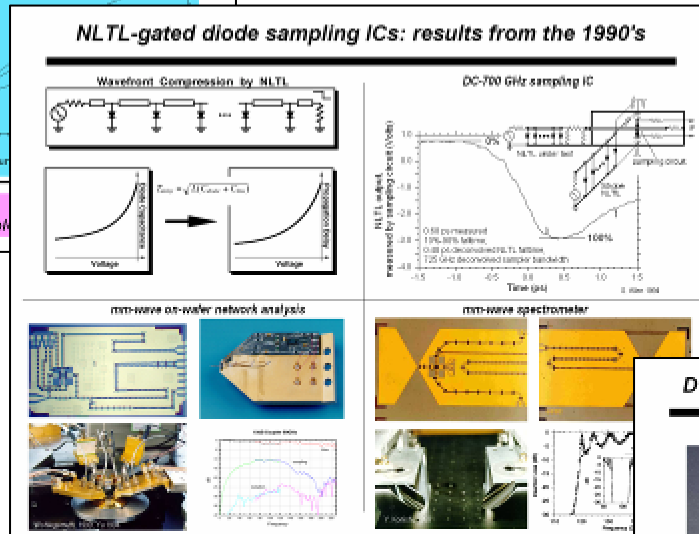


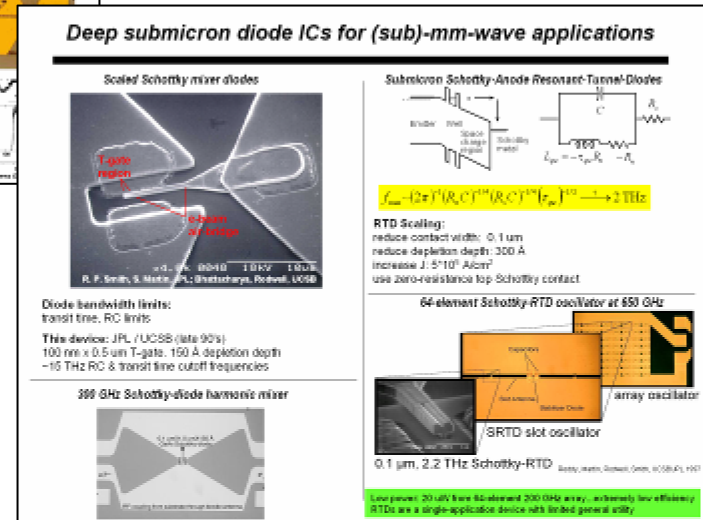


Backups

Submicron diodes for sub-millimeter-waves

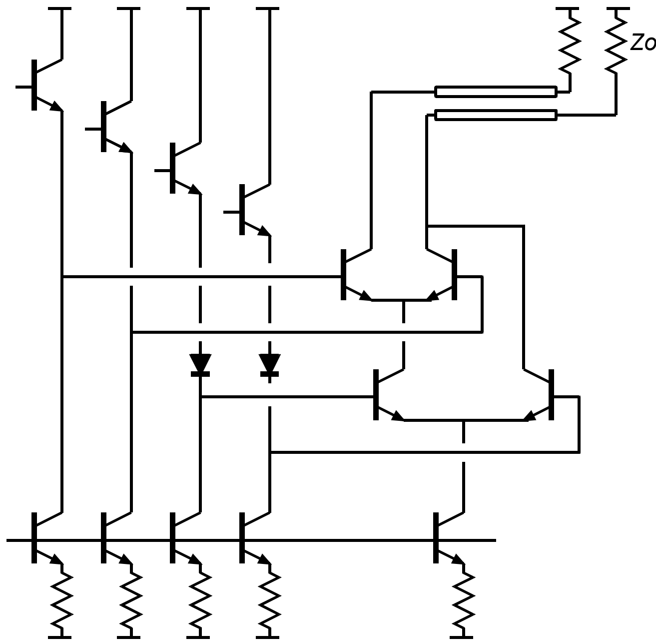




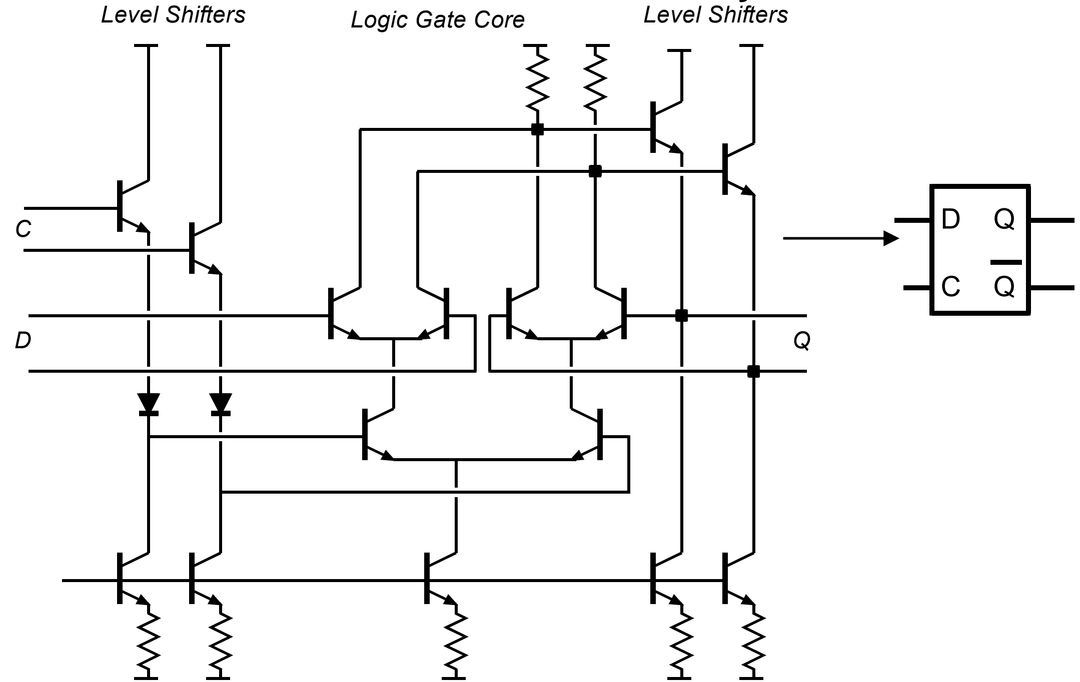


Hierarchy of ECL Static Frequency Divider

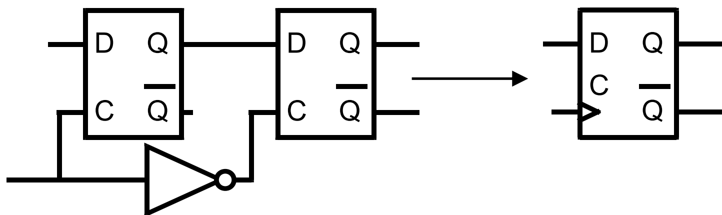
ECL NAND/NOR Gate



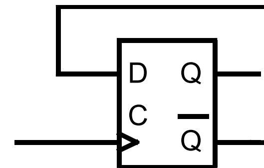
ECL Latch: level-clocked memory element



Master-Slave Latch: transition-clocked memory element



2:1 Static Frequency Divider



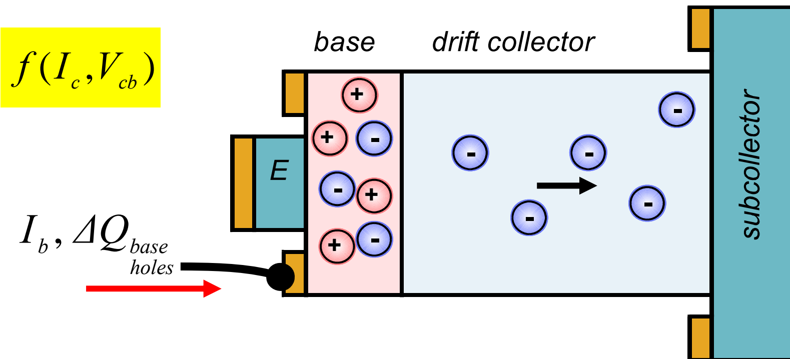
Transit time Modulation Causes C_{cb} Modulation

$$Q_{\substack{base\\holes}} = \text{constant} + Q_{\substack{base\\electrons}} + \int_0^{T_c} qn(x)A(1 - x/T_c)dx + V_{bc}\varepsilon A/T_c = f(I_c, V_{cb})$$

(The terms from "constant" through $V_{bc}\varepsilon A/T_c$ are struck through.)

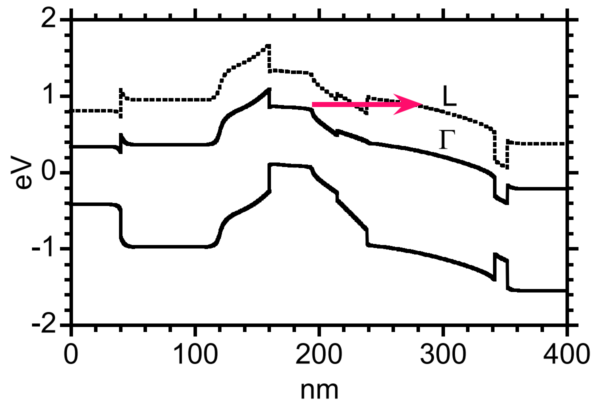
$$C_{cb} \equiv -\frac{\partial Q_{base\ holes}}{\partial V_{cb}} \qquad \tau_f \equiv \frac{\partial Q_{base\ holes}}{\partial I_c} \Rightarrow \frac{\partial C_{cb}}{\partial I_c} = -\frac{\partial \tau_f}{\partial V_{cb}}$$

Camnitz and Moll, Betser & Ritter, *D. Root*



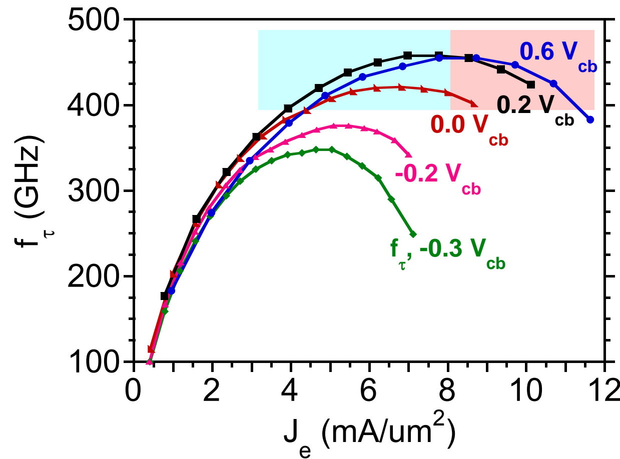
Collector Velocity Modulation :

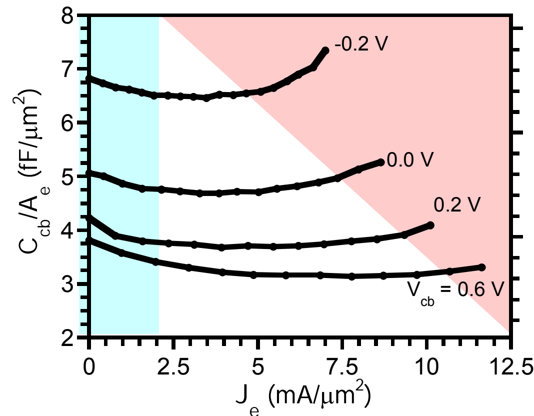
$$\partial \tau_f / \partial V_{cb} > 0 \Rightarrow \partial C_{cb} / \partial I_c < 0$$



Increase in τ_c with V_{cb} → reduced C_{cb}

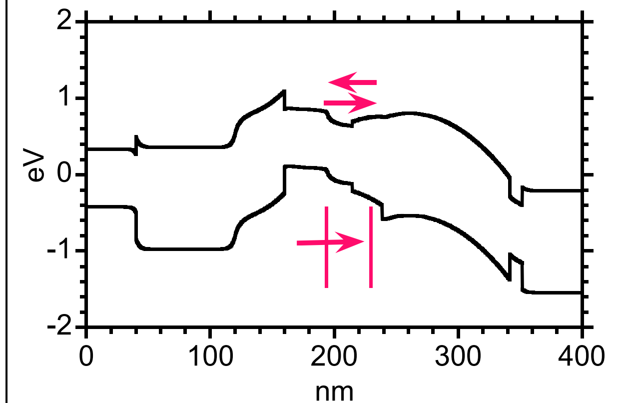
- ***strong effect in InGaAs SHBTs***
- ***weak effect in InP DHBTs***





Kirk Effect :

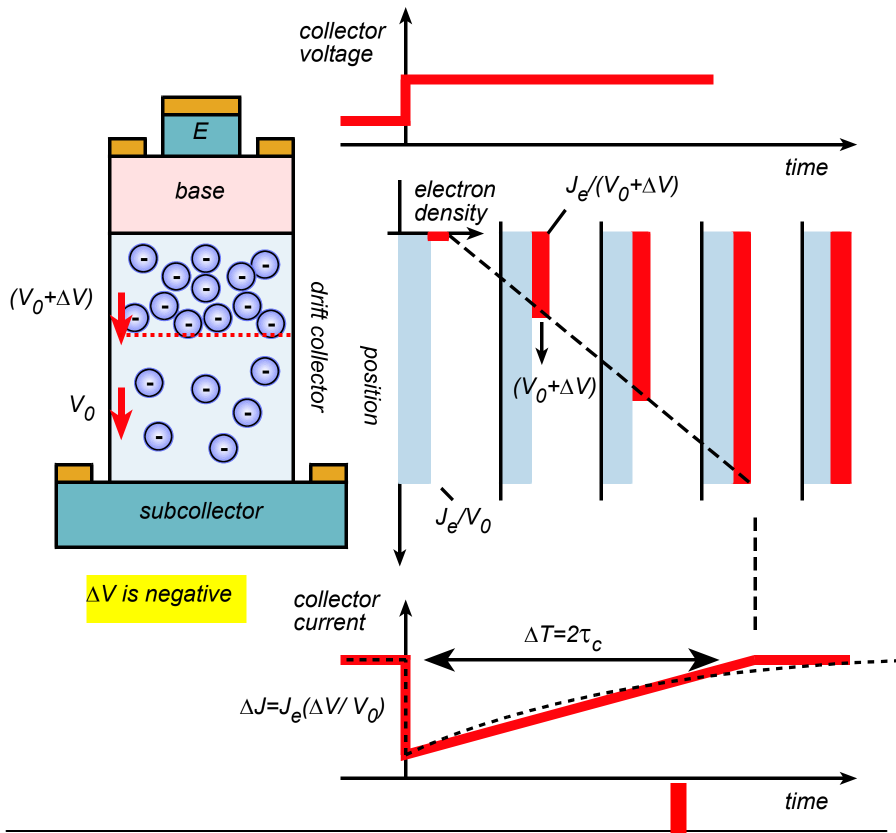
$$\partial \tau_f / \partial V_{cb} < 0 \Rightarrow \partial C_{cb} / \partial I_c > 0$$

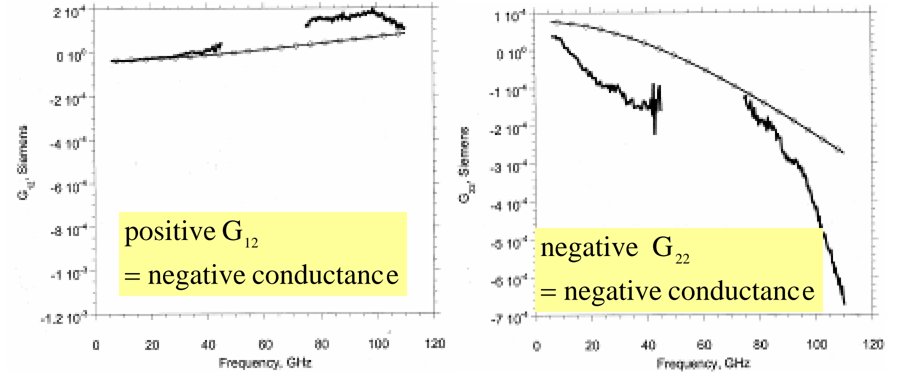


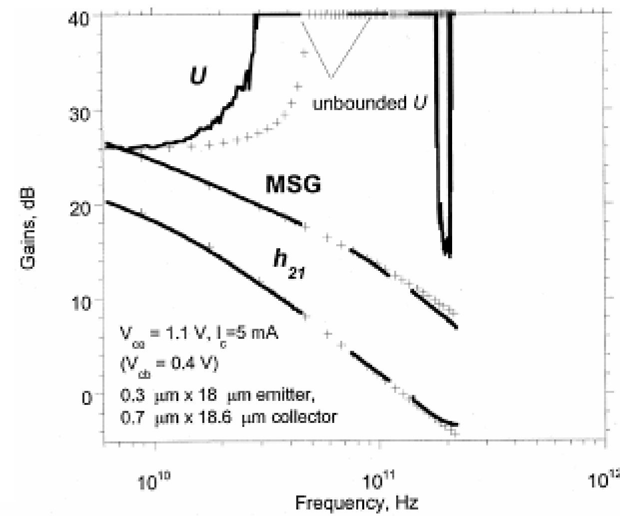
Increase in C_{cb} is due to both

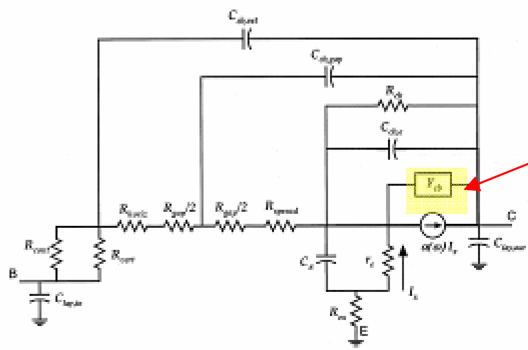
- ***base pushout into collector***
- ***and modulation of τ_b by V_{cb}***

Transit time Modulation → Negative Resistance → Infinite Gain









negative capacitance

$$C_{cb,canc} = -I_c\left(\partial\tau_f / \partial V_{cb}\right)$$

negative resistance

$$R = 2(\tau_c / 3C_{cb,canc})$$