# InP Bipolar Transistors: High Speed Circuits and Manufacturable Submicron Fabrication Processes

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***Abstract* — Compared to SiGe, InP HBTs offer superior electron transport but inferior scaling and parasitic reduction. Figures of merit for mixed-signal ICs are developed and HBT scaling laws for improved circuit speed are introduced. Device and circuit results are summarized, including >370 GHz $f_\tau$ & $f_{max}$ HBTs, 174 GHz amplifiers, 75 GHz power amplifiers, 87 GHz static frequency dividers, and 8 GHz Δ–Σ ADCs. To compete with 100 nm SiGe processes, InP must be similarly scaled. Device structures and initial results are shown for two processes intended for high-yield fabrication of low-parasitic InP HBTs at ~300 nm emitter width.**

## I. Introduction

Despite the rapidly improving bandwidth of scaled CMOS processes, bipolar ICs continue to find applications in 10-40 Gb/s optical transmission systems, in RF/microwave transceivers, and in high-frequency ADCs and DACs. While SiGe HBT is superior for lower GHz frequencies, SiGe and InP HBT processes compete for applications at the highest frequencies.

InP has substantially better electron transport properties than silicon. Effective collector electron velocities *measured* in thin (150-200 nm) InP collectors are $3-4\cdot10^7$ cm/s, as compared to $10^7$ cm/s for Si. With depletion thicknesses selected for equal transit times and Kirk-effect limits, the InP HBT has smaller collector capacitance and larger breakdown voltage. Base electron diffusivity in $\sim10^{20}$ /cm$^3$-doped InGaAs is ~40 cm$^2$/s, as compared to ~4 cm$^2$/s in SiGe. This results in smaller $\tau_b$ at a given base thickness. Typical intrinsic base sheet resistance is much lower (~500 vs. ~5000 Ω/square), resulting in lower $R_{bb}$ at a given emitter width. As a consequence, given the same junction dimensions, an InP HBT would have ~3:1 greater bandwidth than a SiGe HBT. Given devices designed for the same bandwidth, an InP HBT would have ~3:1 greater breakdown voltage. Today, SiGe HBTs are fabricated with much narrower junctions and much smaller extrinsic parasitics. Consequently, the two technologies today have comparable bandwidth, while SiGe offers much higher integration scales. It is therefore imperative to develop high-yield fabrication processes for highly scaled InP HBTs.

## II. HBT Performance Metrics

In designing HBTs for high-speed ICs, performance objectives must be defined. $f_\tau$ and $f_{\max}$ are of limited value in predicting the speed of large-signal circuits such as logic gates, latched comparators in ADCs, current-steering switches in DACs, and the limiting amplifiers, decision circuits, modulator drivers, and PLLs in optical fiber transceivers.

| .. | $C_{je}$ | $C_{cbx}$ | $C_{cbi}$ | $\tau_f I_E/\Delta V_L$ | $\tau_W I_E/\Delta V_L$ |
|---|---|---|---|---|---|
| $\Delta V_L/I_E$ | 1 | 6 | 6 | 1 | 1 |
| $kT/qI_E$ | 0.5 | 1 | 1 | 0.5 | 0 |
| $R_{EX}$ | -0.3 | 0.5 | 0.5 | 0.5 | 0 |
| $R_{bb}$ | 0.5 | 0 | 1 | 0.5 | 0 |

(a)

| .. | $C_{je}$ | $C_{cbx}$ | $C_{cbi}$ | $\tau_f I_E/\Delta V_L$ | $\tau_W I_E/\Delta V_L$ | sum |
|---|---|---|---|---|---|---|
| $\Delta V_L/I_E$ | 11% | 16% | 22% | | | 49% |
| $\Delta V_L/I_E$ | | | | 15% | 18% | 33% |
| $kT/qI_E$ | | | | 1% | | 1% |
| $R_{EX}$ | -1% | | | 1% | | 0% |
| $R_{bb}$ | 5% | | 3% | 7% | | 15% |
| sum | 16% | 16% | 25% | 24% | 18% | 100% |
| | | 42% | | | | |

(b)

Table. 1: (a) Approximate delay coefficients $a_{ij}$ for an ECL M-S latch. Delay is of the form $T_{gate}=1/2\,f_{\text{clock,max}}=\sum a_{ij}R_iC_j$ . (b) Proportions of total gate delay for a 300-nm scaling-generation HBT with target 260 GHz clock rate. $C_{je}$ is the emitter depletion capacitance, $C_{cbx}$ and $C_{cbi}$ the extrinsic and intrinsic collector base capacitances, $\tau_f=\tau_b+\tau_c$ the forward transit time, $\tau_W$ the wiring delay, $I_E$ the emitter current, $\Delta V_L$ the logic voltage swing, and $R_{ex}$ and $R_{bb}$ the parasitic emitter and base resistances. $R_{ex}$ influences $f_{\text{clock,max}}$ *indirectly* through increased $\Delta V_L$ .

Consider the maximum clock frequency $f_{\text{clock,max}}$ of an ECL master-slave latch, a key logic component. Limiting amplifier and DAC risetime analyses are similar. Approximate delay expressions are found by charge-control hand analysis or by fitting to SPICE simulations [1,2],

$$T_{gate}=1/2\,f_{\text{clock,max}}=\sum a_{ij}R_iC_j \qquad (1)$$

Table 1 gives the coefficients $a_{ij}$ and the components of the total delay for a 300-nm scaling-generation HBT with target 260 GHz clock rate.

Viewed in terms of resistances, 72% of the total delay is associated with the load resistance $\Delta V_L/I_E$ . High

current density is desirable. Since the logic voltage swing $\Delta V_L$ must be at least $4(kT + R_{EX} I_E)$, increased current density much be accompanied by reduced emitter resistance, so as to maintain low $\Delta V_L$. Emitter resistance thus plays a much larger proportional role in logic speed than it does in $f_\tau$, and very low $R_{EX}$ is required. Viewed in terms of capacitances, 58% of the total delay is associated with charging the depletion capacitances $C_{cb} + C_{je}$, and only 18% with $\tau_f$, even given the assumed transistor design. In past UCSB HBT logic ICs [3,4], depletion capacitance charging constituted ~85% of the total delay.

| Parameter | Gen. 1 | Gen. 2 | Gen. 3 |
|---|---|---|---|
| MS-DFF speed | 60 GHz | 121 GHz | 260 GHz |
| Emitter Width | 1 μm | 0.8 μm | 0.3 μm |
| Parasitic Resistivity | 50 Ω-μm$^2$ | 20 Ω-μm$^2$ | 5 Ω-μm$^2$ |
| Base Thickness | 400Å | 400Å | 300 Å |
| Doping | 5 10$^{19}$/cm$^2$ | 7 10$^{19}$/cm$^2$ | 7 10$^{19}$/cm$^2$ |
| Sheet resistance | 750 Ω | 700 Ω | 700 Ω |
| Contact resistance | 150 Ω-μm$^2$ | 20 Ω-μm$^2$ | 20 Ω-μm$^2$ |
| Collector Width | 3 μm | 1.6 μm | 0.7 μm |
| Collector Thickness | 3000 Å | 2000 Å | 1000 Å |
| Current Density | 1 mA/μm$^2$ | 2.3 mA/μm$^2$ | 12 mA/μm$^2$ |
| $A_{collector}/A_{emitter}$ | 4.55 | 2.6 | 2.9 |
| $f_\tau$ | 170 GHz | 248 GHz | 570 GHz |
| $f_{max}$ | 170 GHz | 411 GHz | 680 GHz |
| $I_E / L_E$ | 1 mA/μm | 1.9 mA/μm | 3.7 mA/μm |
| $\tau_f$ | 0.67 ps | 0.50 ps | 0.22 ps |
| $C_{cb} / I_c$ | 1.7 ps/V | 0.62 ps/V | 0.26 ps/V |
| $C_{cb}\Delta V_{logic} / I_c$ | 0.5 ps | 0.19 ps | 0.09 ps |
| $R_{bb} /(\Delta V_{logic} / I_c)$ | 0.8 | 0.68 | 0.99 |
| $C_{je}(\Delta V_{logic} / I_C)$ | 1.7 ps | 0.72 ps | 0.15 ps |
| $R_{ex} /(\Delta V_{logic} / I_c)$ | 0.1 | 0.15 | 0.17 |

Table. 2: Technology roadmaps for 40, and 160 Gb/s ICs. Master-slave latch delay includes 10% interconnect delay.

In HBTs designed for fast logic, fiber transmission, and mixed-signal ICs, low $C_{cb}\Delta V_L / I_E$ and $C_{je}\Delta V_L / I_E$ charging times are critically important, necessitating very high current density, minimal excess collector junction area, and very low emitter access resistance. Transit delay plays a relatively smaller role, hence HBTs can be designed for high $f_\tau$ without significantly benefiting mixed-signal IC speed.

## II. Scaling: Laws, Limitations, & Roadmaps

Given the significant contribution of many transistor parasitics on circuit speed, a systematic approach is desirable in order to obtain balanced and proportional improvements in transistor performance with device scaling [1,4]. To obtain a 2:1 speed increase in an arbitrary circuit, all device capacitances and transit delays must be reduced 2:1 while maintaining constant the bias current, the transconductance, and all parasitic resistances. This is accomplished by thinning the collector depletion layer 2:1, thinning the base $\sqrt{2}$:1, reducing the emitter and collector junction widths 4:1, reducing the emitter resistance per unit area 4:1, and increasing the current density 4:1. It is essential to note that thinning the collector depletion layer 2:1 increases the collector capacitance per unit area 2:1 but increases the Kirk-effect-limited current density 4:1; $C_{cb} / I_E$ is thus reduced 2:1. If the base Ohmic contacts lie above the collector junction, their width must be reduced 2:1, necessitating a 4:1 reduction in contact resistivity; if the contacts do not lie above the junction, their resistivity can remain unscaled.

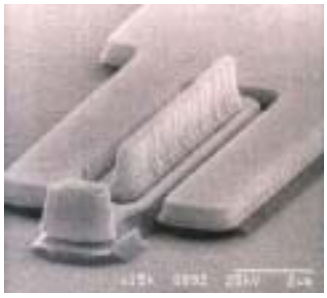

Figure. 1: SEM photograph of a typical InP Mesa HBT

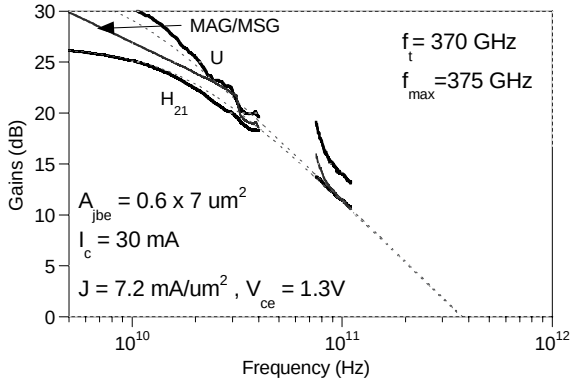


Figure. 2: DC and microwave parameters of an InP DHBT with a 1500-Å thick collector and a 5-8x10$^{19}$/cm$^3$ carbon-doped InGaAs base.

There are significant challenges to scaling. In typical InP mesa HBTs, the collector-base junction lies below the full width of the base contact, hence narrow collector junctions demand narrow base contacts. This demands both low contact resistance and low contact metal sheet resistance. Emitter contact resistivity is a key challenge, as very low values (~5 $\Omega - \mu m^2$) are required for 200 GHz clock speed. Current density must be very high (~10 mA/$\mu m^2$), hence thermal resistance must be very low [5]. Breakdown voltage progressively decreases, preventing scaling of HBTs for higher-voltage circuits.

Given technology improvements feasible in the next 2-3 years, table 2 shows scaling roadmaps for 40 Gb/s, 80 Gb/s, and 160 Gb/s ICs, specified with a M/S latch toggle frequency 1.5:1 higher than the target data rate.

## II. Transistor & IC Results For Mesa HBTs

InP HBTs today typically use a mesa structure (fig. 1). Production processes use dimensions and have performance typical of the 1st-generation HBT of table 2. Leading research processes typically employ ~0.4 $\mu$m emitter widths with significant collector undercut for $C_{cb}$ reduction. Mesa processes are simple and low-investment, but only moderate yield, with 1000-2000 HBTs/IC being feasible.

Fig. 2 shows the measured DC parameters of a recent mesa InP DHBT from our laboratory [6]. The transistor exhibits >370 GHz $f_\tau$ and $f_{\max}$, $C_{cb}/I_E$ =0.4 ps/V at $V_{cb}$ =0 volts (ECL emitter-follower bias), while $R_{ex}/(\Delta V_{\text{logic}}/I_E)$ =0.33 at $10^6$ A/cm$^2$. These parameters are sufficient for ~160 GHz MS-DFF clock rate. $V_{BR,CEO} \cong 5$ V at low currents; usable voltage at $10^6$ A/cm$^2$ is > 2.5 V, the difference due to self-heating. InP mesa HBTs with thicker 2000 Å collectors obtain 280 GHz $f_\tau$, 400 GHz $f_{\max}$, and $V_{BR,CEO}$ =7 Volts [7]; such devices are suitable for 100-200 GHz power amplifiers.

We had earlier developed a modified mesa HBT process which employed a substrate transfer step [4]. This allowed 2-sided processing of the transistor structure, permitting very narrow collector junctions and low $R_{bb}C_{cb}$ time constants. The transistors exhibit a weak negative collector-base conductance [8] resulting in *infinite* unilateral power gain above 30 GHz (fig 3). An amplifier using a single transferred-substrate HBT obtained 6.3 dB gain at 174 GHz (fig. 4) [9]. DHBTs in the transferred-substrate process have obtained 460 GHz $f_{\max}$ [10] ; with these 80 mW power amplifiers (fig. 5) have been demonstrated at 75 GHz [11].

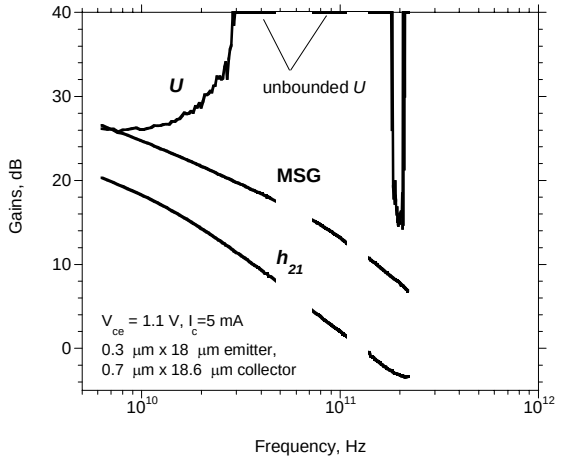


Figure 3: 0.3 $\mu$m transferred-substrate HBT: 5-220 GHz gains

Figure. 4: Single-HBT amplifier with 6.3 dB gain at 174 GHz

Figure. 5: 75 GHz, 80 mW HBT power amplifier in the transferred-substrate process

Moderately more complex ICs have been fabricated at UCSB in a slower (200 GHz $f_\tau$, $f_{\max}$) InP mesa DHBT process. These include an 87 GHz static frequency divider (fig. 6) [3] and an 8 GHz clock $\Delta-\Sigma$ (fig. 6) ADC [12] exhibiting 133 dB (1 Hz) SNR at 74 MHz (equivalent to ~8.8 bits at 200 MS/s)

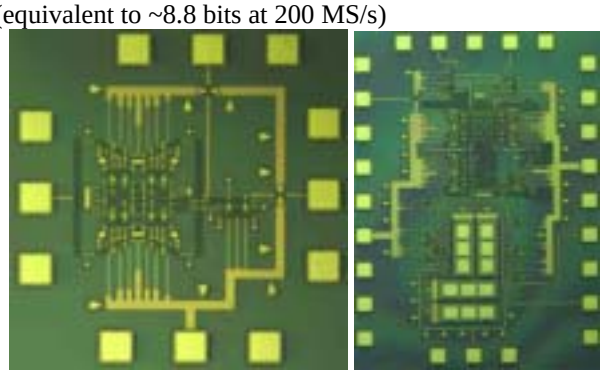

Figure. 6: Left: 87 GHz static frequency divider. Right: 8 GHz $\Delta-\Sigma$ ADC. Both are fabricated using mesa DHBTs.

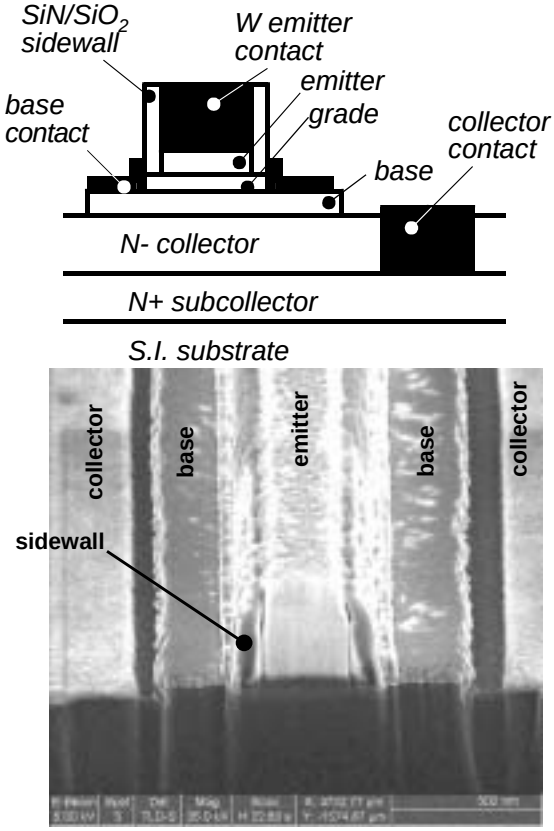


Figure. 7: Submicron-sidewall-spacer emitter-base process; schematic and FIB/SEM cross-section of fabricated device.

## II. Advanced InP HBT Fabrication Processes

SiGe fabrication processes provide high yield, permitting much larger ICs than feasible today in InP. SiGe are much more highly scaled, with ~100 nm emitter dimensions feasible. This increases transistor bandwidth. SiGe processes have extensive parasitic reduction, further improving bandwidth. Regrowth of a T-shaped polysilicon extrinsic emitter produces an emitter contact wider than the junction, reducing $R_{EX}$. Polysilicon base regrowth greatly reduces the sheet resistance in the extrinsic base, reducing $R_{bb}$. The extrinsic base regrowth is over a dielectric spacer layer, reducing $C_{cb}$. We seek

to develop similar processes for InP, increasing fabrication yield, and facilitating deep submicron junction formation and extrinsic parasitic reduction for increased bandwidth. We are pursuing two alternatives

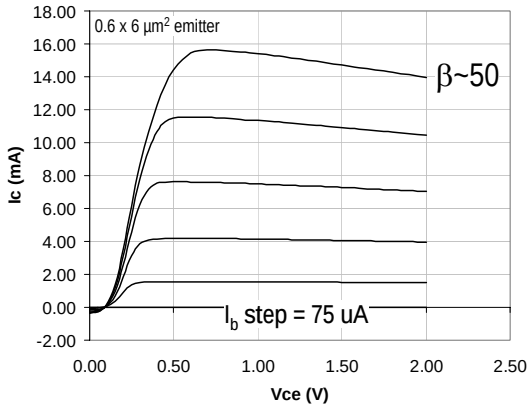


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Figure. 8: DC characteristics of an HBT fabricated using a dielectric sidewall spacer in the emitter-base junction.

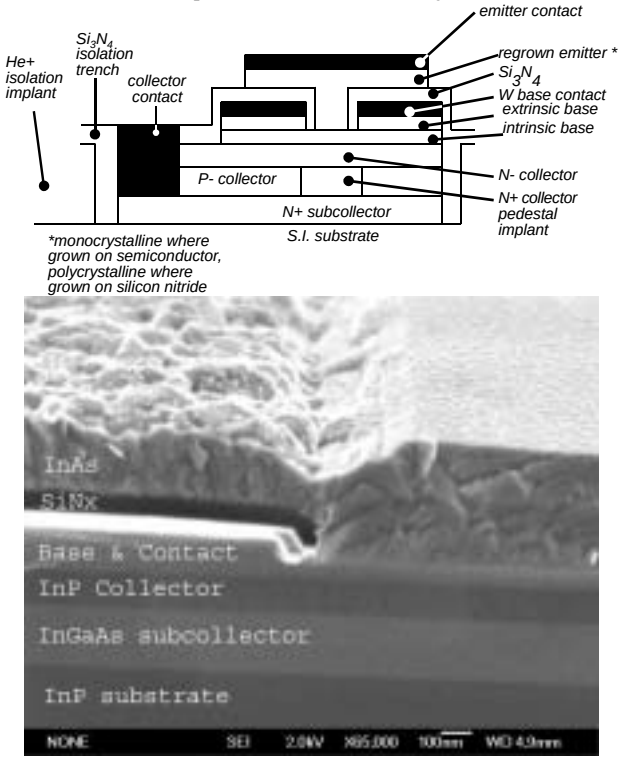


Figure. 9: Polycrystalline extrinsic emitter regrowth HBT: device schematic and regrown junction SEM cross-section.

As a result of both liftoff failures (metal strands shorting emitter and base) and excessive junction etch undercut, self-aligned base-emitter contact liftoff processes become progressively lower-yield at submicron dimensions. An alternative (fig. 7) is to separate base and collector contacts with a dielectric sidewall spacer, similar to a GaAs process reported by Oka [13]. Emitter and base contacts can be sputtered W, rather than evaporated. The process provides $Si_xN_y$ junction passivation and a high-surface-Al-content emitter-base junction ledge for leakage suppression. Initial DC characteristics are shown in figure 8; the transistors show 185 GHz $f_\tau$ & 135 GHz $f_{\max}$.

We are also developing a fabrication process which closely follows the SiGe fabrication process flow (fig. 10) [14]. MBE regrowth of polycrystalline InAs results in low-resistance films suitable for the extrinsic emitter, while recent regrowth experiments indicate that low junction leakage can be obtained even for large junction areas. Through emitter regrowth in a recess-etched window in the base, a low-transit-time intrinsic base and low-sheet-resistance extrinsic base [15] are formed. As with SiGe, the emitter contact can be much wider than the junction. An N+ collector pedestal implant forms a thin collector depletion region under the emitter and a thicker depletion region under the base contacts, reducing $C_{cb}$. We are exploring both dielectric-filled trench and (Fe and He) isolation implantation. Fig. 9 shows an SEM cross-section of a regrown junction. Low leakage large-area junctions have been obtained, as have functioning transistors with submicron emitters. RF devices are now being developed.

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